ATLAS LAr Calorimeter Commissioning for LHC Run-3

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the ATLAS Liquid Argon Calorimeter Group

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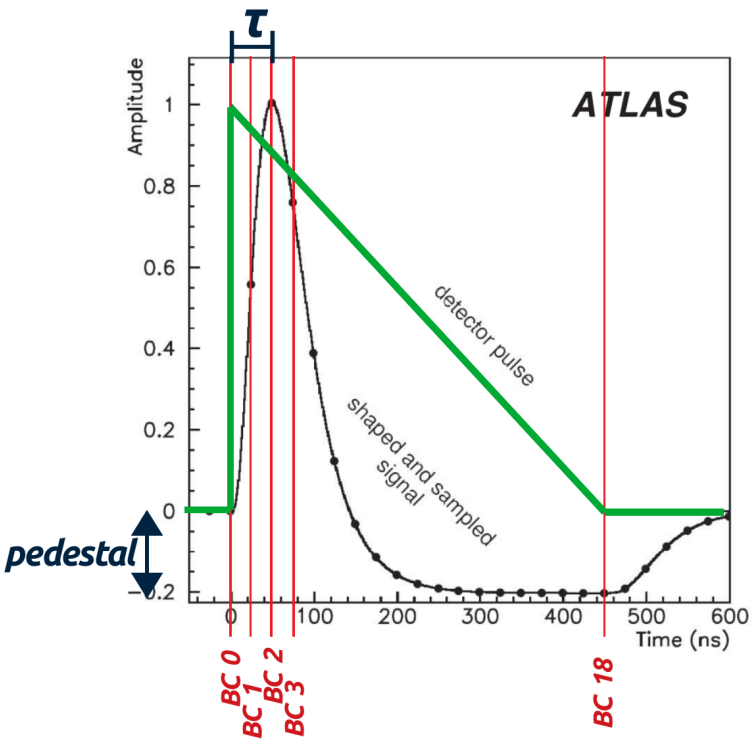
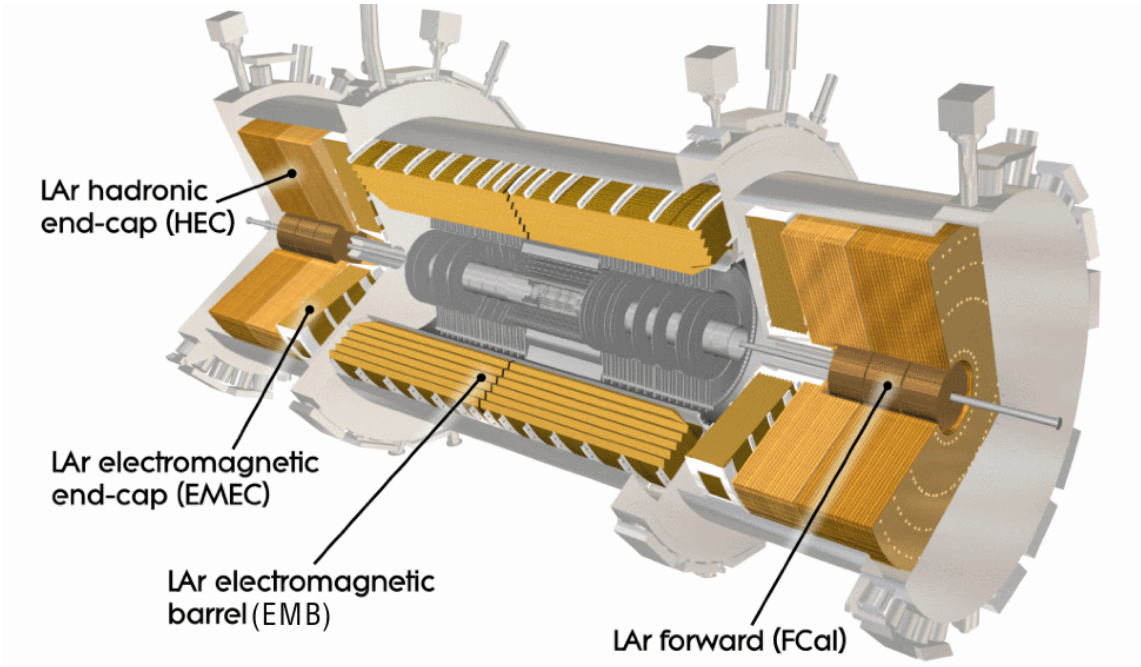
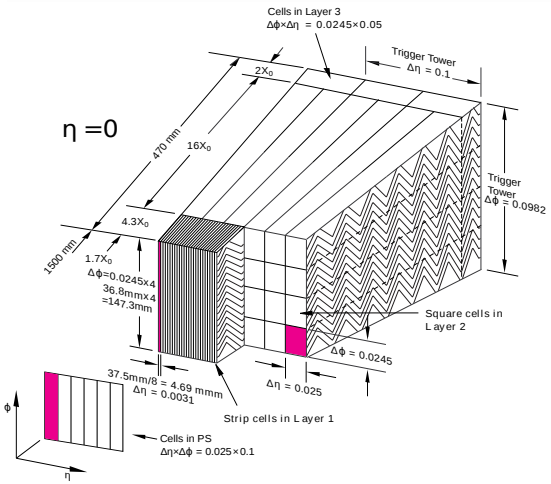
Liquid Argon calorimeter

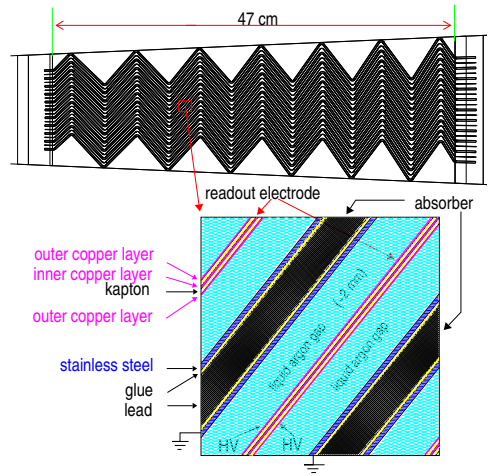
Sampling calorimeter with ∼180k channels

- Four different regions
- Mediums
  - Active: Liquid Argon (∼ 88 K)
  - Passive: Lead (EM), Copper (Had), Tungsten (FCAL)
- Longitudinal segmentation

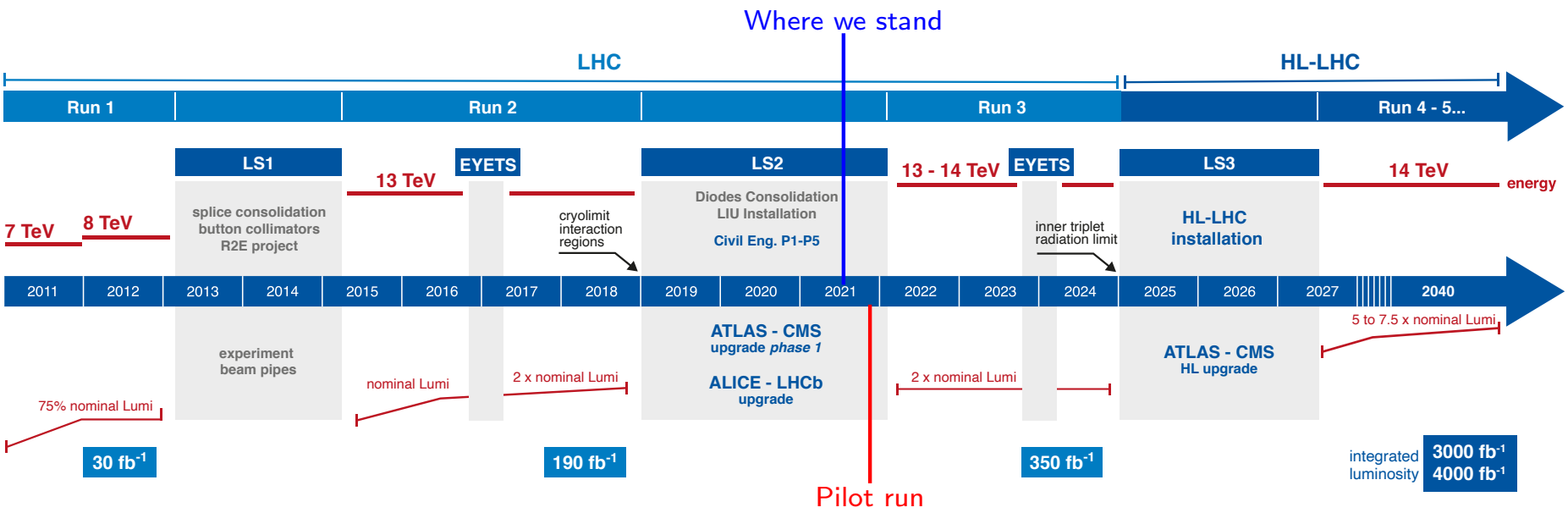








LHC Run3 restart and conditions



- Run3 starting in early 2022
- Pilot run in October 2021
- Luminosity and pileup almost doubled
- ATLAS keeps same L1 and HLT rates
  $\Rightarrow$ we would need to operate at 270 kHz to keep same E_T threshold

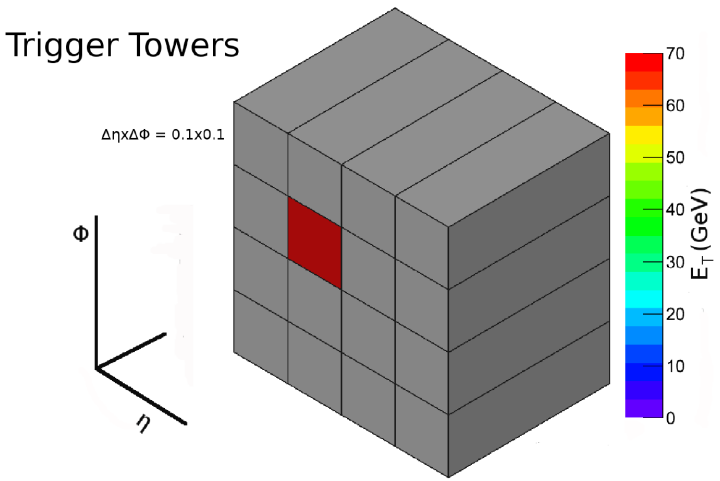
	Run2	Run3	Increase
Lumi [$10^{34}\,cm^{-2}\,s^{-1}$]	1.9	3	$\sim$x1.5
Avg pileup	36	80	$\sim$x2
L1 trigger rate [kHz]	100	100	1
HLT trigger rate [kHz]	1	1	1

$\Downarrow$

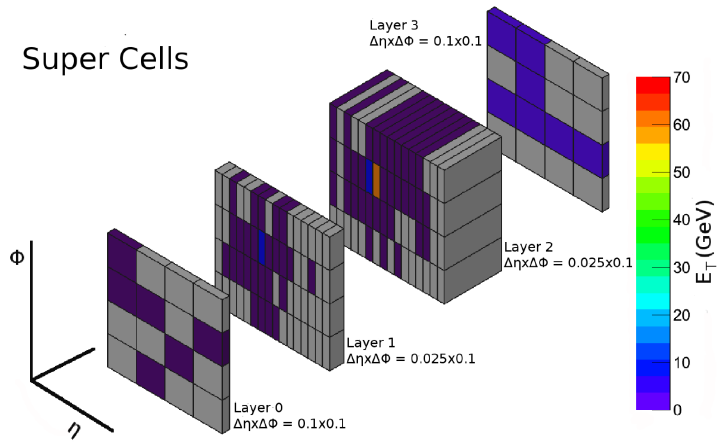
Upgrade Level1 trigger to maintain the same Run2 performances

Phase-I upgrade performance

Run2 ↔ Trigger Tower (TT)



Run3 ↔ Super Cell (SC)



Simulation for a 70 GeV electron

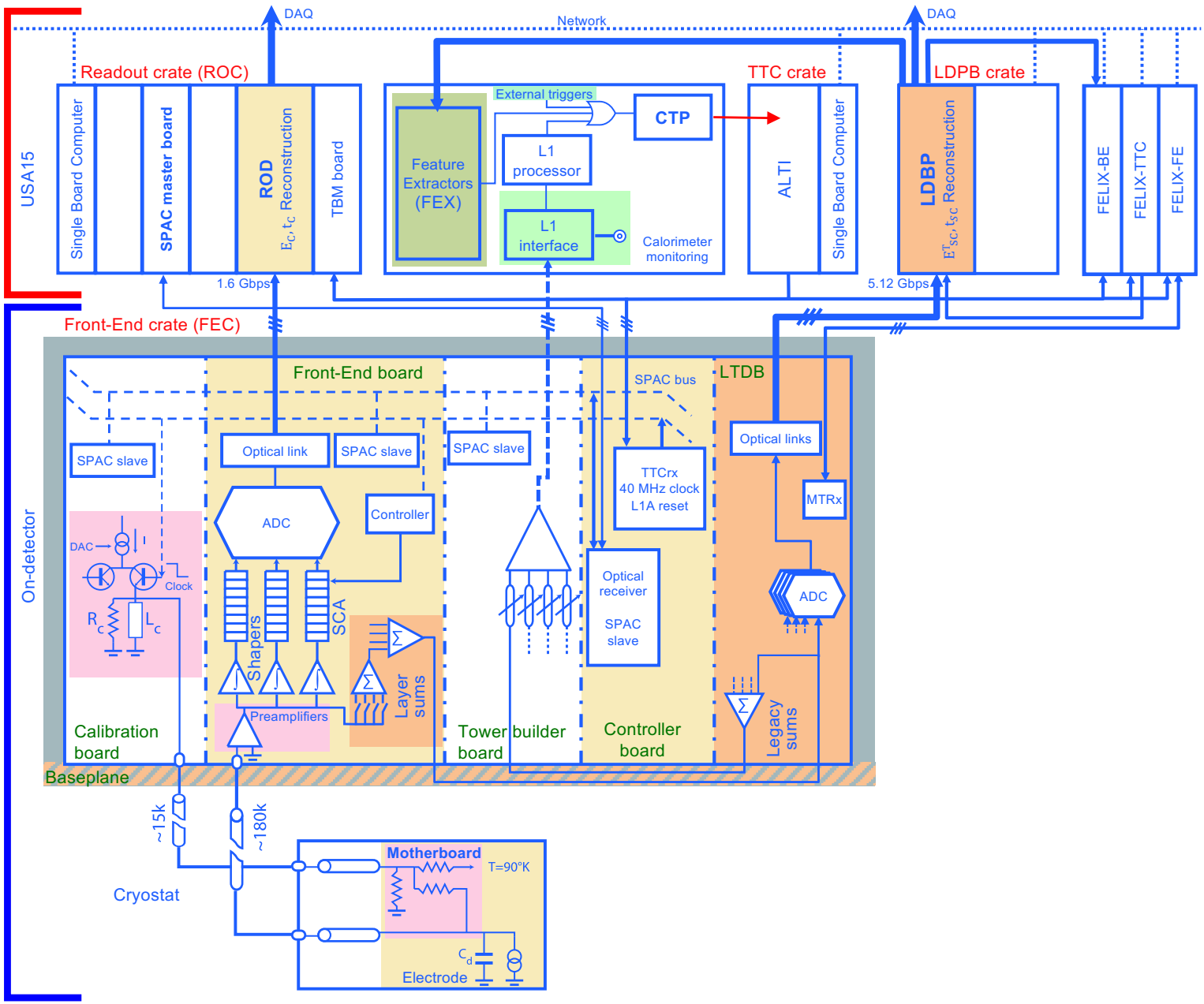
- No longitudinal segmentation
- Fixed size in $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$
- Up to 60 cells from 4 layers
- Only 5.4k TT from 180k cells

- Longitudinally segmented as calorimeter
- Increased granularity in Front and Middle to $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$
- Up to 8 cells from 1 layer
- 34k SCs from 180k cells

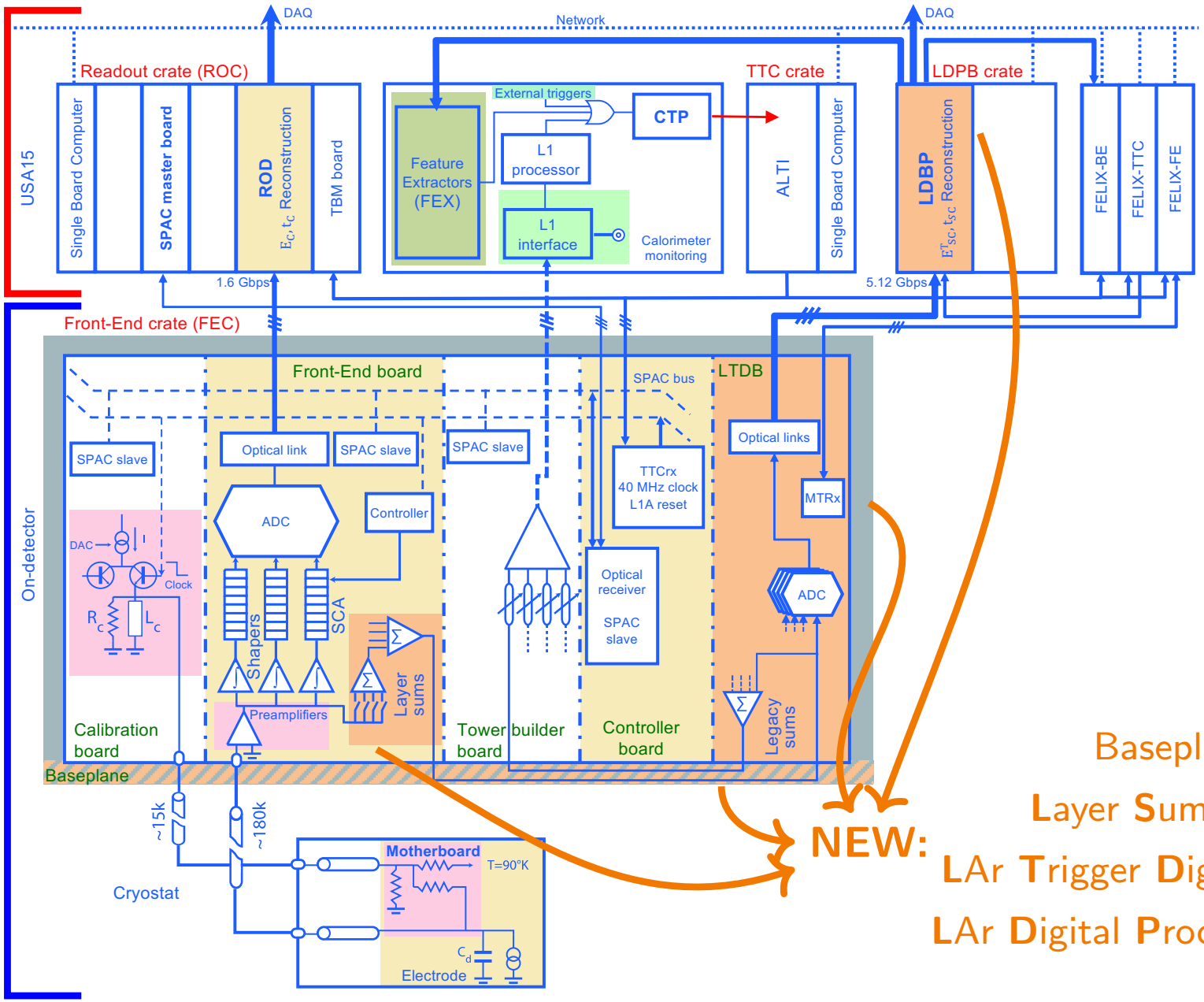
Use more information at trigger level to better reject background

- Thanks to $\sim \times 10$ more cells
- Using topological information as we do in offline analysis
- Better pileup subtraction with advanced algorithms

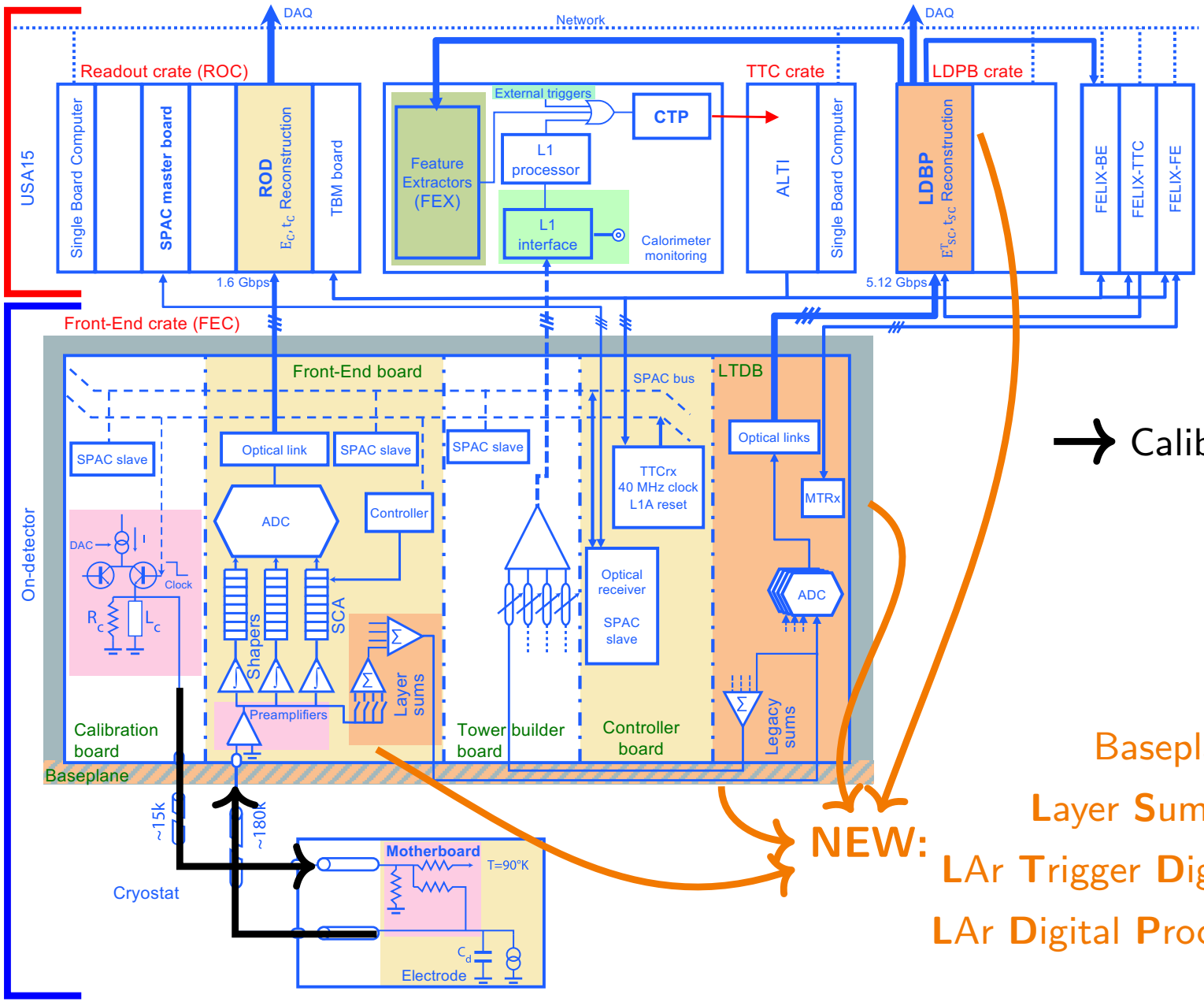
LAr Digital trigger overview



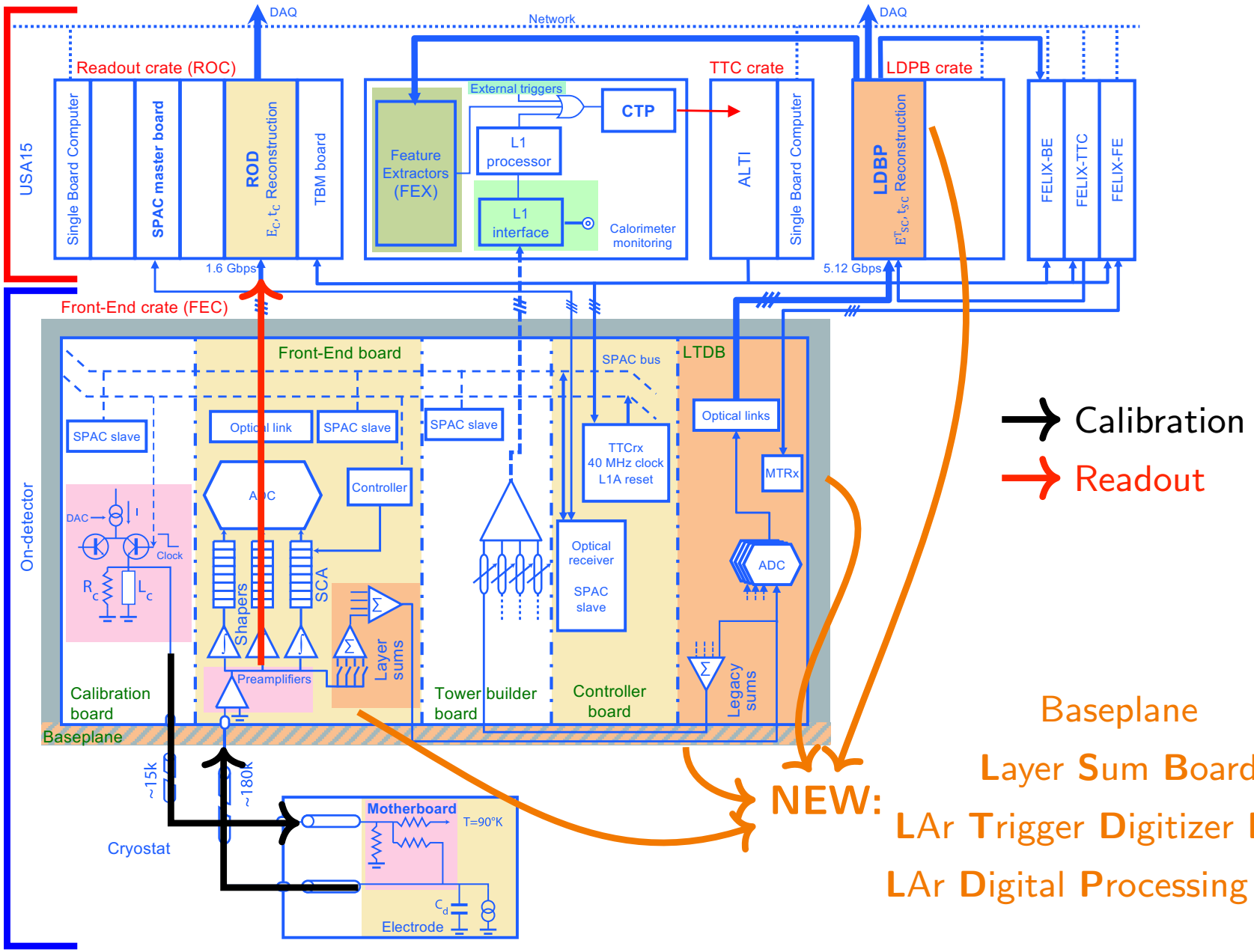
LAr Digital trigger overview



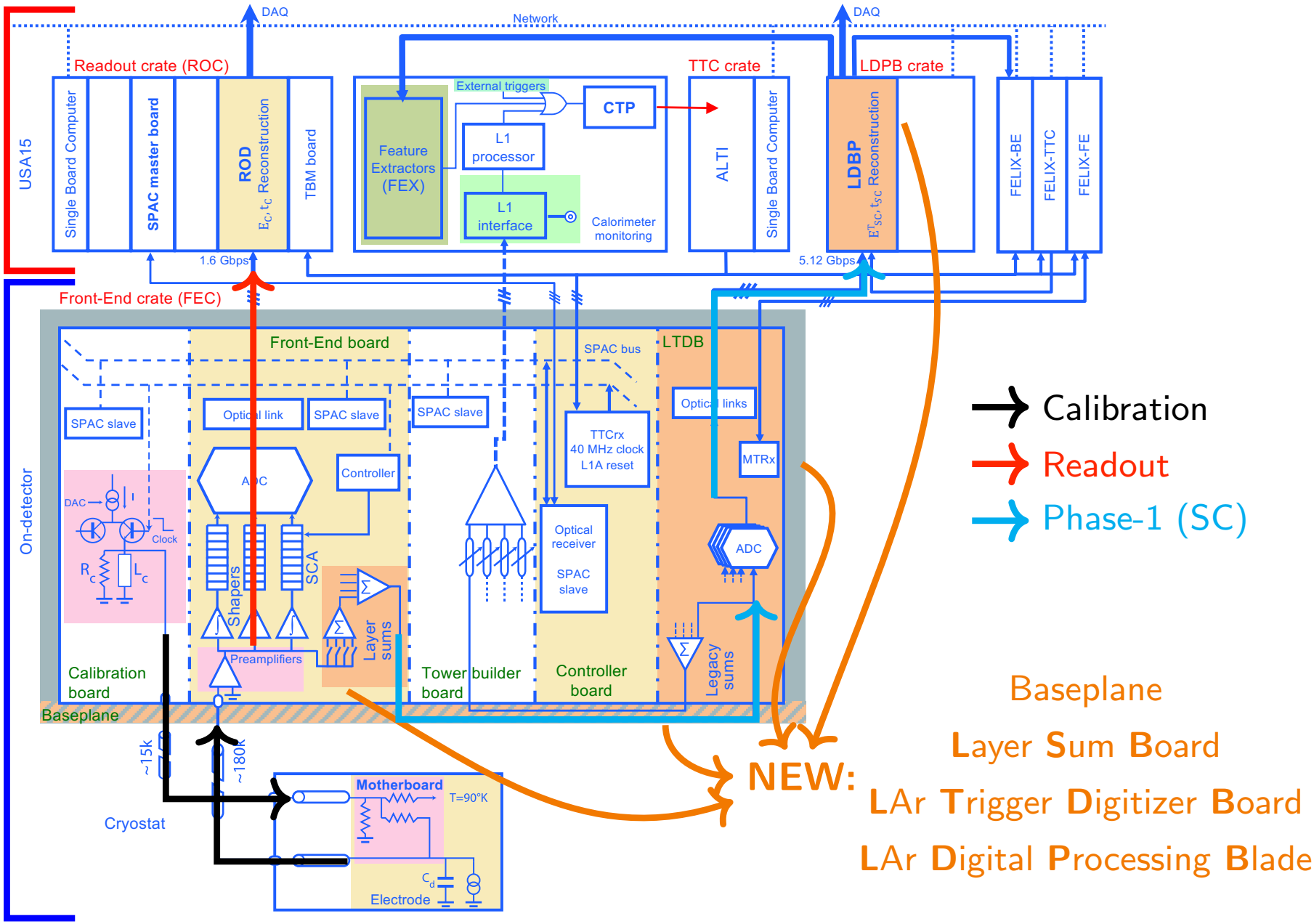
LAr Digital trigger overview



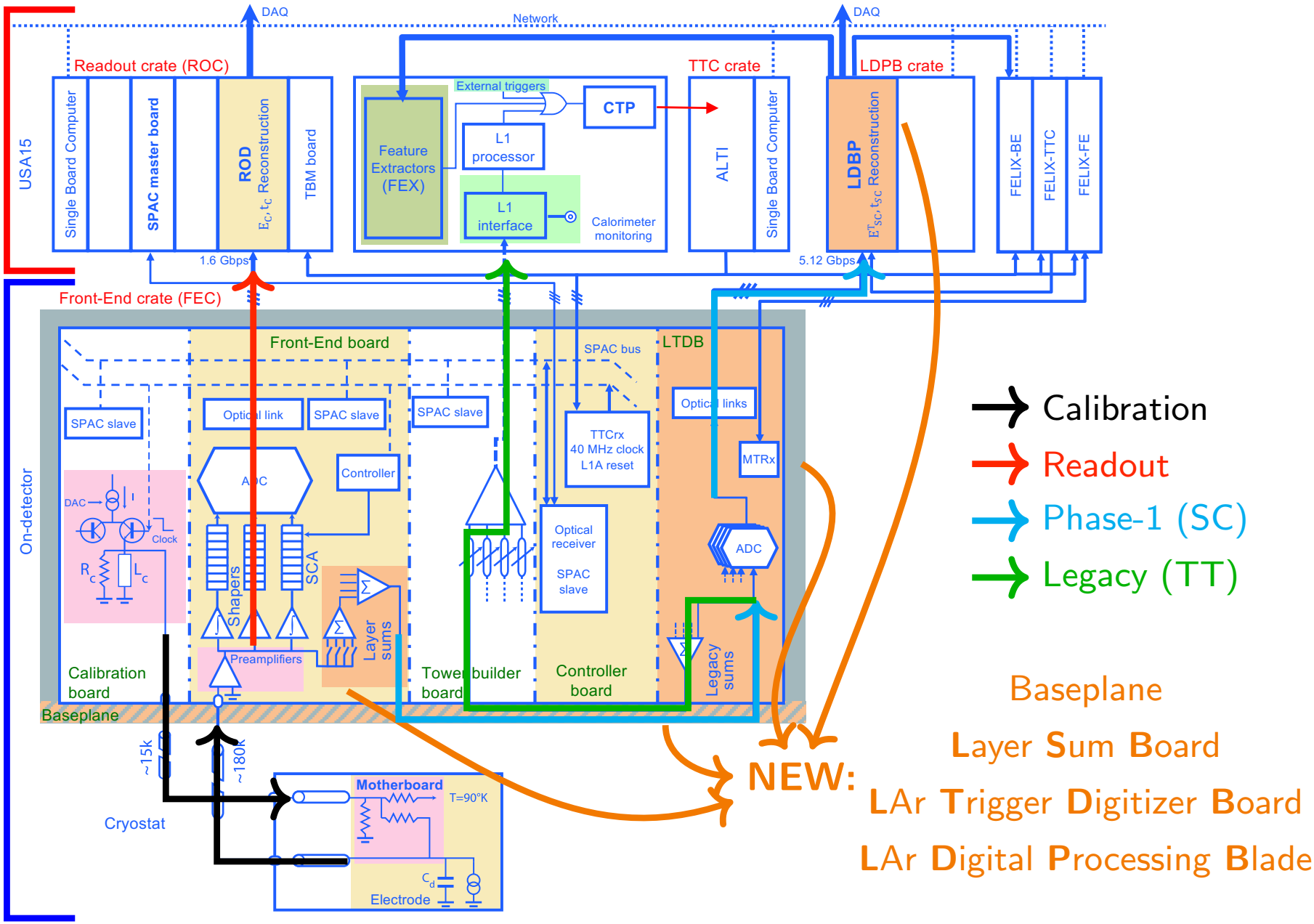
LAr Digital trigger overview



LAr Digital trigger overview



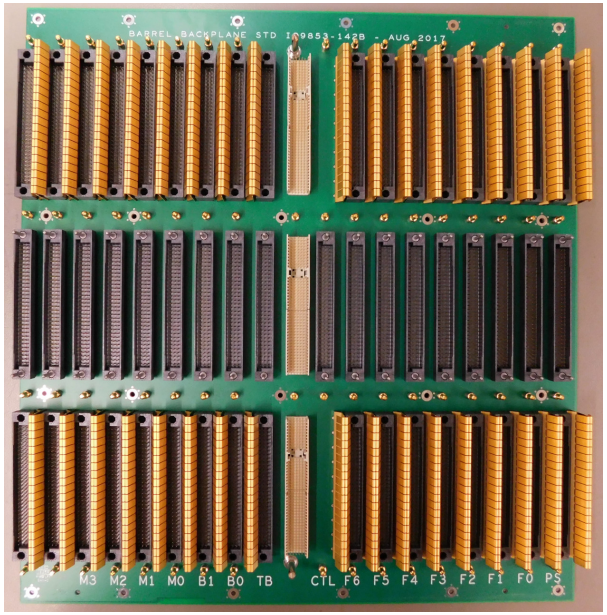
LAr Digital trigger overview

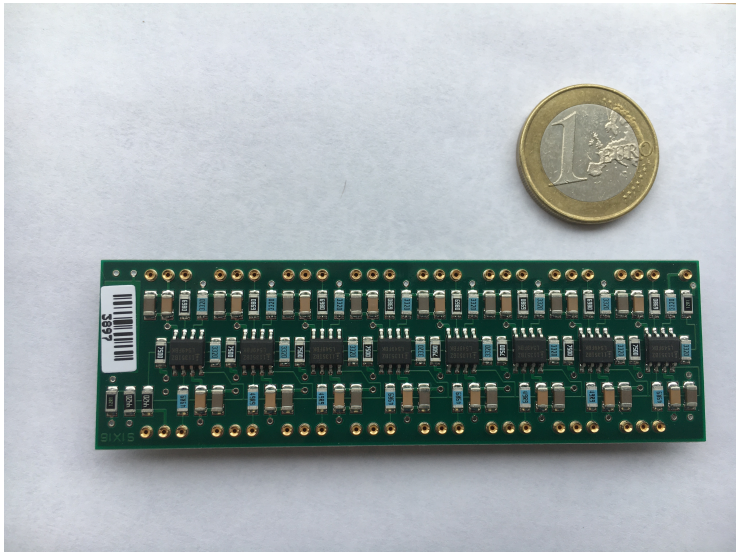


New FrontEnd: Baseplane, LSB

Baseplane

- Connect various boards in the **F**ront **E**nd **C**rate (FEC)
- Replaced to operate digital and legacy system concurrently
  - Additional slots for the new LAr Trigger Digitizer Board (LTDB)
  - Additional routing for both systems
  - Crate re-organization
- Installed 114 baseplanes





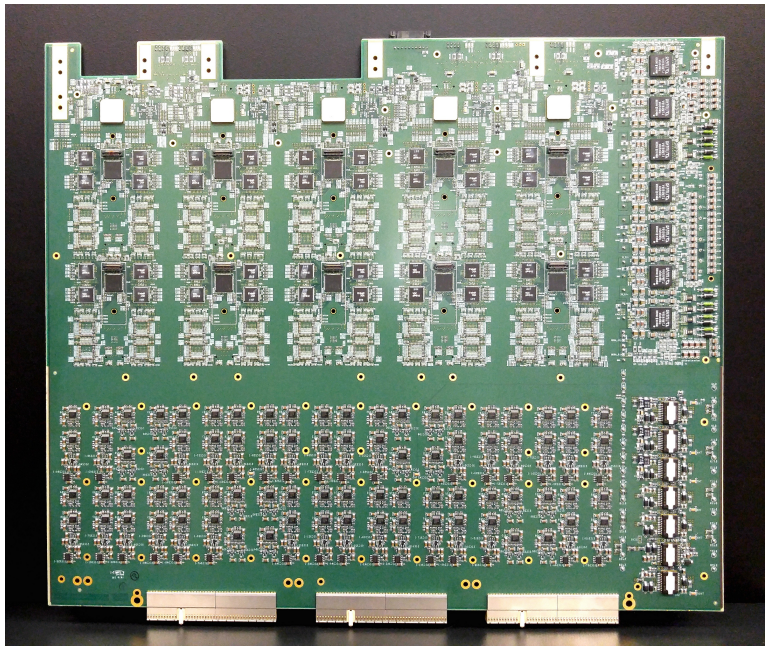
Layer Sum Board

- Plug-in card for Front End Board, 6 different types installed
- Provide signals for LTDB by analogue sums of calo cells
- Replaced: we need finer sum segmentation for SCs in the front and middle layers
- Installed 2968 LSBs

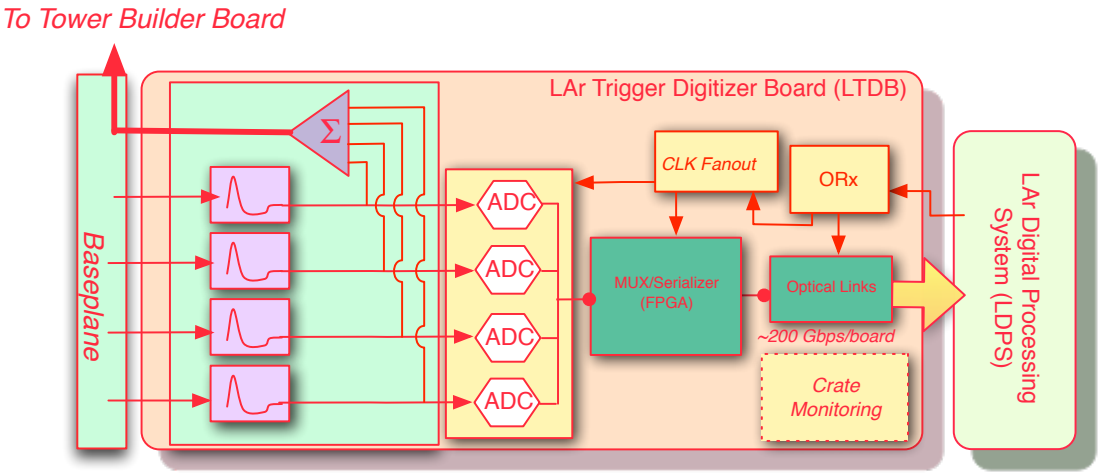
New FrontEnd: LTDB

LAr Trigger Digitizer Board: processing and digitizing SC analogue signals

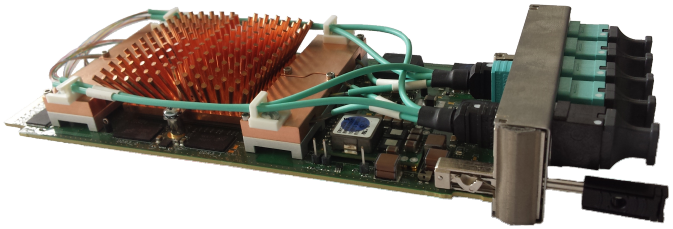
- Custom designed 12 bit ADC at 40 MHz, in 130 nm TSMC technology
  - Least significant bit of the ADC is $\sim$ 150 (300) MeV in Front (Middle) layer
- Processes up to 320 Super Cells
- Provides analogue sums for legacy Trigger Tower boards
- Transmits to LDPB via optical fiber links (8 SCs per fiber at 5.12 Gb/s)
  - Custom serializer (LOCx2) and laser drive (LOCld), using 250 nm SOI process

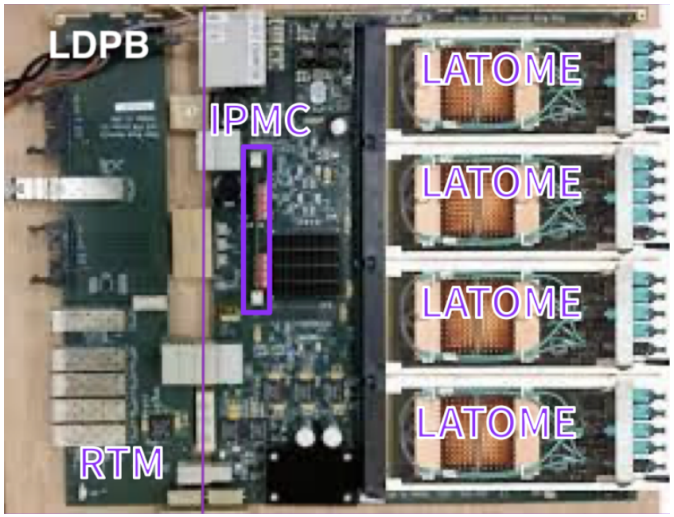


- 124 LTDBs in total, 7 different flavours
- Required to be operational for HL-LHC too
  - After exchange of power mezzanines



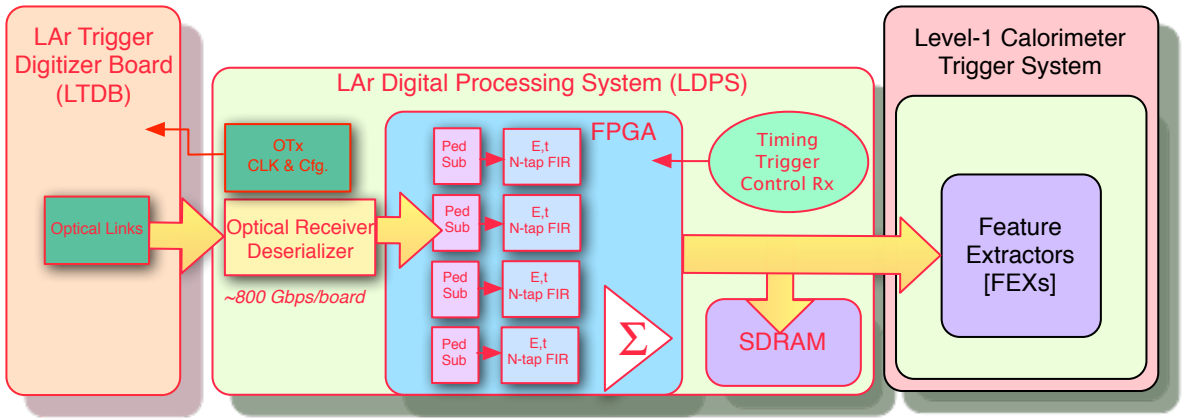
New BackEnd: LDPB





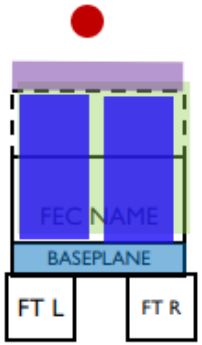
LAr Digital Processing Blade:

- System gets data from LTDB (∼25 Tbps, 40 MHz) and transmit to L1 Calo Trigger (∼41 Tbps, 40 MHz)
- System composed of 30 Blades, each hosting 4 **LA**r **T**rigger pr**O**cessing **ME**zzanines (LATOMEs) over one **LAr C**arrier (LArC)
  - LATOME and LArC operated by commercial FPGAs
    - Intel Arria-10 and Xilinx Virtex 7 respectively
- Main goals: reconstruct E_T and identify bunch cross
  - Strict latency limit for E_T and pulse phase algorithms (5 to 6 bunch crossing)
- System distributed in 3 ATCA crates

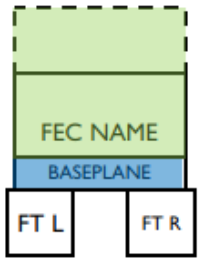


Installation status: Front End

- All crates baseplanes and legacy boards refurbished and installed
- 85% LTDBs are installed and connected (all at CERN)
- Waiting for access, expected finished end July



Fully done

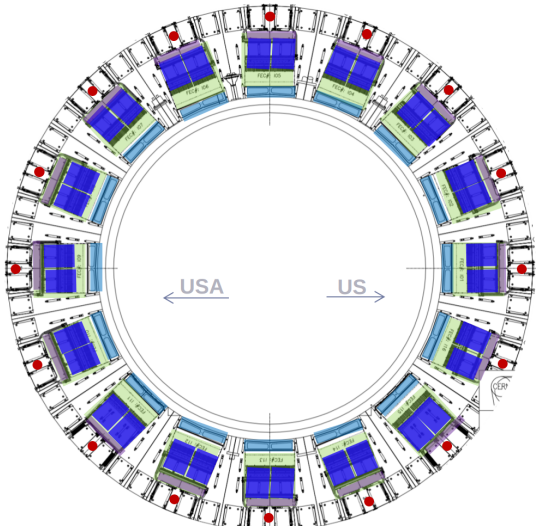


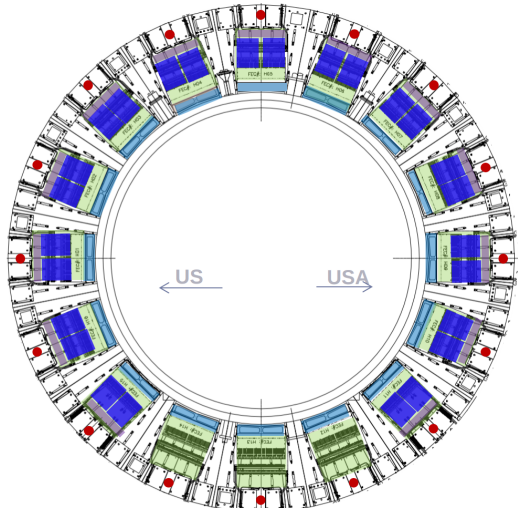
No LTDBs

Side A

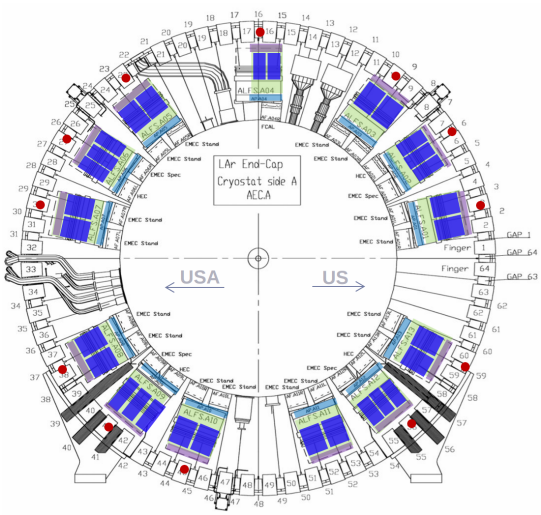
Side C

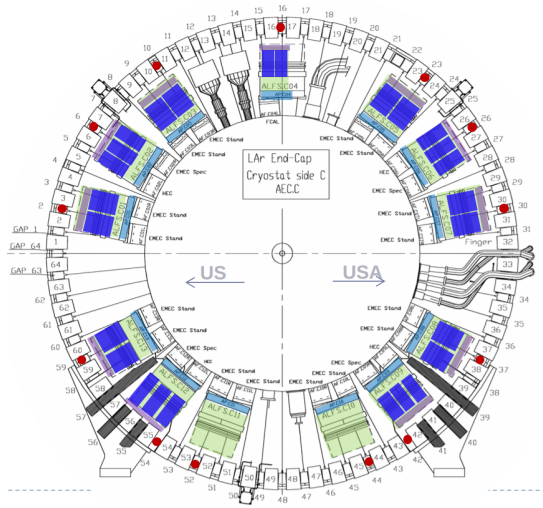
Barrel





EndCap





Installation status: Back End

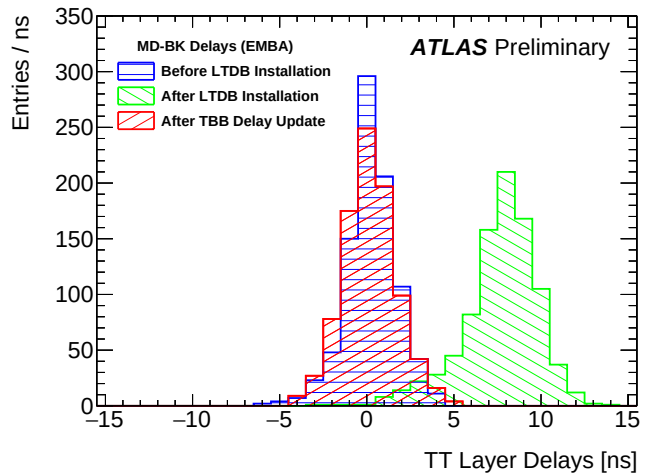
- All LDPB installed in the 3 ATCA crates
  - 10 LArC per crate
  - LArC are grouped by readout regions
- 85% fiber from LTDB to LATOME connected
  - waiting for LTDB installed on front end
- Monitoring and control system in place, included in ATLAS control
- Parallelized configuration of LTDB in place too

Validation and commissioning (1)

Legacy trigger readout

- Additional extra path for TTB ⇒ testing gain and timing at L1
  - Corrections applied, consistent results as before
- Connectivity scan automatised
  - No problems found so far

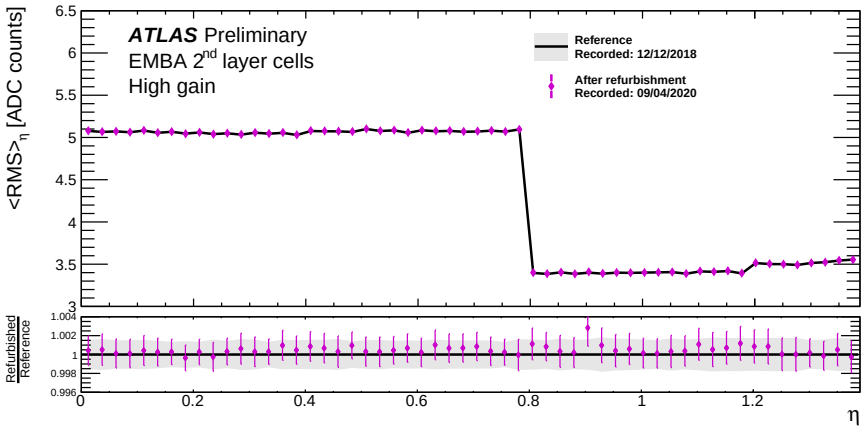
TTB timing correction middle vs back layers



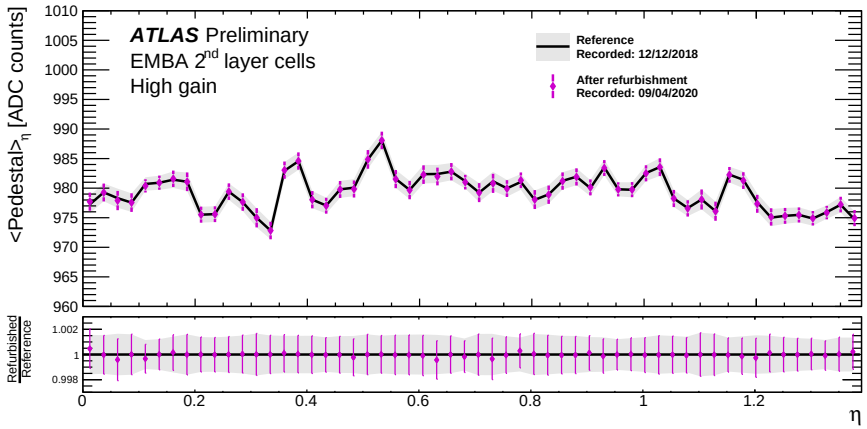
Main data readout

- FEBs refurbished with LSB ⇒ should have similar calibration coefficients and same noise level as before
  - No change in electronic noise level after refurbishment of the FEBs
  - Calibration runs compared to pre-LS2 calibration set show same results

Noise level



Pedestal value

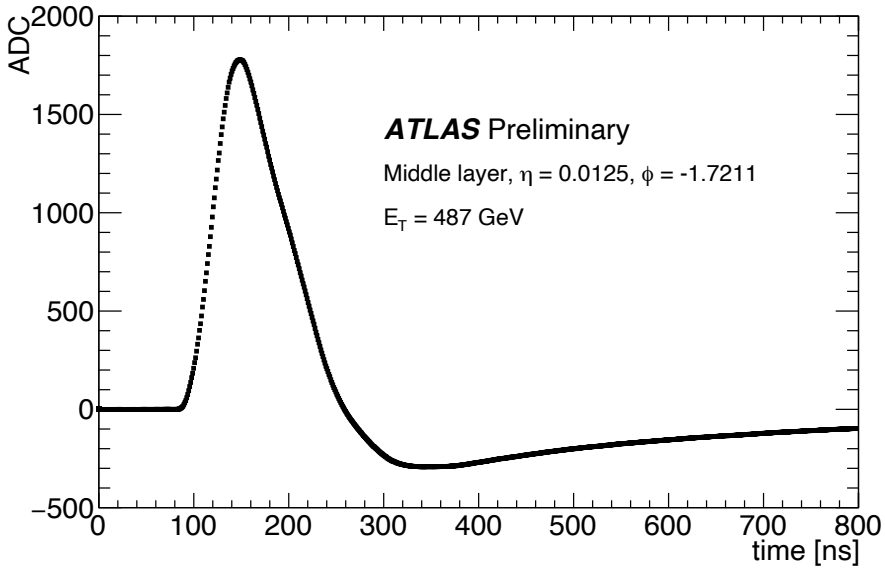


Validation and commissioning (2)

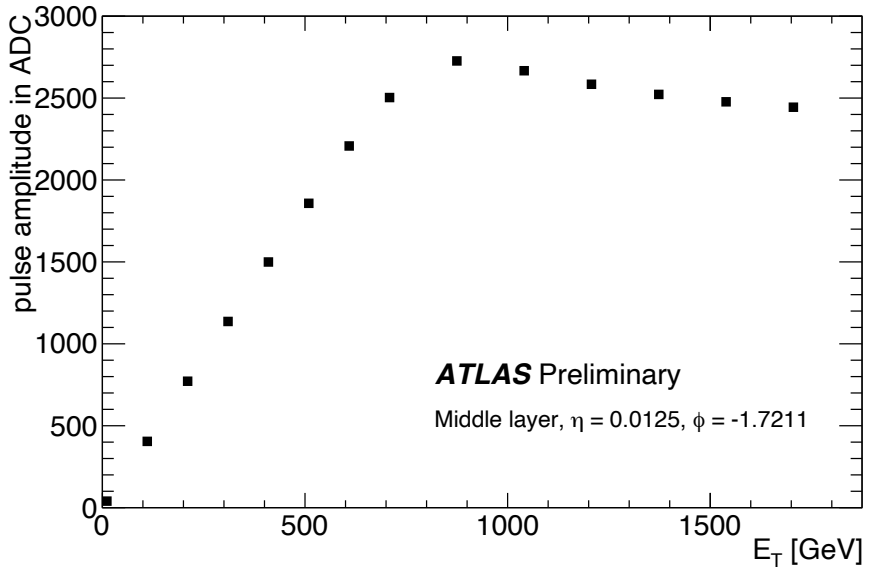
Digital trigger readout

- Energy and timing of SCs should be similar to legacy TTs
  - Linearity valid up to ∼700 GeV for all SCs, much higher than previous TTs (250 GeV)
- Channel pulsing scans to verify SC mapping

Pulse recorded with new Digital trigger



Amplitude pulse vs injected calibration signal



Energy computed with LATOME

- Online and Offline algorithm should gave similar results
  - Differences below 1%
  - Automatic processing in place

Conclusions

LAr Digital trigger installation almost finalized despite the pandemic

- Front end close to be fully installed: all baseplanes, LSB, and FEBs refurbished, $> 80\%$ LTDBs installed
  - Expect to install remaining LTDBs by the end of $\sim$July
- Back end fully installed, with monitoring system too
  - Additional fibers routing to the back end to be performed as well

Validation and commissioning progressing very well

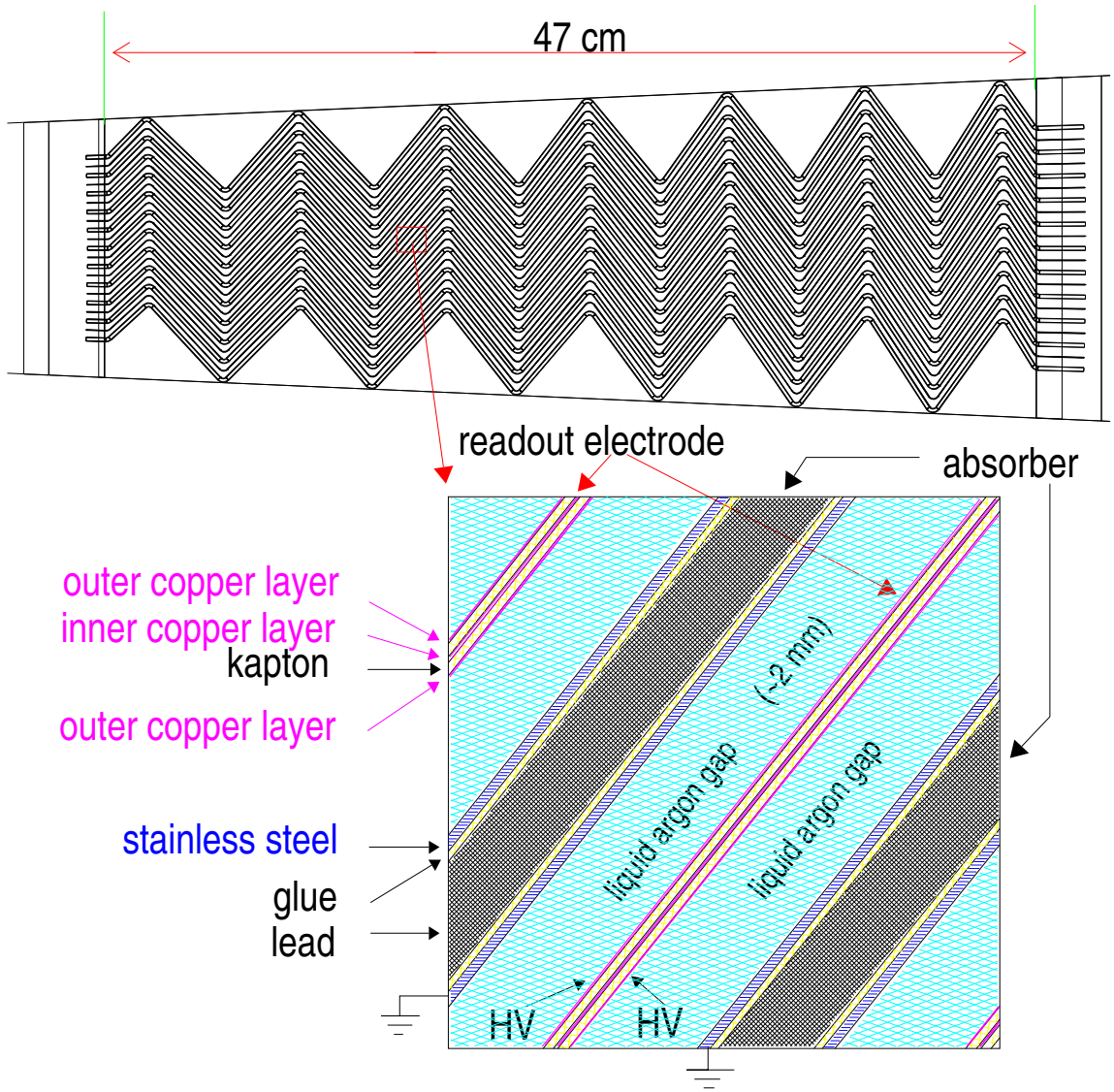
- Main readout path is validated
- Already applied corrections to synchronize legacy and new systems
- Continuously improving stability and robustness
- Expect to keep providing excellent performance during Run-3

On track to have a fully operational readout and digital trigger by the Pilot Run in October and for Run3, thanks to a devoted and overachieving group of scientists!

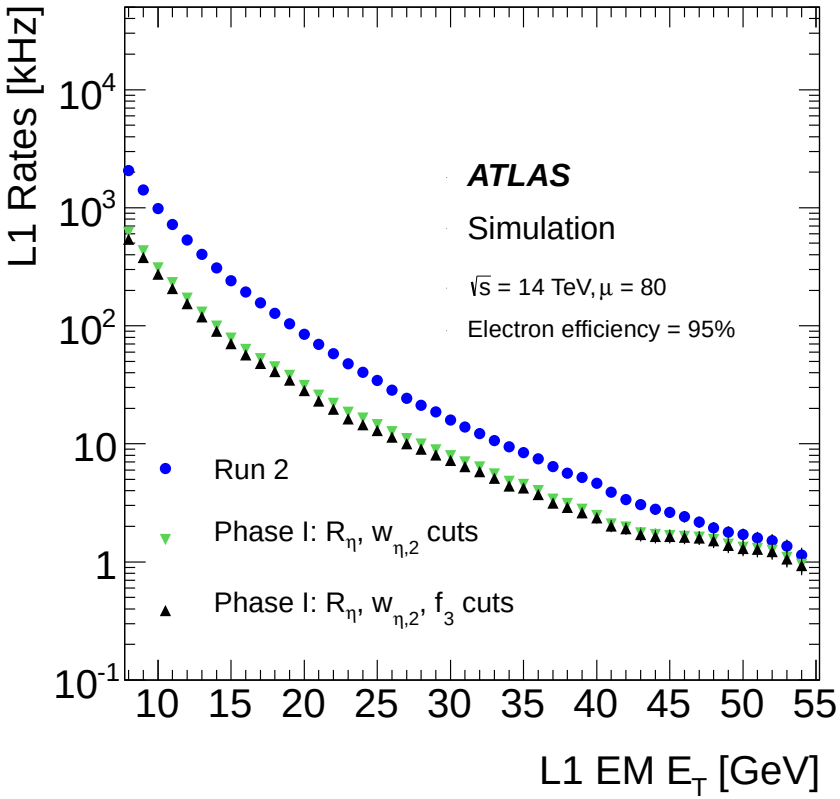
BACKUP

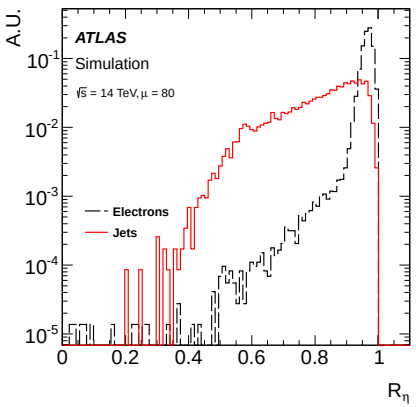
Physic signlas from LAr cells

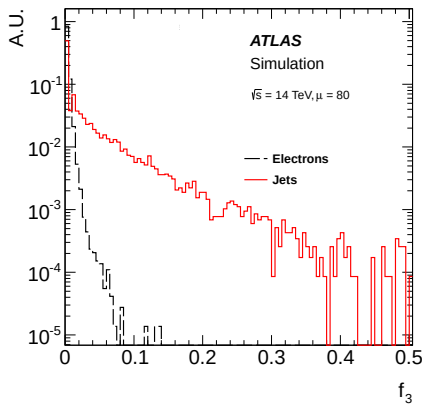
- 2.1 mm gap with ∼2 kV applied
- Particles interact with the absorber creating secondary particles ⇒ shower
- Secondary particles ionize LAr ⇒ collected by electrodes, drift time ∼450 ns,
- Current is read out, amplified and shaped (CR-RC^2)
- Signal then sampled and stored in analogue memory on the Front End waiting for L1 trigger decision



Phase I physics motivation



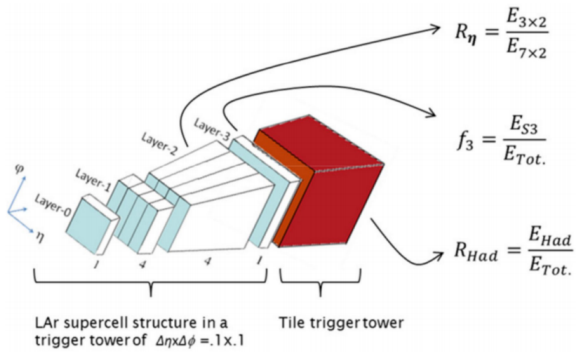




Use shower information as done in offline analysis to improve background rejection

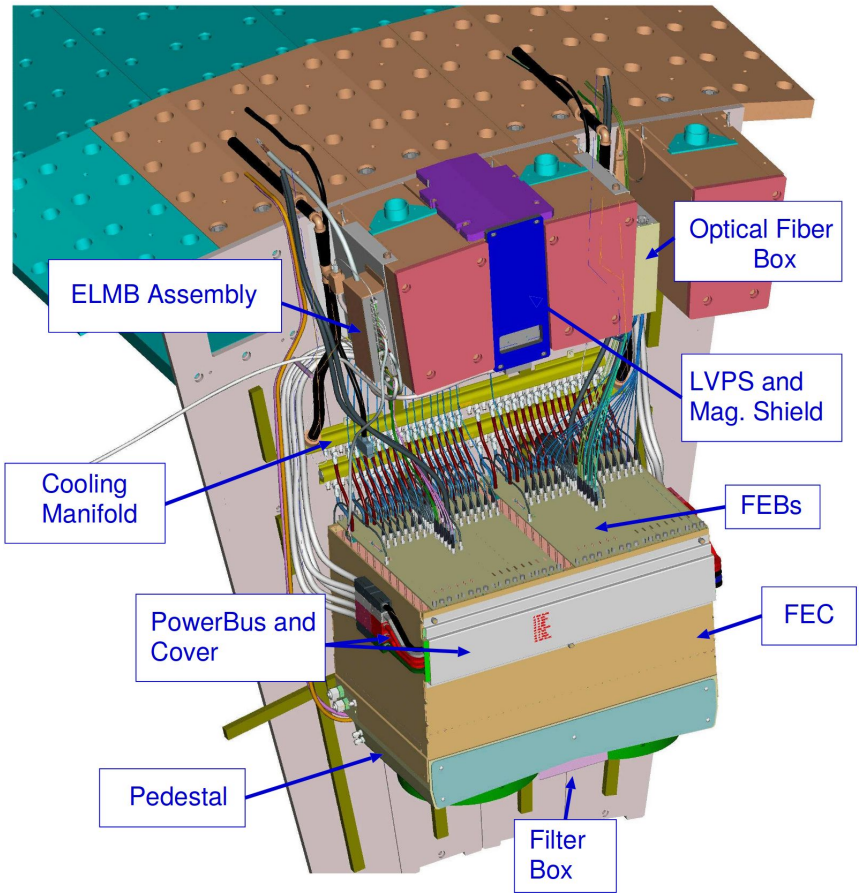
Example 95% efficiency on electrons from $Z \rightarrow ee$ events with Run3 conditions

- assuming Run2 trigger algorithms: to have L1 rate 20 kHz need $E_T = 28.5$ GeV threshold
- Using shower shapes from SCs, lower to $E_T = 21$ GeV threshold



Moreover, improved L1 EM resolution $\Rightarrow$ substantially sharpen the trigger turn-on curves $\Rightarrow$ reduction offline E_T threshold and increase acceptance

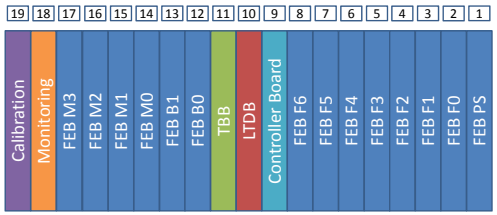
Front End Crates



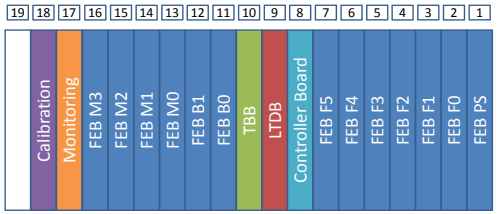
Front End crates contains most of the FE electronics for readout and trigger

- 1524 Front End Boards, each reading 128 channels
- Calibration boards
- Trigger Builder Boards (for TT building)
- From now on also LTDBs

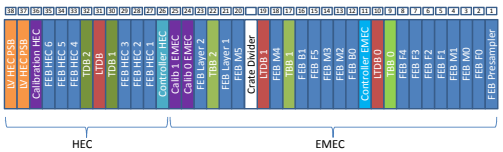
EMB



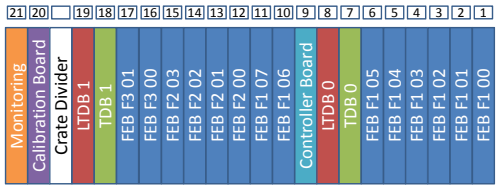
EMEC



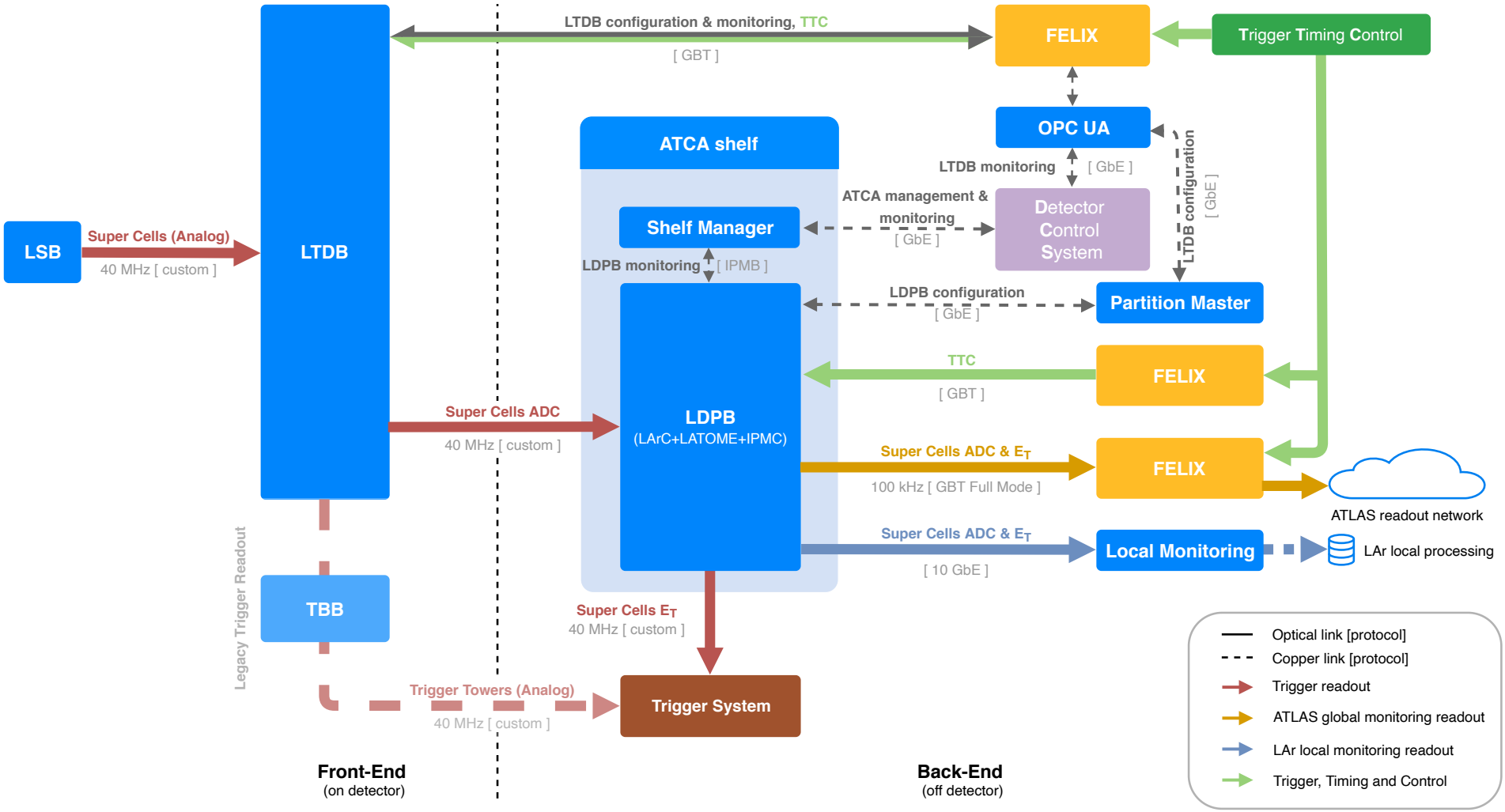
HEC and EMEC Special



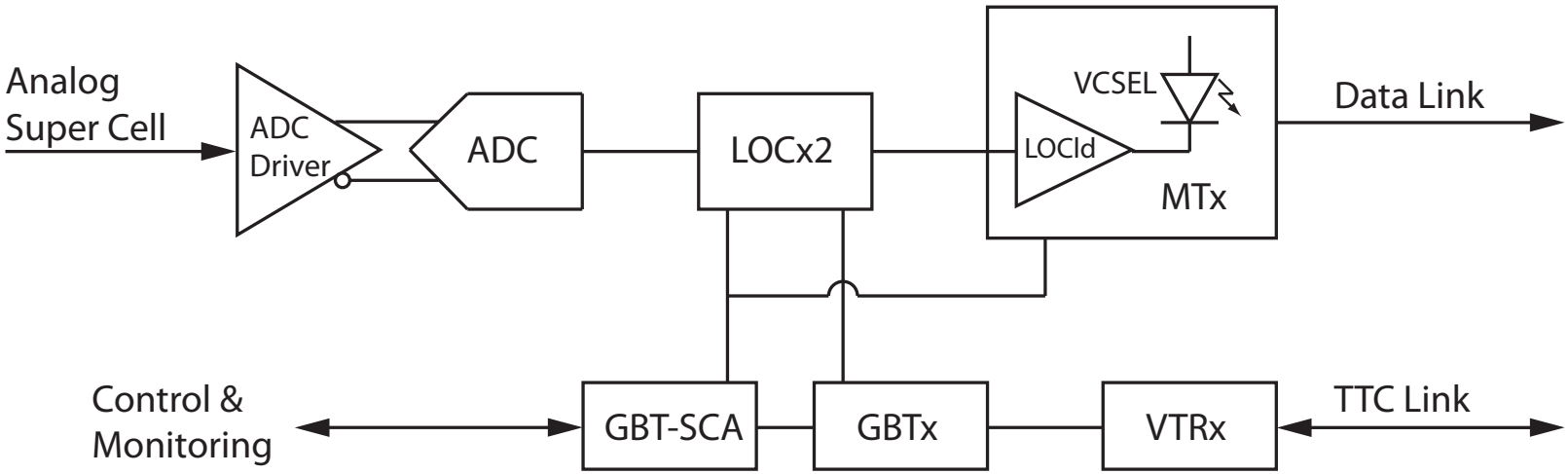
FCal



Digital trigger integration



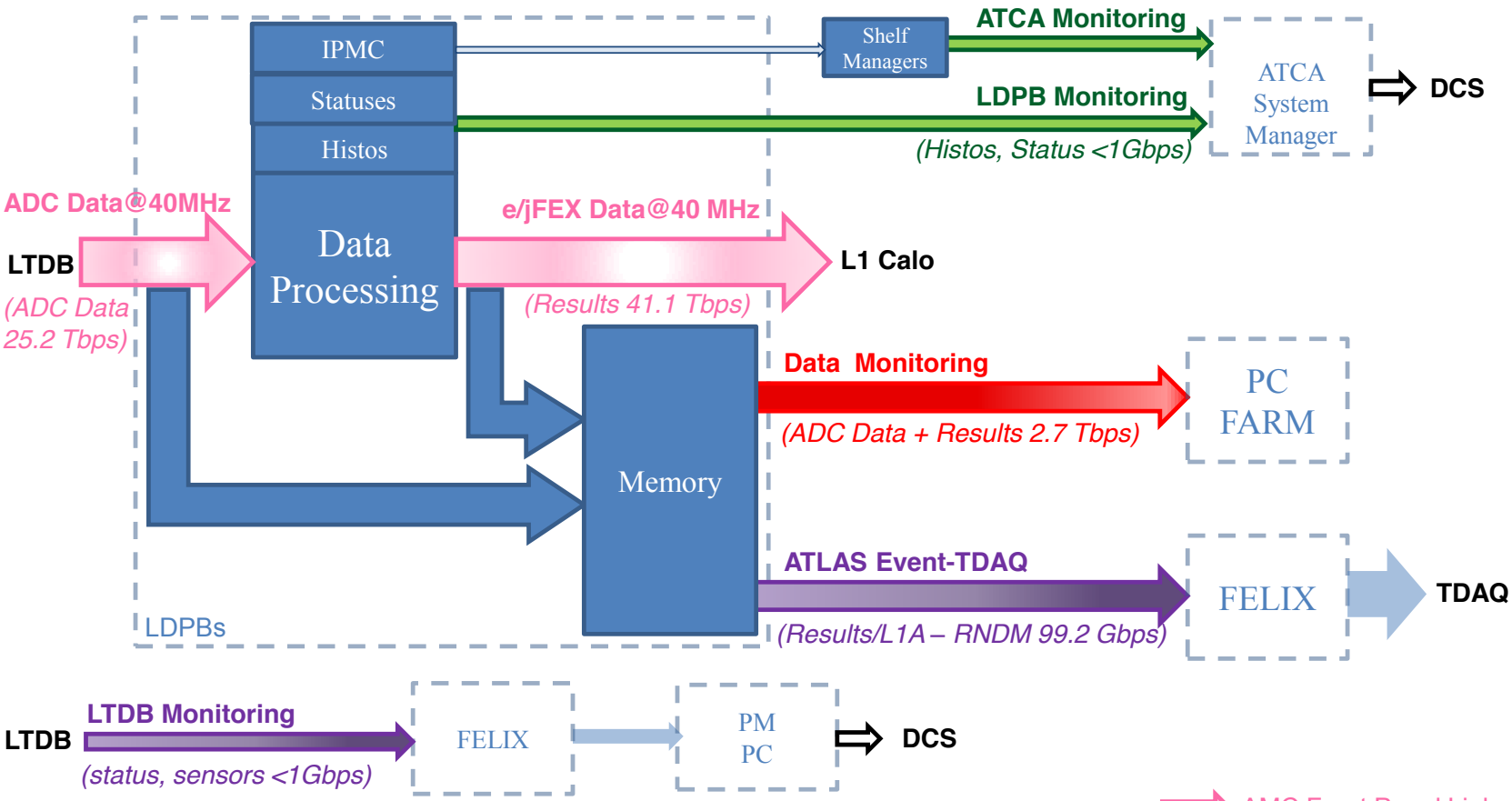
Signal paths in LTDB



LTDB digital section includes two signal flow paths: the data link and the control (TTC) link.

- data link: SC signals are digitized by the ADC, reorganized and serialized by LOCx2, and transmitted via the MTx over fiber optical links
- control link: the TTC link is responsible for clock distribution, slow control and monitoring; it is composed of the GBTx, GBT-SCA and VTRx
  - GBTx interfaces to the back end of the TTC system via VTRx over duplex fiber optical
  - GBTx and GBT-SCA chipset is used to provide clock distribution, slow control and monitoring on the LTDB.

Data flows



LTDB: 124 Modules LDPB: 31 Blades

Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps