ATLAS towards the High Luminosity era: challenges on electronic systems

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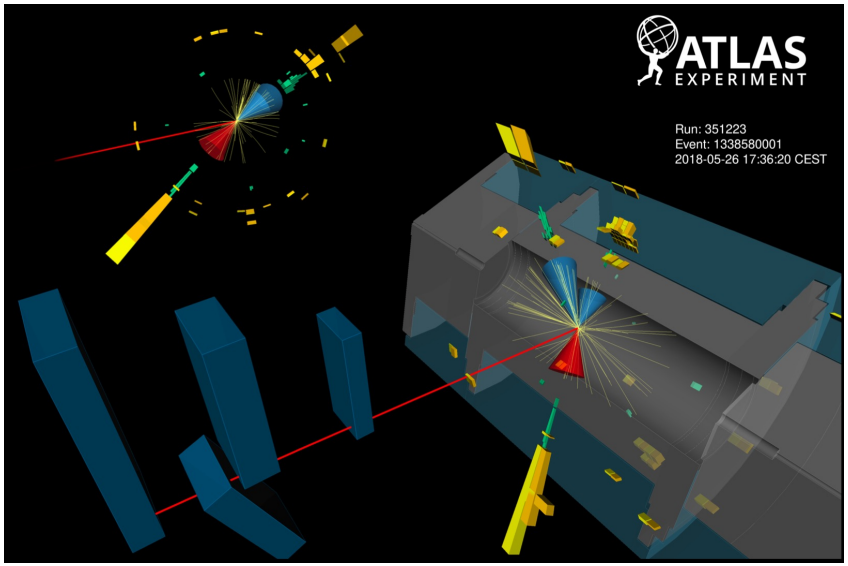
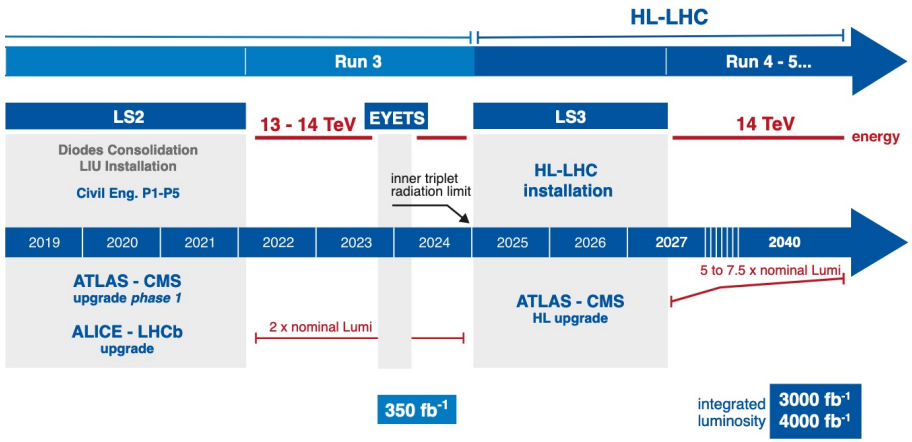
on behalf of ATLAS Collaboration

Motivation for High Luminosity LHC

- Fully exploit the physics potential of the LHC
  - Precision measurements of Higgs Boson and SM properties (couplings, top mass, cross sections)
  - Searches for BSM signatures (SUSY, resonances, dark matter)
  - Increase the coverage for rare physics events
- HL-LHC design parameters
  - Deliver up to 4000 fb^{-1} at center of mass energy of 14 TeV
  - Peak instantaneous luminosity of 7.5 x 10^{34} cm^{-2} s^{-1}

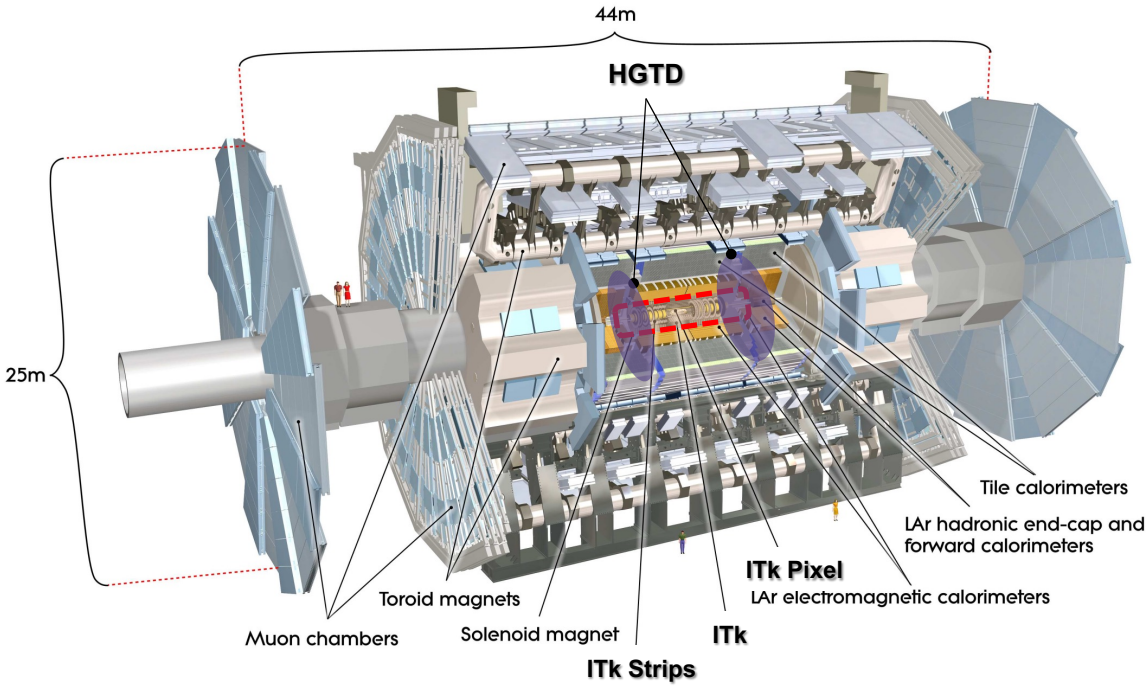


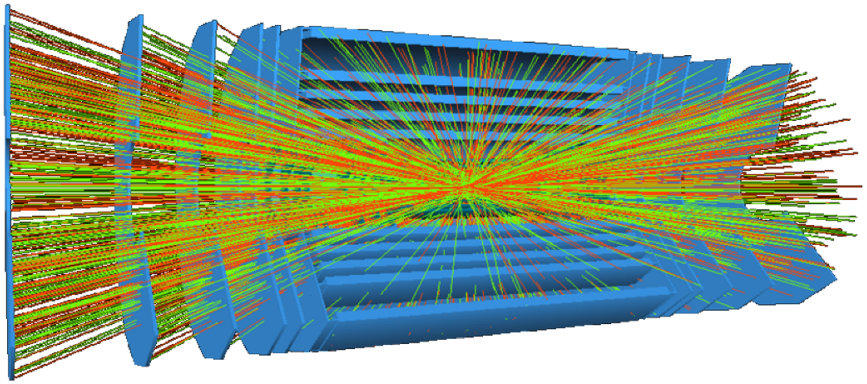
Non-resonant di-Higgs H(bb)H(ττ) candidate event



ATLAS experiment for HL-LHC

- Upgrade in two Phases
  - New Small Wheels, BIS78 and LAR trigger for Phase-I
- Phase-II upgrade
  - New all-silicon Inner Tracker (ITk) up to |η|<4
  - New High-Granularity Timing Detector in end-cap region
  - New muon chambers in inner barrel region
  - Data streaming at 40 MHz for calorimeter and muon systems to off-detector readout and trigger electronics
  - New hardware triggers (L0)
- Challenges
  - New hardware L0 trigger
  - Radiation hardness against single-event-effects
  - Shortages in silicon wafers

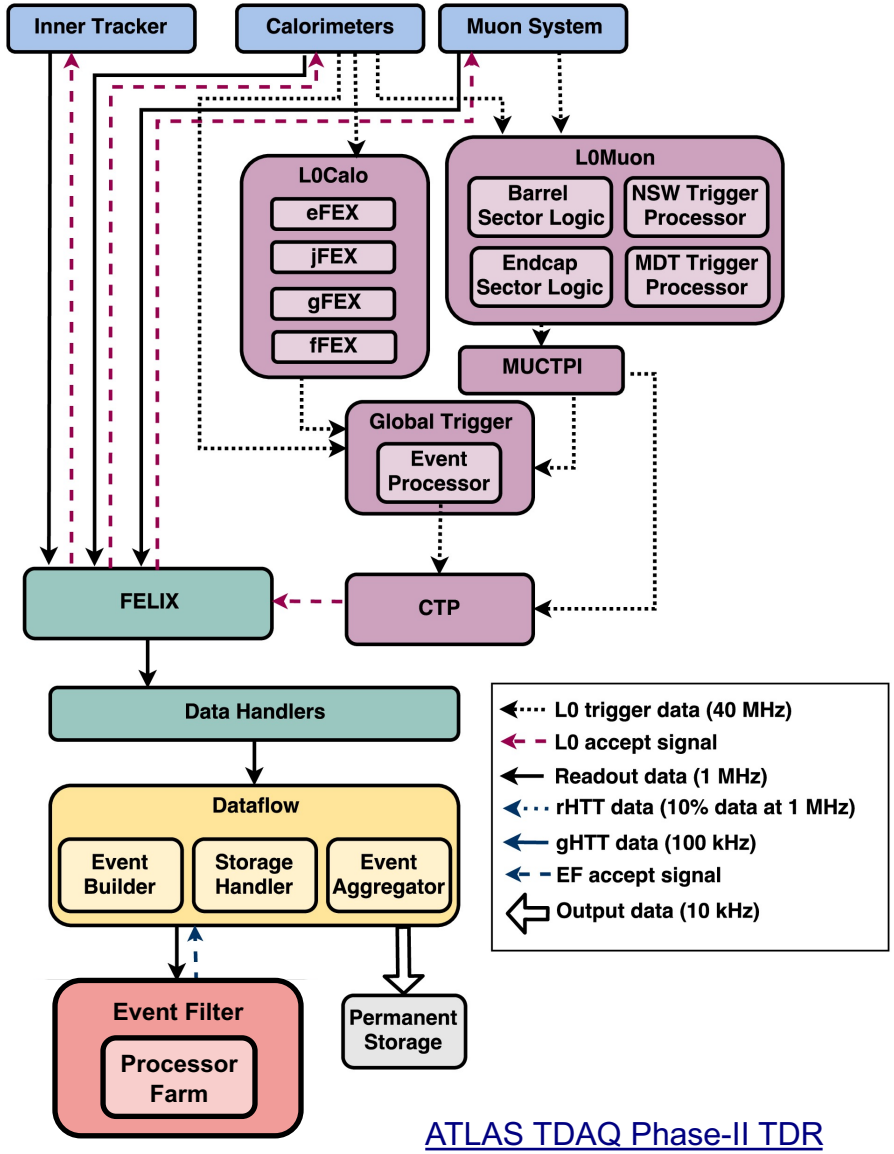




HL-LHC event 140-200 pile-up events

Phase-II Trigger architecture

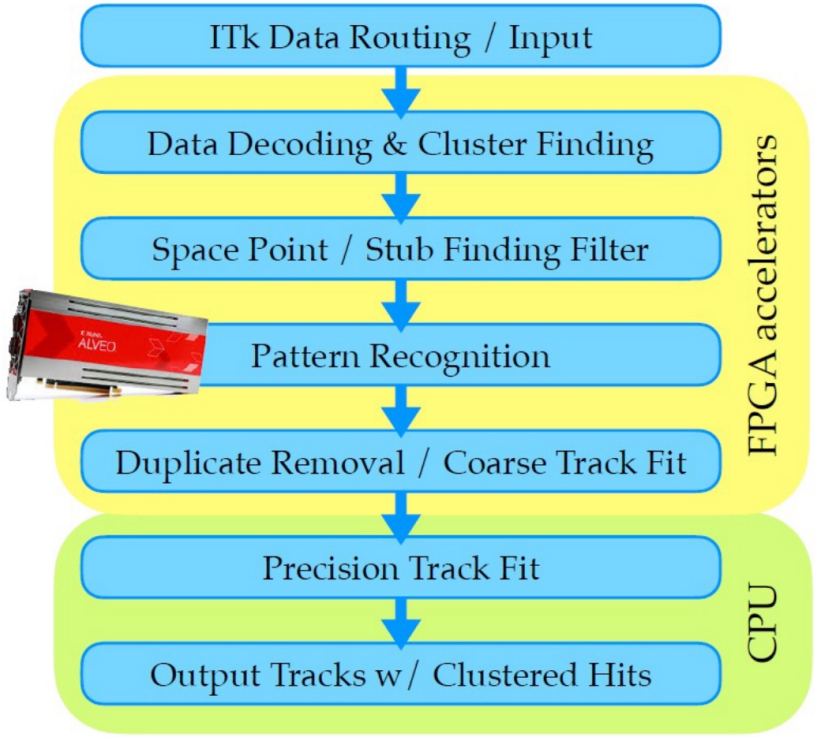
- ATLAS Phase-II Trigger system will be L0-only
  - Hardware based Trigger at 40 MHz
  - Feature extractors for calorimeter and muon systems combined at Global Trigger with improved acceptance and momentum resolution
- Full FELIX read-out after LS3
  - Up to 3.5 MB events (2MB in Run2)
  - 290 GB/s throughput (50 GB/s in Run2)
  - 3.2 GB/s recording (1.5 GB/s Run2)
- Event Filter Trigger
  - Provide high-level Trigger functionality using algorithms close to offline reconstruction and tracking methods



ATLAS TDAQ Phase-II TDR

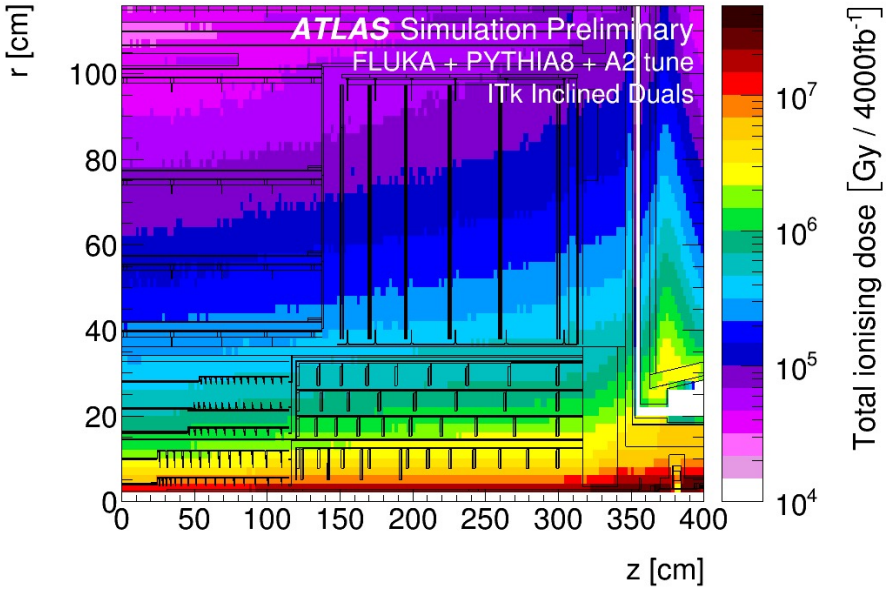
Event Filter Trigger

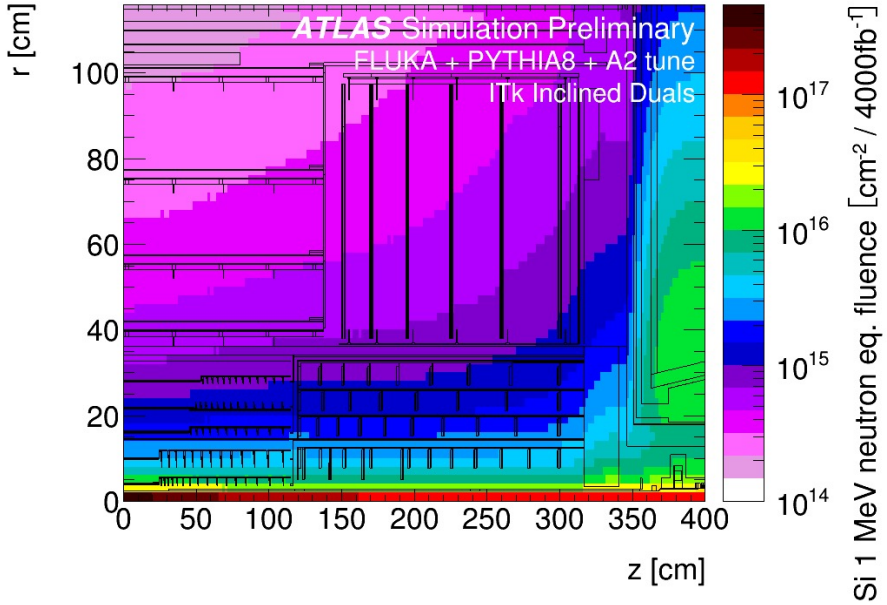
- Options for Event Filter Trigger
  - Custom Associative Memory
  - Commodity based: accelerators
  - Commodity based: software only
  - Full software design
- Recommendation to commit to a software solution
  - Strongest candidate except for power and cooling
  - No real advantage to custom solution
  - Less risk and smaller short-term investment
  - Keep options open for heterogenous solutions (FPGA accelerators)



Example of commodity-based solution for track reconstruction at the Event Filter Trigger

Radiation maps at 4000 fb^{-1}

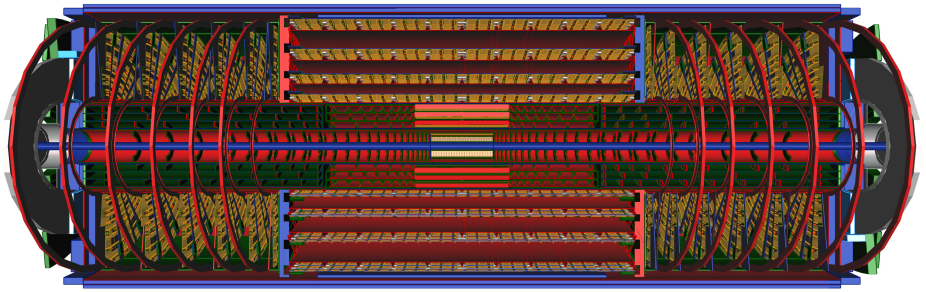




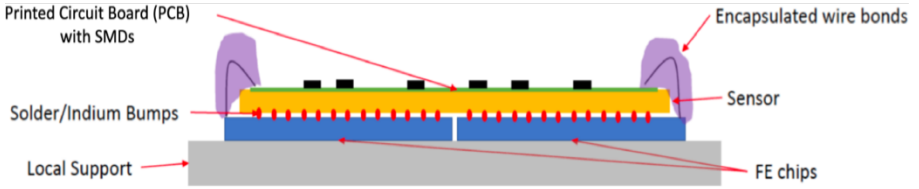
- TID > 10 MGy and 10^{16} 1 MeV n/cm^2 fluence in ITk inner system
  - Up to 1 MGy TID and 10^{15} 1 MeV n/cm^2 fluence in the outer layers
  - Use radiation tolerant ASIC designs and optimized services
- TID ~ 100 Gy and 10^{14} 1 MeV n/cm^2 in the outer layers of the detector
  - Allow use of flexible FPGA designs and single-point-failure-free engineering
- Require qualification against TID (surface effects, transistor damage) and SEE (single event upsets, latch-up events)

ITk

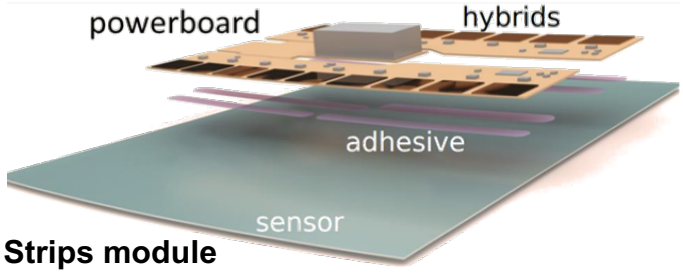
- All silicon tracker to replace the current ATLAS inner detector
  - Extreme radiation tolerance, high granularity and low material budget
  - Tracking coverage up to $|\eta|<4$
  - Up to 1 MHz L0 Trigger rate
- 5 layers of hybrid Pixel detector
  - 3D-sensors in innermost layer, planar sensors in other layers
  - Pixel size 100x25 μm^2 (innermost barrel), 50x50 μm^2 (all other layers)
  - Data output 4x1.28 Gbps / module
- 4 layers of Strip detectors
  - 8 sensor types (2 barrel, 6 endcap)
  - Strips size: 2 - 5 cm
  - Data output 4x640 Mbps / module



ITk Layout – ATL-PHYS-PUB-2021-024



ITk Pixel module



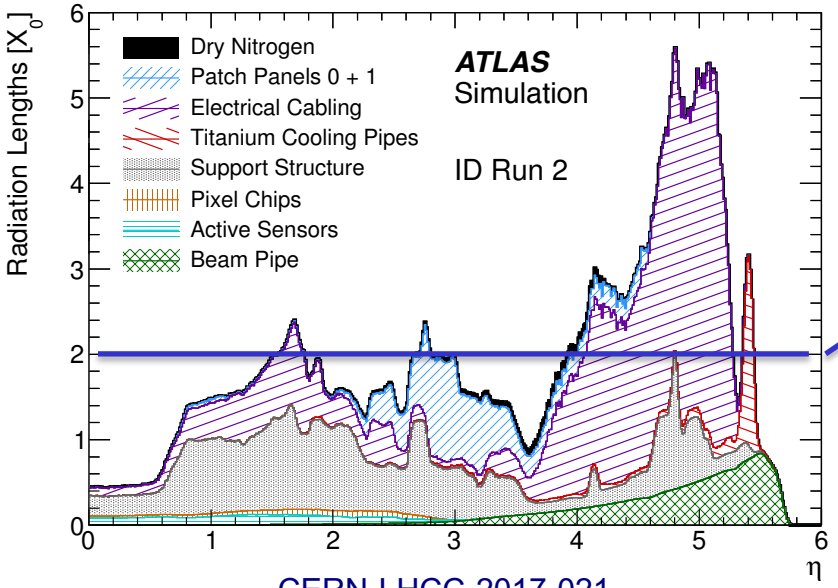
ITk Strips module

	Surface [m^2]	# Channels	# modules
Pixel	13	5.1 G	9.2 k
Strip	165	60 M	18 k

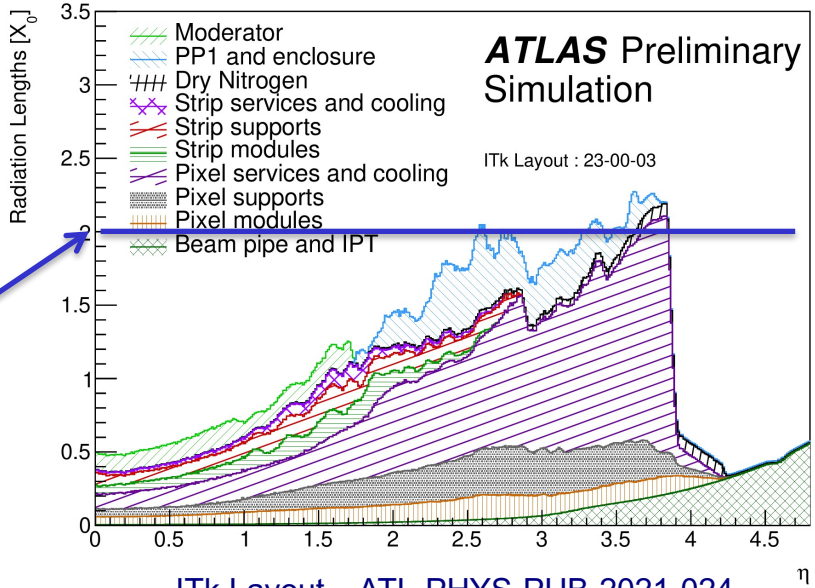
ITK Pixel TDR ATLAS-TDR-030

Material budget in ITk

- Reduction of material budget as much as possible
  - More than factor 2 in forward region vs current ID in Run 2
  - Usage of optical links and point of load regulators in Strips
  - Thinned sensors, serial powering, 10 Gbps read-out links in Pixels
  - Light structures, capillary cooling distribution, and rad-hard monitoring
- Material budget will still evolve with engineering design



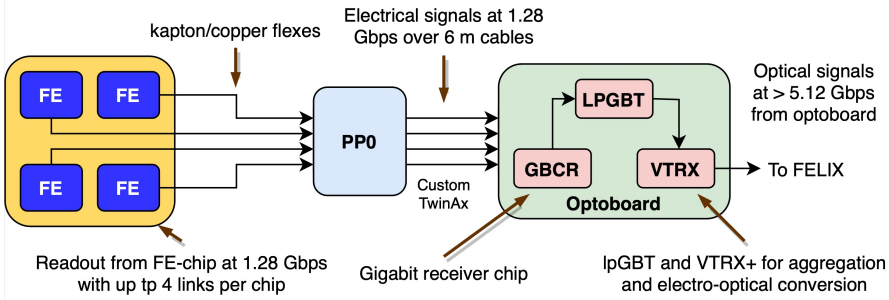
CERN-LHCC-2017-021



ITk Layout – ATL-PHYS-PUB-2021-024

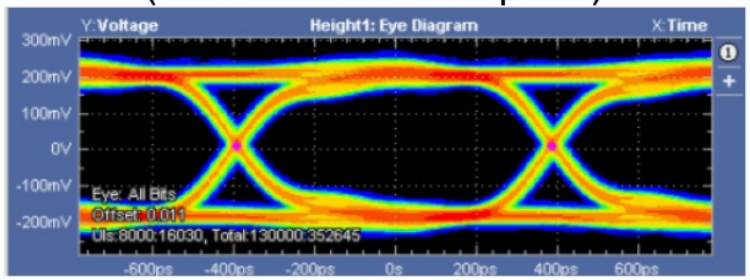
Data transmission

- Optical transceivers are so sensitive to single-event-effects that we cannot place them inside the ITk detector volume
  - Expect 1 SEU per day per VTRX+ outside the detector volume mitigated by continuous monitoring
- Use CERN wide low power Gigabit Transceiver (lpGBT) for optical transmission
  - Still require electrical transmission at 1.28 Gbps over 6m of custom twisted pairs
  - Custom Gigabit Receiver Chip (GBCR) recovers the signal for lpGBT
  - Measurement of peak-to-peak eye opening of 94 ps at the output of the GBCR



ITk pixel on-detector data transmission chain

GBCRv2 equaliser + retiming
(1.28GHz EClk0 from lpGBT)

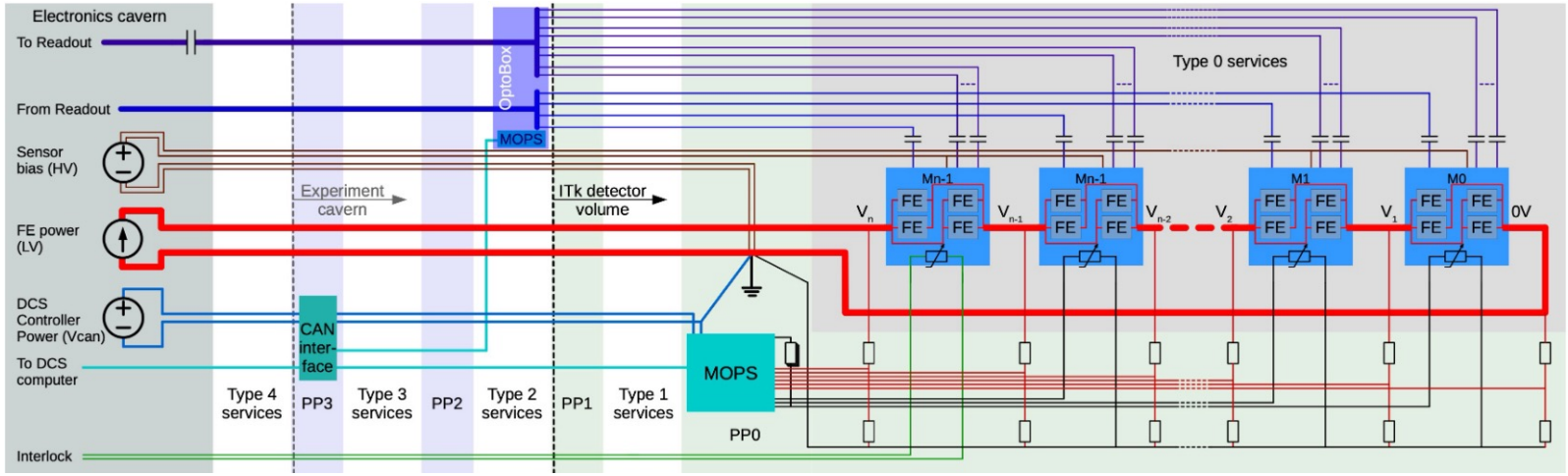


TIE p-p: **94 ps**

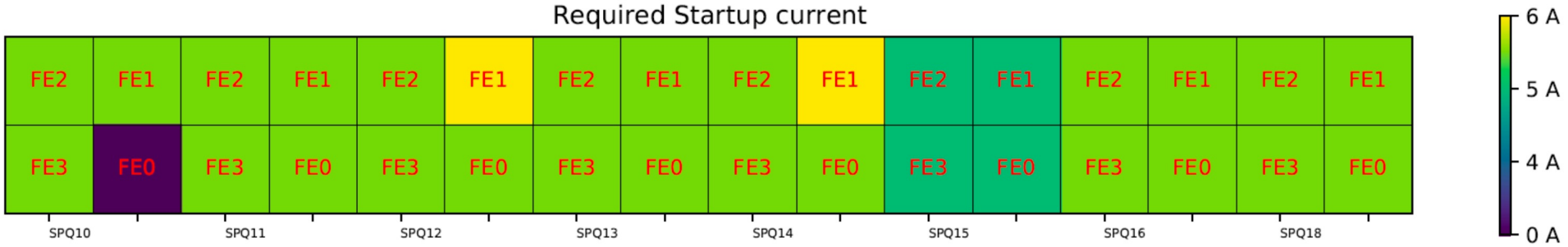
Jitter source:

* lpGBT output clock jitter
* GBCR v2 retiming

Serial powering

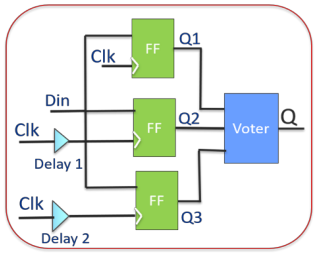


- ITk Pixel modules are connected in series by a constant current source
  - 912 serial powering chains with 3 to 14 modules are monitored by dedicated chip
  - All module front-ends powered in parallel and regulated by 2 shunt LDOs (analog, digital)
- Ongoing tests with RD53A to measure the minimum current required to power up
  - Up to 6 A necessary in some cases
  - Next step to test with ITKPIXV1.1 as they become available

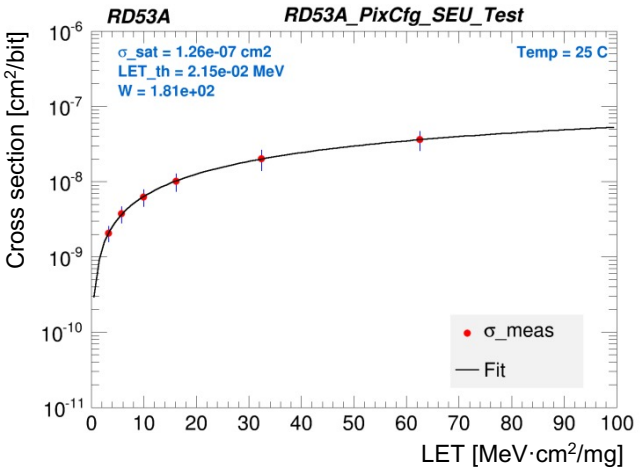


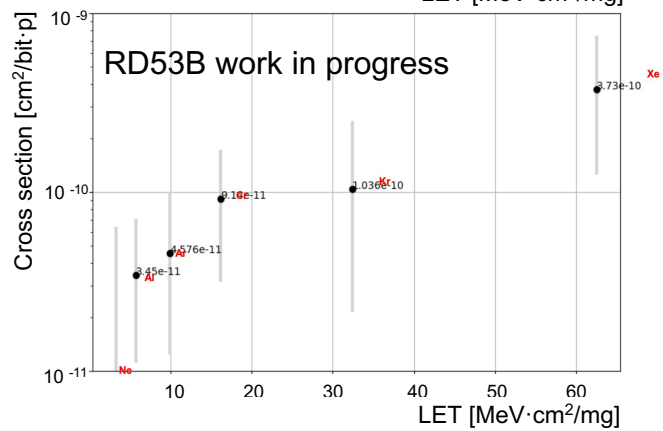
SEE mitigation in ITK Pixel (RD53)

- Results with RD53A (read-out ASIC)
  - Limited fluence 2x10^5 p/cm^2 due to comm. errors
  - Tested the pixel registers ~1Mbit
  - Saturation cross section 1.26 10^{-7} cm^2
- RD53B implements TMR in TSMC 65nm
  - Data to 3 different flip flops is delayed
  - Status voted from the majority
  - Including temporal delay for global registers
  - Implemented by synthesis in digital flow
  - Requires 40% more space
- Results with RD53B – ATLAS ITKPixV1
  - No SEL observed
  - SEU σ = 2-6 x 10^{-15} cm^2 for single latch
  - SEU σ = 2-7 x 10^{-17} cm^2 for global registers
- Continuous reconfiguration needed
  - Considering a rate of 500 MHz/cm^2 of particles above upset threshold
  - Upset rate 2 x 10^{-5} Hz
  - 1% pixels corrupted every 500 s
- Submission of ITKPixV2 planned for Feb 2022



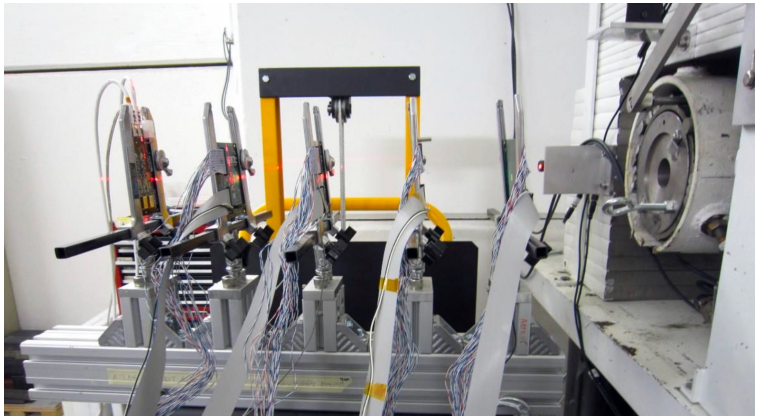
Triple Module Redundancy with temporal delay



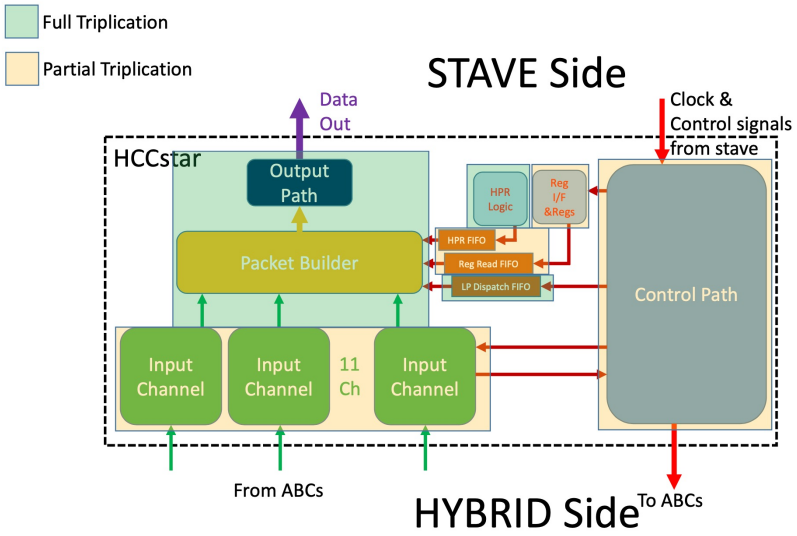


SEE mitigation in ITK Strips

- Tests with ABCStar (binary chip)
  - 480 MeV protons at TRIUMF
  - Heavy ions at Louvain
  - Recommended HCCStar re-design
- HCCStar (readout ASIC) re-design
  - Removed regional readout features
  - Replaced asynchronous resets by synchronous ones
  - Fully triplicated logic, packet builder, and output path with TMRG tool
  - Partially triplicated control path, input channels, and registers
  - Functional simulations show good recovery in non-TMR logic
- Similar re-design for AMACStar (monitoring and interlock ASIC)



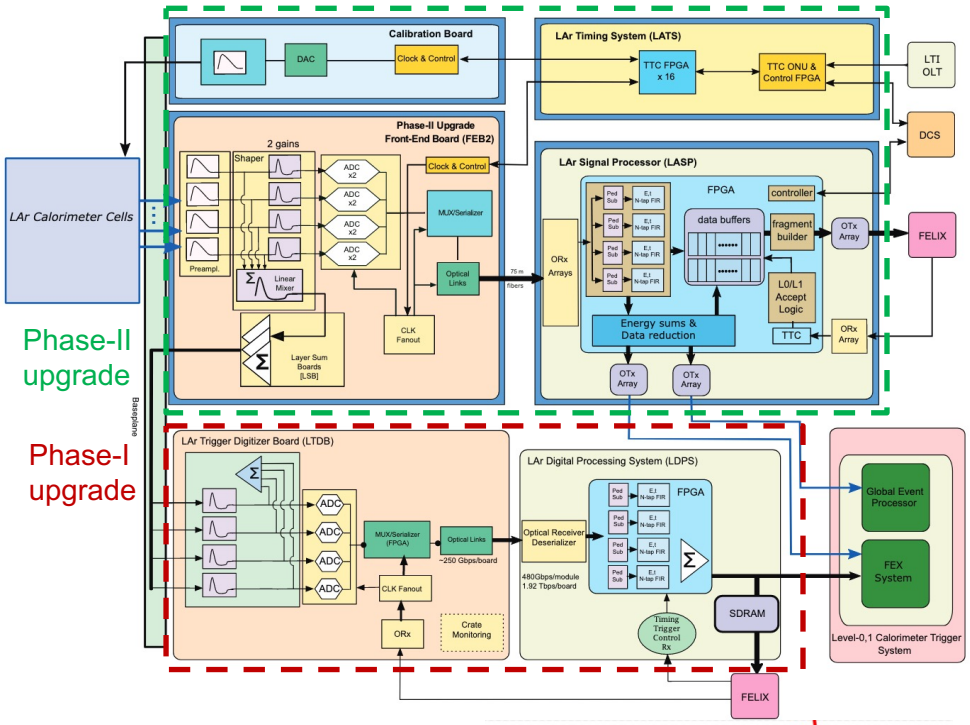
ABCStar measurement campaign at TRIUMF



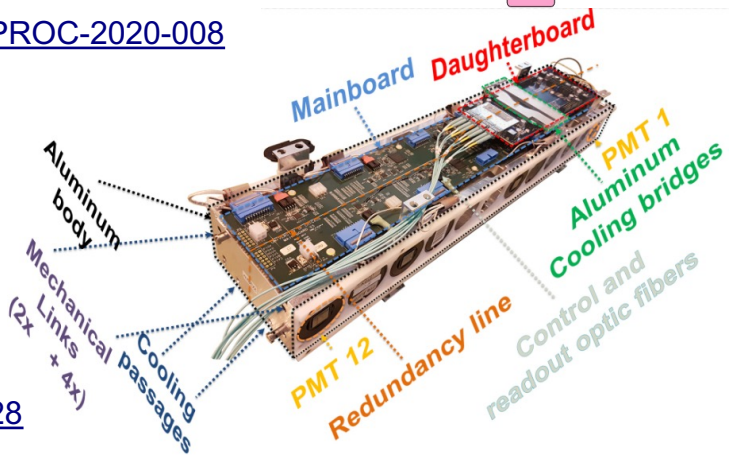
Block diagram of HCCStar

Calorimeters

- New readout electronics sampling at bunch crossing rate (40 MHz)
- LAR calorimeter Phase-I
  - Higher energy resolution and more longitudinal information for Trigger
- LAR Phase-II
  - Replace front-end boards (FEB2)
  - Design 2 ASICs in CMOS 130 nm
  - Full custom 14-bit ADC with SAR architecture in 65 nm CMOS
  - Calib ASIC in HV-CMOS 180 nm
- Tile calorimeter
  - Modular front-end mini-drawers
  - Improved front-end linearity
  - Complete redundancy from the cell to the off-detector electronics
  - Combine TMR design with Xilinx Soft Error Mitigation core



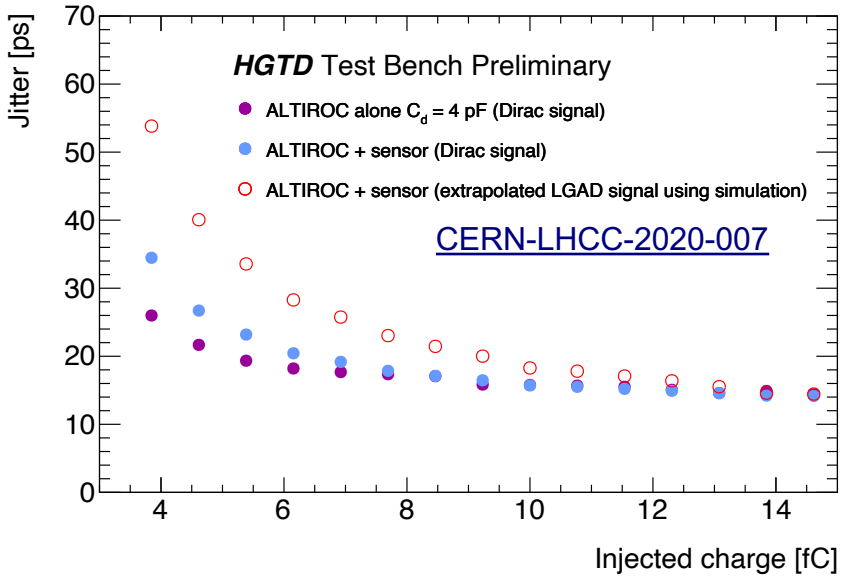
ATL-LARG-PROC-2020-008

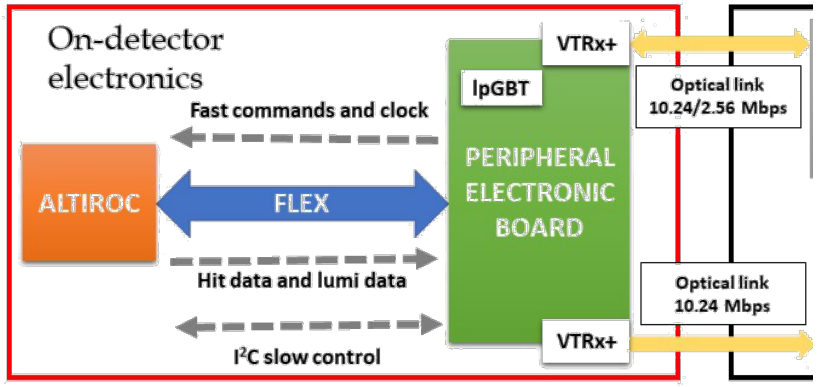


ATL-TDR-028

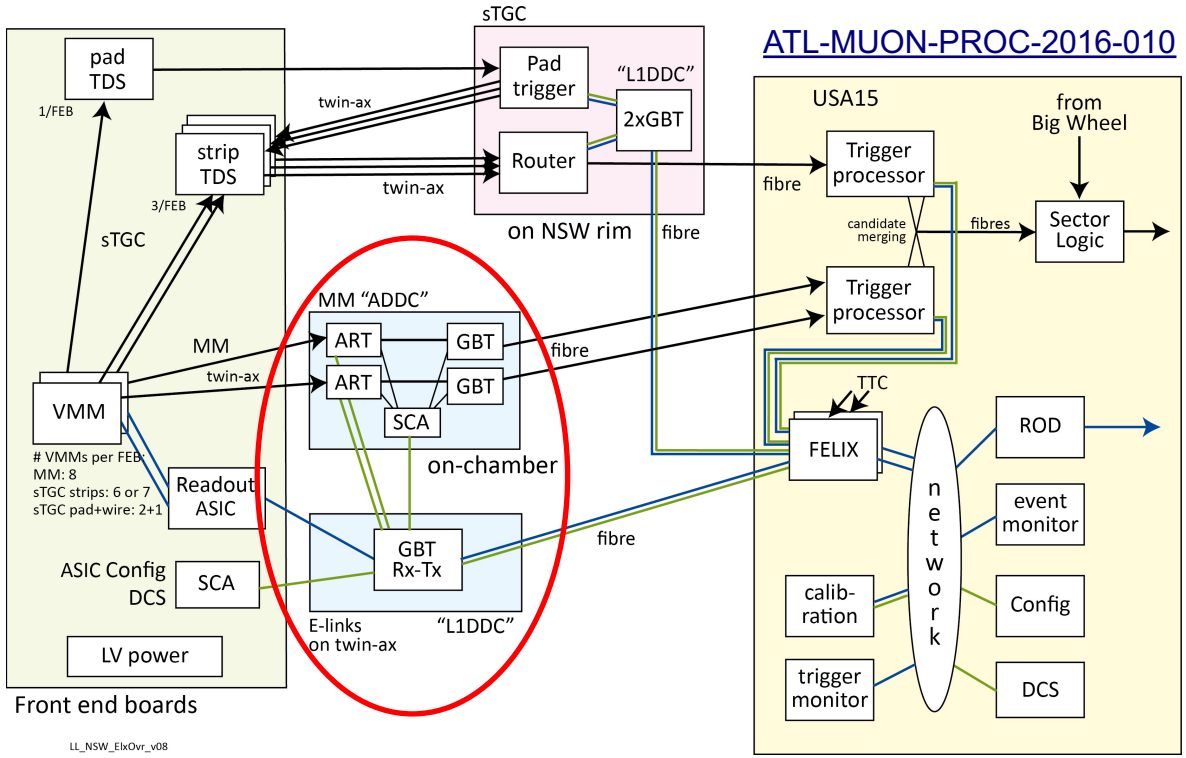
High granularity timing detector

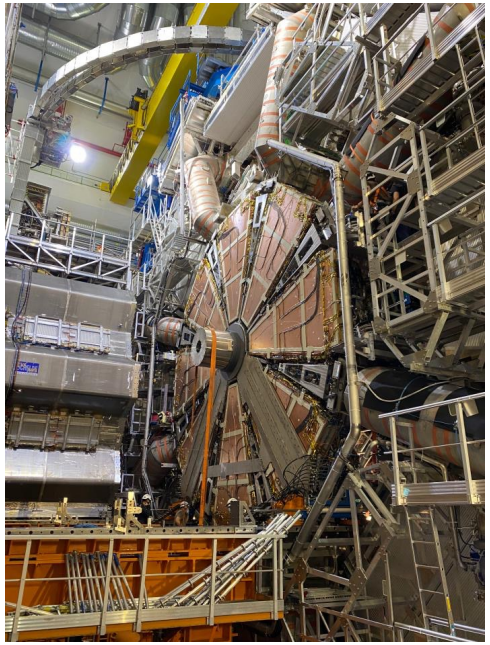
- LGADs in rad-hard environment
  - R&D from ATLAS/CMS/RD50
  - Arrays of 15x15 1.3mm^2 sensors
  - 2 sensors + 2 ALTIROCs per module
  - Contribute to luminosity measurement with dedicated path
- ALTIROC2 (front-end chip)
  - Submitted in TSMC 130 nm
  - Full-sized boards expected this year
  - Expected jitter < 20 ps above 10 fC
  - Rad-hard up to 1.5 MGy TID and 2.5 x 10^{15} n/cm2 NIEL
  - To be evaluated this year and might need mitigation strategies





New Small Wheel





NSW-A installed in ATLAS

- New MicroMegas and sTGC chambers installed during LS2
  - Using FEAST DC-DC rad-hard to 200 MRad TID and $5x10^{14}$ n/cm2 NIEL
  - Using GBTx 130 nm CMOS chips for continuous read-out through FELIX
- Require configuration of secondary GBTX chips through SCA/DCS
  - More data links than command links → increased risk of single point failure

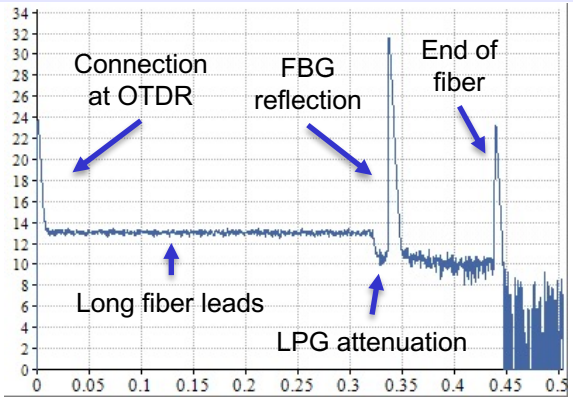
Conclusions

- The Trigger and DAQ challenge
  - 1 MHz Hardware Trigger decision, detector readout and HLT processing
  - ATLAS decision to focus on L0 only trigger for Phase-II upgrade
  - Plan to use commodity solution in High Level Trigger
- Radiation hardness against Single-Event-Effects
  - Implementing robust enough designs against SEU and SEL
  - Specific to all ATLAS front-end ASIC including lpGBT
  - More relevant for ITk Pixel and Strip due to closeness to beam pipe
- The global semiconductor shortage
  - Affecting production schedule and delivery dates

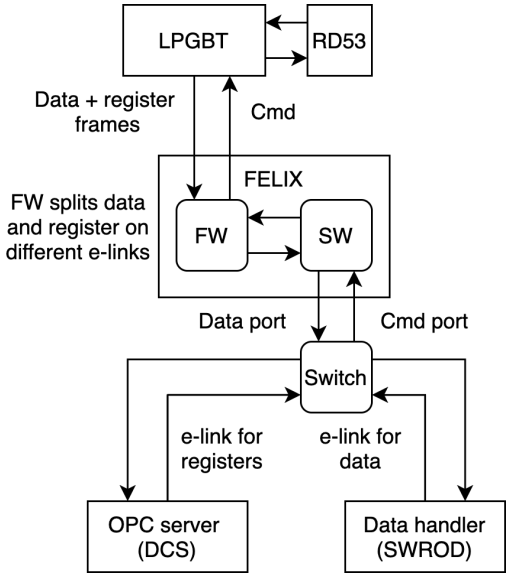
Bonus

Other challenges

- Measurement of humidity in high radiation and low temperature (-30 C) environment
  - Combine LPG (humidity) + FBG (temperature) fiber optic sensors
  - Proven radiation hard up to 2 MGy
  - Require humidity sensitivity ~0.5 %
  - Require distributed installation and testing
- Running the DCS through the DAQ FELIX
  - FELIX is the interface between custom front-end electronics and a commercial switched network
  - Data, monitoring, and detector control flow through the same FELIX link
  - LPGBT also configured through FELIX
  - Requires FELIX up while front-end is powered



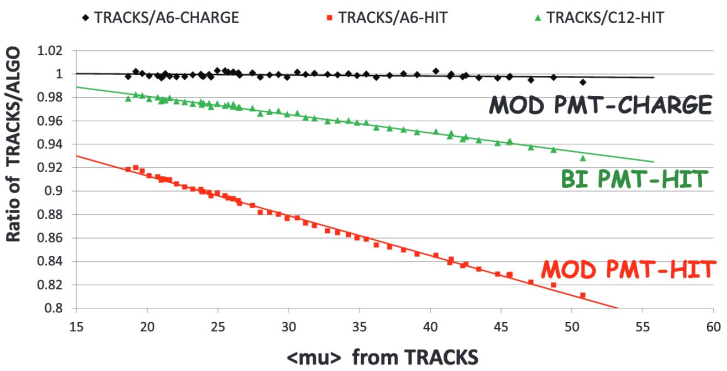
OTDR measurement of LPG + FBG fiber optic sensors

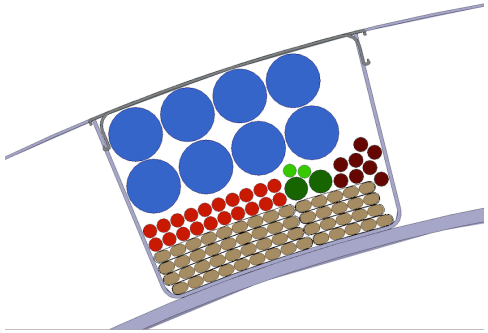


Possible implementation for DCS using FELIX

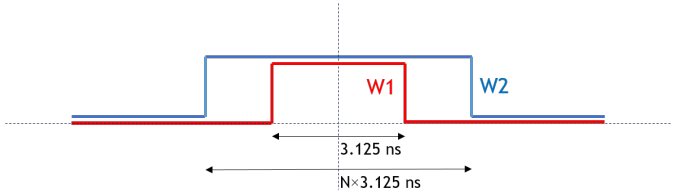
Luminometers

- Aim for redundant luminosity measurement
  - Three bunch-by-bunch detectors: LUCID-3, BCM', HGTD
  - Provide statistical sensitivity over 7 orders of magnitude
  - Measure outside stable beams
  - Calibration in van der Meer scans
- LUCID-3
  - Quartz fiber + PMT detector
  - Use hit counting + charge integrating algorithms
  - Affected by saturation, mu correction, gain changes, train dependence, beam crossing angle
- BCM'
  - Diamond sensor + semi-digital read-out
  - Requires low latency + radiation hard services
  - Services optimization to place VTRX+ in radiation compatible environment
- HGTD
  - Pixel cluster counting method in windows
  - ALTIROC processing of LGAD signals per bunch-crossing
- Other luminometers
  - Pixel Lumi Ring: Track, cluster counting
  - Tile gap/crack cells: anode currents
  - LAR electronics: pedestal evolution





Services for BCM' (green) in an already packed channel



HGTD time windows used for counting hits for luminosity