Electronic Integration and Commissioning of the New Small Wheel small-strip Thin Gap Chambers

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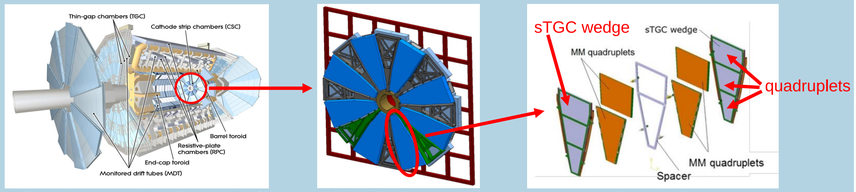
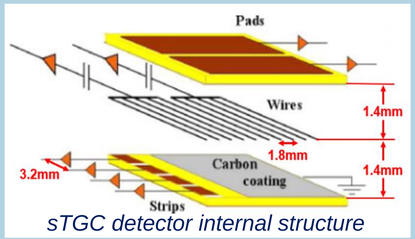
On behalf of the ATLAS Muon Collaboration

Introduction

ATLAS Detector | New Small Wheel | Sector



The Large Hadron Collider (LHC) is expected to reach an instantaneous luminosity of 5-7.5 x 10^{34}cm^{-2}s^{-1} for the future high-luminosity phase. To improve Level-1 muon trigger selectivity and maintain good muon tracking capability under high background rate and pile-up environment, the ATLAS experiment plans to replace the present innermost station of Muon Spectrometer in the forward region, Small Wheels, with the New Small Wheel (NSW) detector system during Phase-I upgrade, a major detector upgrade program to cope with the huge performance foreseen for the LHC machine. The NSW features two novel gaseous detector technologies, Micro Mesh Gaseous Structures (MM) and small-strip Thin Gap Chambers (sTGC). This detector system is expected to provide segment measurements with 1 mrad accuracy for Level-1 triggering as well as high precision offline tracking under background rate up to 20kHz/cm^2



sTGC detector internal structure

The sTGC and the MM can both provide complementary trigger and tracking information. Given its single bunch crossing identification ability, the sTGC will be used as the primary trigger detector. It has 3 types of readout channels, among which only pads and strips are used for Level-1 triggering.

The integration and commissioning of the sTGC detector is currently on-going at CERN. This presentation contains the status and progress on the sTGC electronics integration and commissioning, the experiences gained from the establishment of integration procedures and quality control. Performance and validation of the assembled detector system will also be presented.

Integration and commissioning workflow

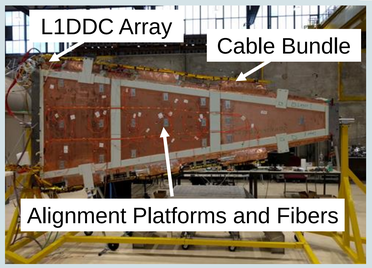
Assembly of quadruplets into wedge

Functionality test:
- Electronics reception test
- Wedge X-ray survey
- Gas leak test
- Long term high voltage test

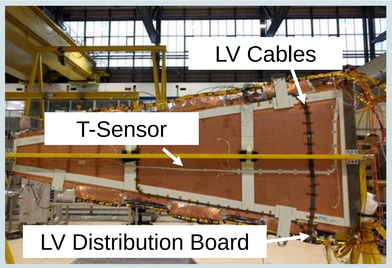
Mechanical integration:
- Electronics installation
- Cooling & gas pipe installation
- Alignment platform installation

Electronics commissioning:
- Channels baseline and noise assessment
- Readout test in L1 trigger matching mode
- Trigger interface validation

Adding all testing results into database



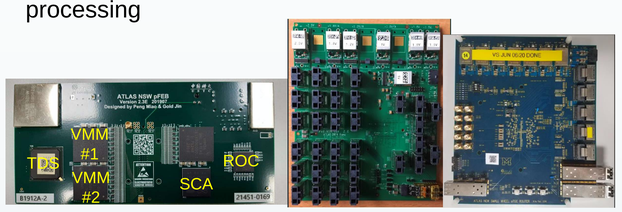
sTGC wedge electronics service side



sTGC wedge alignment side

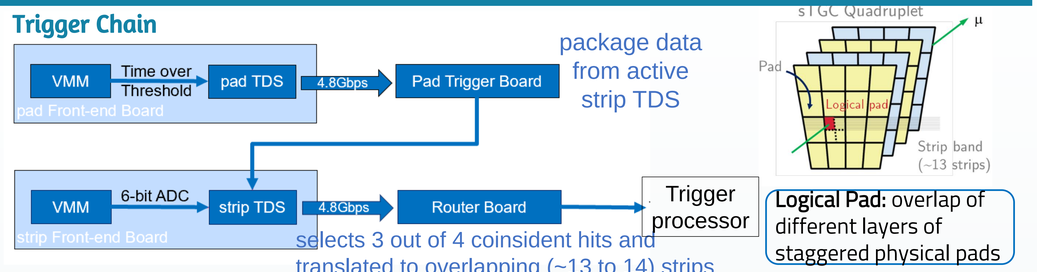
Electronics layout

The sTGC electronics system is designed to simultaneously handle a large volume of trigger and readout data from two separate data paths.
- ~350k readout channels
- >1.5k frontend boards
- ~14k custom-made radiation-tolerant Application Specific Integrated Circuits
- ~300 FPGA-based custom-made cards for trigger processing

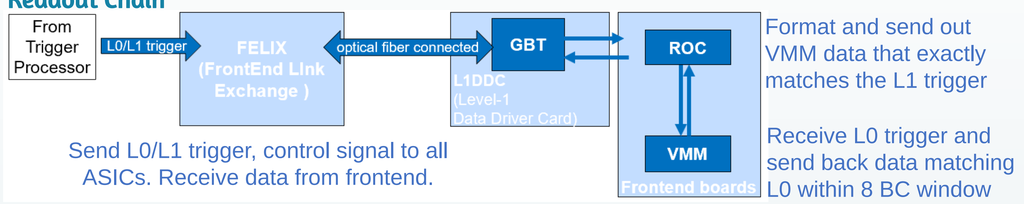


Frontend Board | *Pad Trigger Board* | *Router*

Trigger Chain



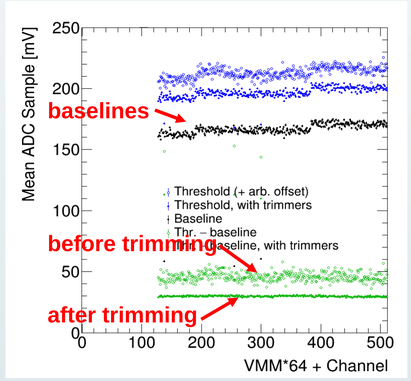
Readout Chain



Electronics test and validation

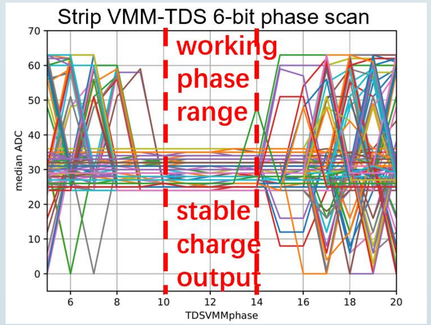
The sTGC electronics team is responsible for the validation of channel connectivity and electronics links, the calibration of channel threshold and numerous clock phases, and the evaluation of noise level. These are all essential to reading out signals with quality signal.

Baseline scan and threshold calibration



Set global threshold to entire VMM and add trimmers to equalize threshold above baseline value for each individual channels.

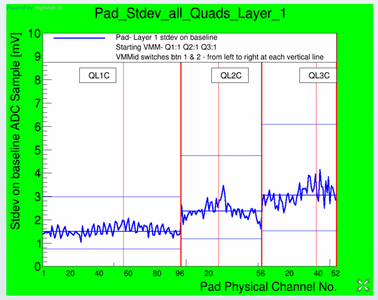
TDS-VMM clock phase scan



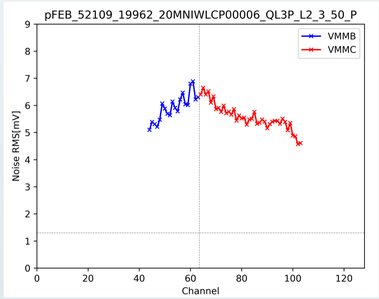
Strip-TDS uses a common clock to read VMM 6b ADC from all channels. A clock phase scan is performed to determine the range that has stable output for all channels.

Noise study

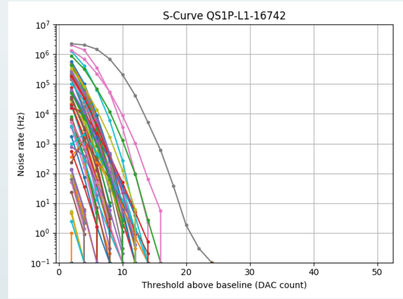
Help assess detector to frontend boards connectivity as well as signal routing scheme. Several adaption of the grounding scheme have been made to decrease the noise and stabilize the detector to external noise sources.



SCA-ADC scan

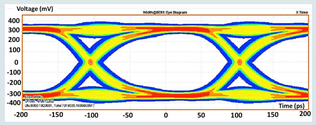


Analog noise scan



Pad noise rate scan

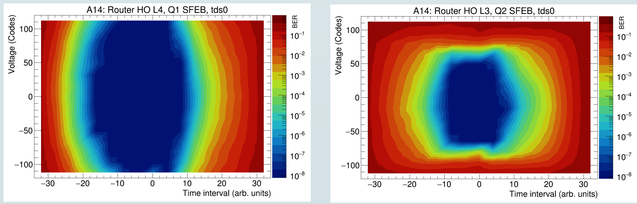
TDS link validation with eye diagram



Classic eye diagram

Classic eye: overlapping of many signal waveforms

Statistic eye: BER as a function of sampling time and voltage



Statistic eyes with BER cutoff at 10^{-8}. Eye on the right indicates larger signal attenuation and more time jitter than the eye on the left since the height and width of the eye are smaller.

Conclusion

- The sTGC electronics team has successfully established the integration and commissioning procedure
- Integration and commissioning of Wheel-A has finished. Wedges already assembled into sectors and installed on wheel
- The team is now working on Wheel-C wedges

Reference

[1] https://project-hl-lhc-industry.web.cern.ch/content/project-schedule. **[2]** Kawamoto, T; ATLAS Collaboration (ATLAS-TDR-020). **[3]** P. Gkountoumis, JINST12, no.01, C01088(2017). **[4]** P. Miao et al, 2020 JINST 15 P11024