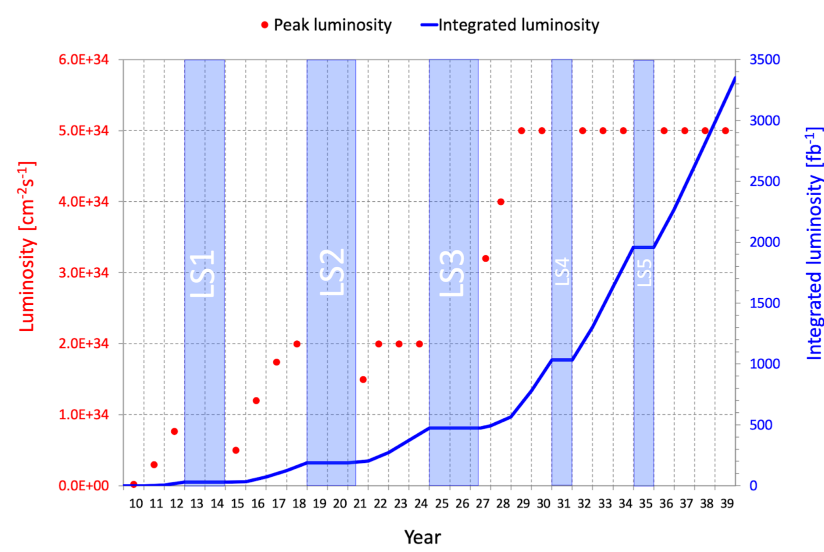
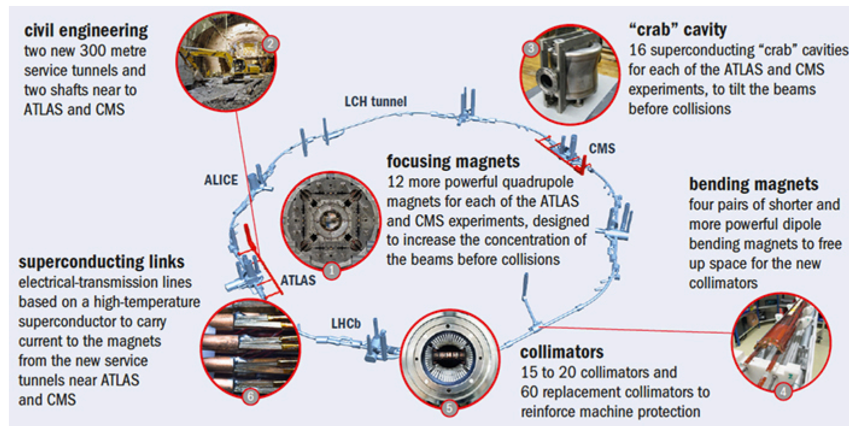
Serial powering and signal integrity characterisation for the TEPX detector for the Phase-2 CMS Inner Tracker

K. Cormier, B. Kilminster, S. Leontsinis, A. Macchiolo, A. Reimers, Y. Takahashi (University of Zurich) for the CMS Tracker Collaboration

HL-LHC and the Phase-2 upgrade

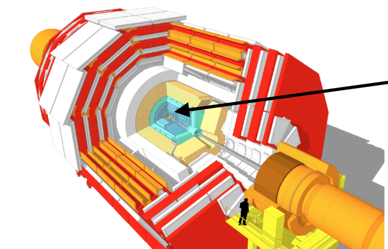
- CERN accelerator complex will be upgraded during the Long Shutdown 3 (LS3 or phase-2) in order to increase instantaneous luminosity up to 5 - 7.5 x 10^{34} (1/cm²s), compared to 1 x 10^{34} at Run-2
- Aim for 3000/fb integrated luminosity until ~2040 (High-Luminosity LHC; HL-LHC)
- Additional pp collisions within the same or adjacent bunch crossings, called pileup, will become 150-200





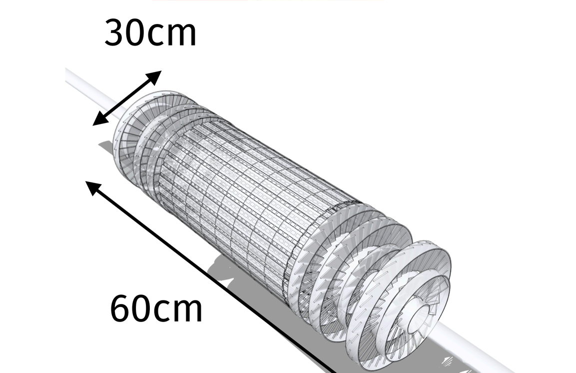
- Precision measurement of the electroweak parameters (α, G_F, m_Z, m_W, m_t, m_H, $\sin^2\theta_{eff}$)
- Higgs self-coupling
- Extending the reach of direct new physics searches

CMS Inner Tracker



Silicon pixel & strip detectors

- Reconstruct charged tracks with > 99% efficiency and calculate its momentum
- Primary- and secondary-Vertex reconstruction



Current system

- 4 layers (barrel) + 6 disks (endcap)
- Inner radius = 3cm
- Active silicon area = 1m²
- 124M channels
- Pixel size = 100 x 150 um²
- Radiation tolerance = 300 Mrad

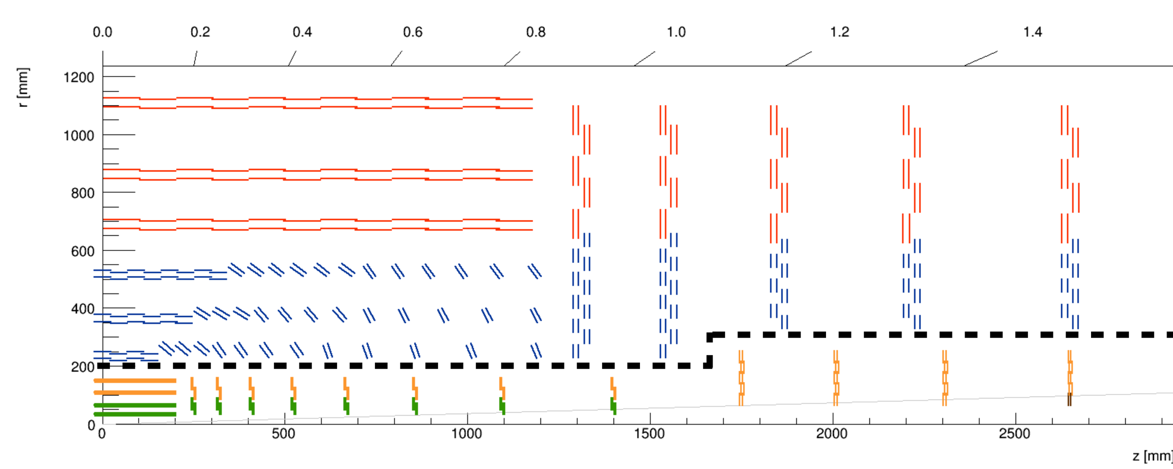
Can we maintain tracking capability in HL-LHC? → No!

- 8 x higher pileup (25 → 200)
- 8 x higher hit rate (→ 3.2 GHz/cm²)
- 4 x longer latency (3.2 → 12.8 μs), need 8 x 4 = 32x bigger buffers
- More radiation tolerance

We need **new tracking system** with

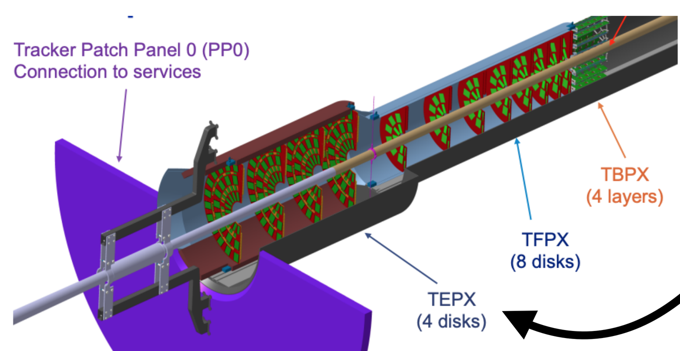
- Increased granularity (x6 smaller pixel size)
- Increased detection coverage (|η| < 4)
- Reduced material budge (light mechanics, services)
- Lower detection threshold (new readout chip)
- Simple installation and removal

Phase-2 tracker system and the TEPX



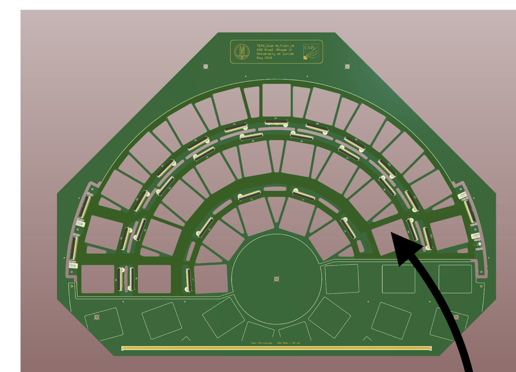
Outer tracker:
2S (Strip-strip sensor modules)
PS (macro-pixel strip sensor modules)

Inner tracker:
2x2 pixel chip modules
2x1 pixel chip modules



- Composed from more than 2 x 10^9 pixels
- Corresponding to an area of 5m²
- 2 disks (double Dee) with modules on front and back side form one "z position"
- Modules arranged in 5 rings on double Dee

Our contributions to the TEPX design

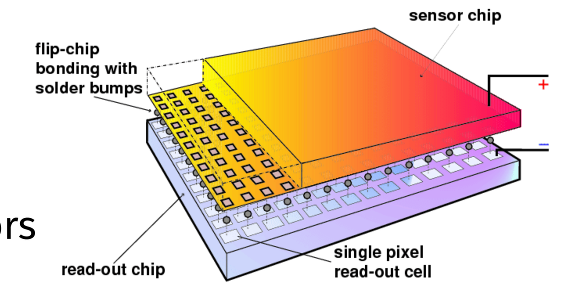


- 3 Layer Polyimide PCB with Epoxy adhesive
- 160µm thickness
- 0.2 x 0.1mm component size (except for 04. x 02mm and 0.8 x 0.5mm for the HV)
- 110 x 250 µm pad size
- Meshed input and return current layers - reduced material

Hybrid pixel module

High-Density Interconnect (HDI)

- Pixel chip is the only active component (no auxiliary electronics)
- Passive: decoupling capacitors and connectors (power and readout)
- Wire bonding



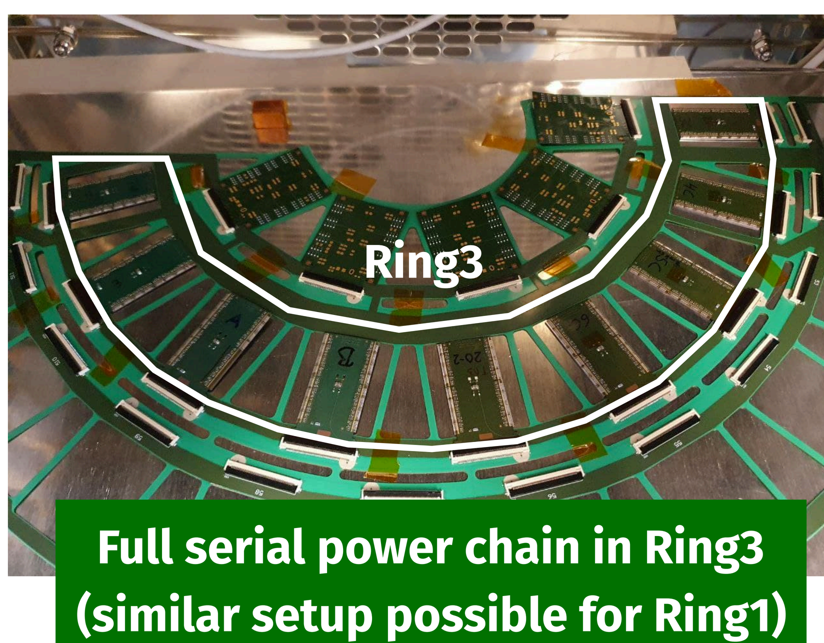
Pixel size = 25 x 100 um²

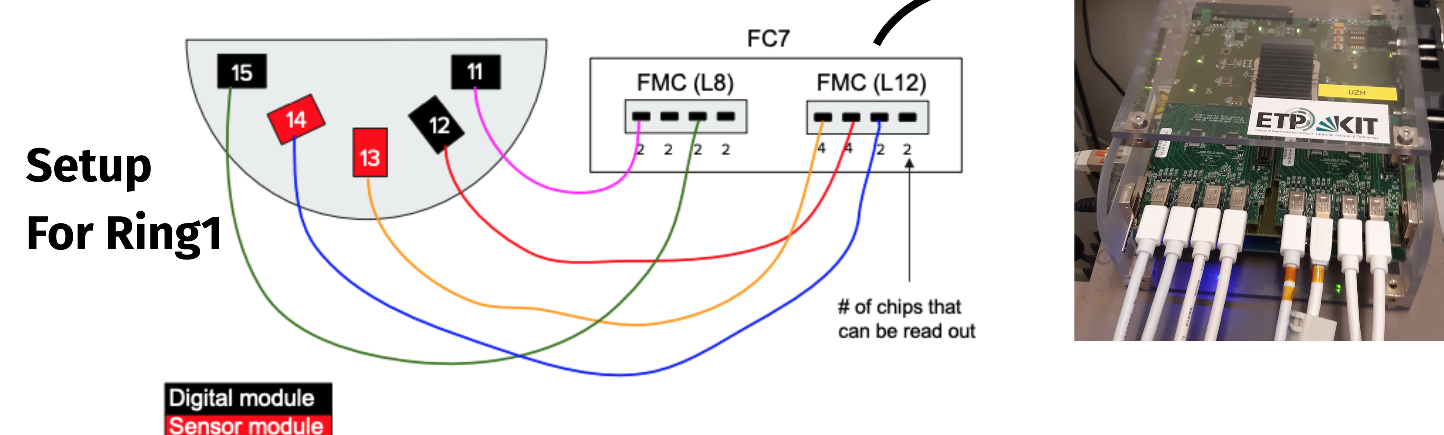
Serial powering and signal integrity test

- Build up the system with all ingredients in place (modules, readout electronics, cabling, serial powering)
- Understand the difference of module behaviour when connected in serial

1) Setup

Climate chamber with -50 deg. ambient temperature

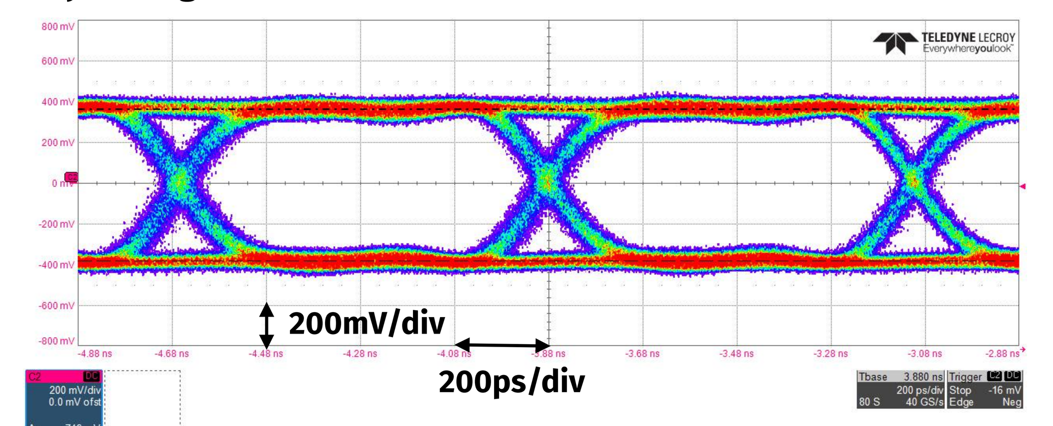




- Digital (analogue) voltage for the RD53 readout chip = 1.3V (1.2V)
- Voltages are provided by Shunt LDO with constant current 6.8A
- In Ring1, the shortest (longest) trace length = 85mm (492mm)

We succeeded, for the first time, to read out and tune all modules in a serial powering chain from Ring1 and Ring3

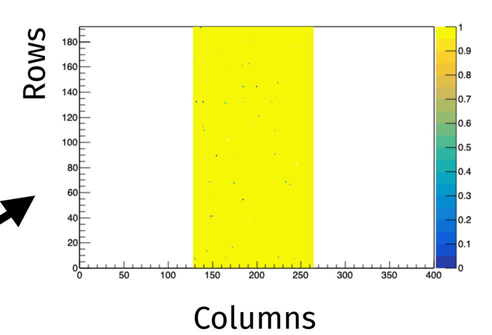
Eye-diagram



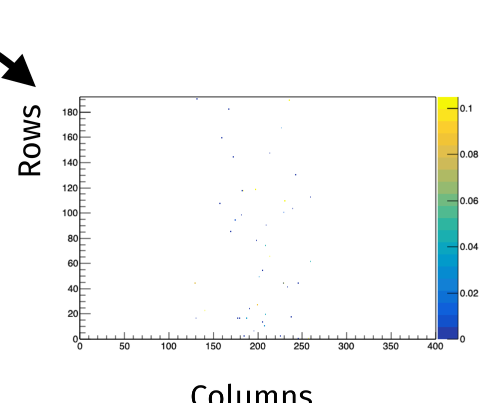
2) Tuning procedure

Tuning (fully automatic) takes roughly ~1h per each module

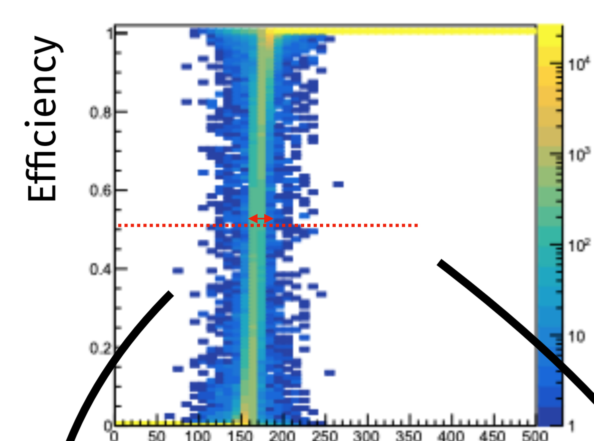
- **Voltage tuning**
  Tune analogue & Digital voltages for RD53 readout chip
- **Pixel Alive**
  Inject calibration charge and see if it corresponds
- **Noise scan**
  Identify noisy channels and mask them
- **Threshold equalisation**
  Adjust threshold trim bit to a common target threshold
- **Threshold adjustment**
  Set all thresholds to ~2000e



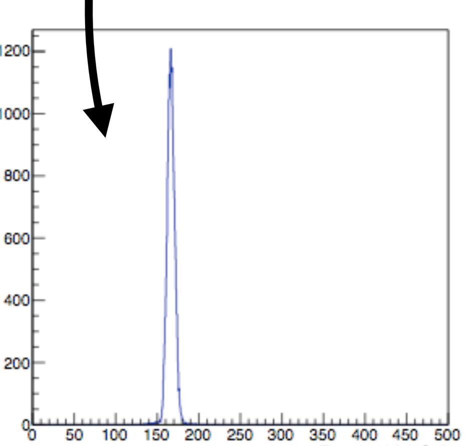
Corresponds to 1 sensor chip (4 chips / module)



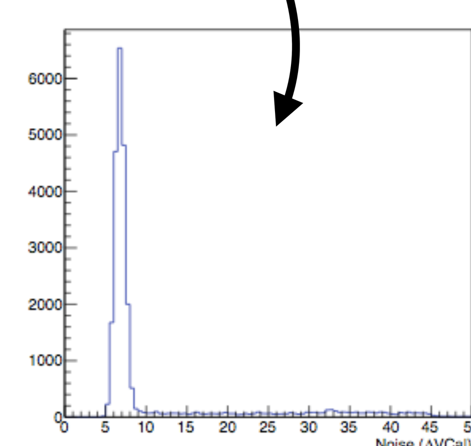
Final performance is characterized, for each pixel channel, by measuring efficiency as a function of injected calibration charge (s-curve)



Injected charge (ΔVCal = # of electrons / 10)

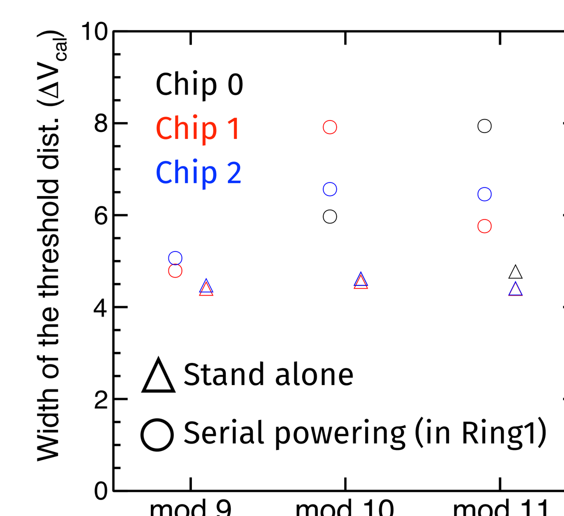


Projection onto the x-axis at eff. ~ 50% (Threshold distribution)

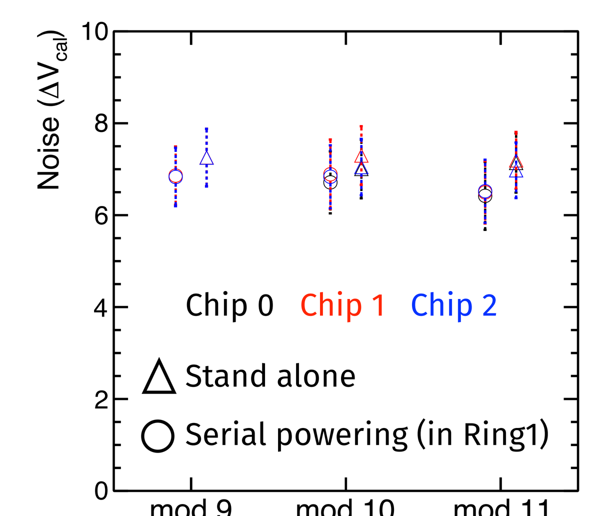


Steepness of the turn-on (indication of the noise-level)

3) Standalone v.s. serial powering chain



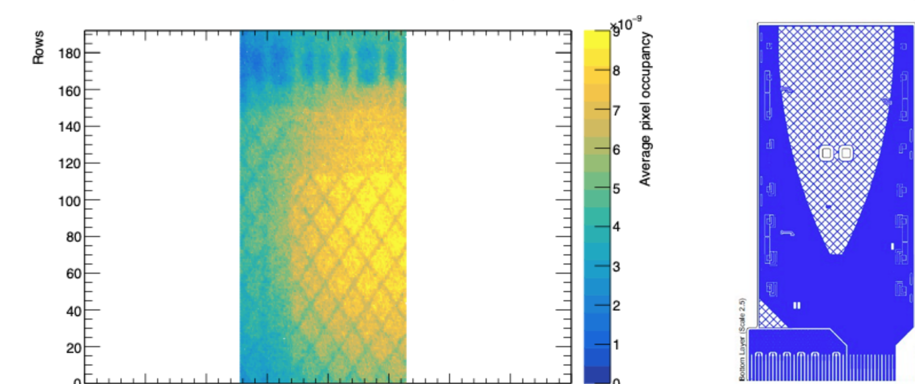
→ slightly worse performance when chained



→ Similar noise level

4) Source scan

Noise scan with ^{90}Sr (β-source, 546 keV e) on top of the module



HDI inner schematic design

- No problem visible in sensor-chip interconnection
- Inner structures of HDI visible