Development of the ATLAS Liquid Argon Calorimeter Read-out Electronics for the HL-LHC

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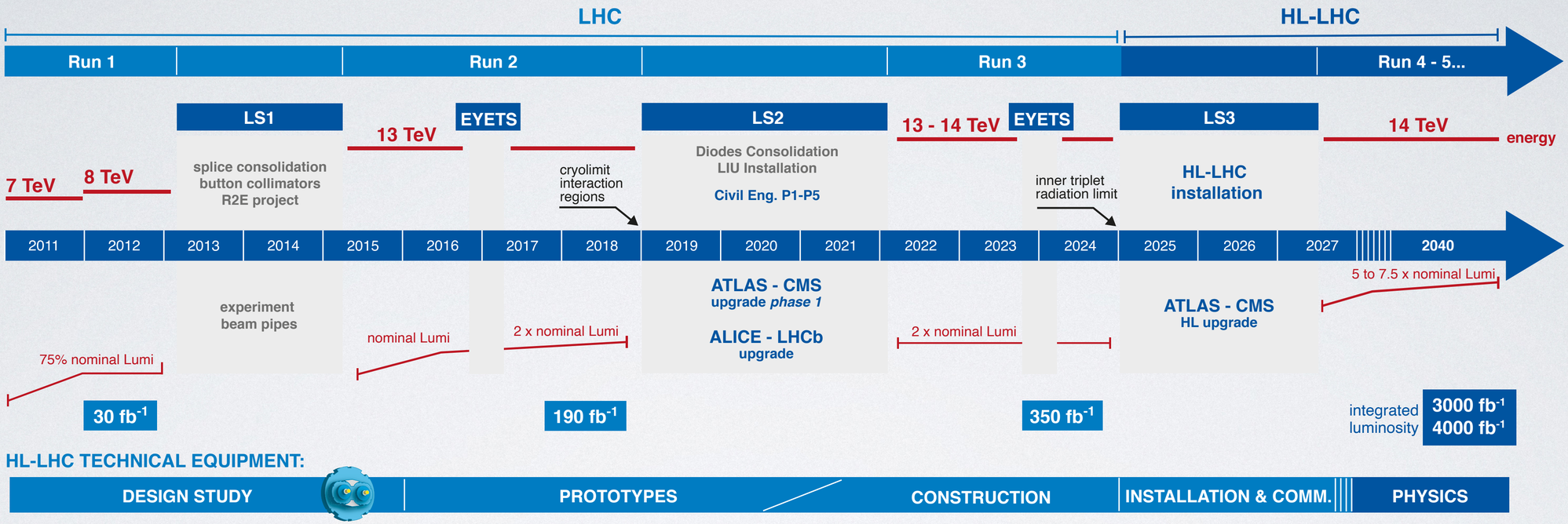
ATLAS
EXPERIMENT

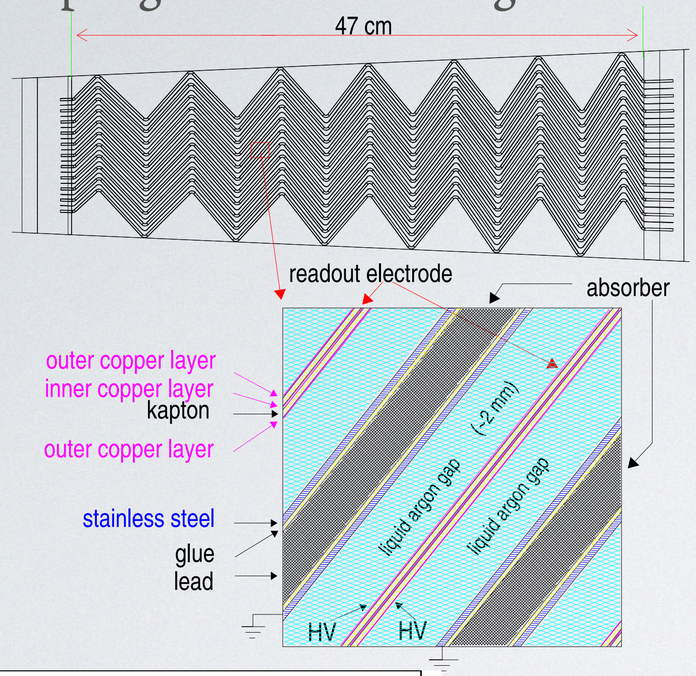
LHC / HL-LHC Plan



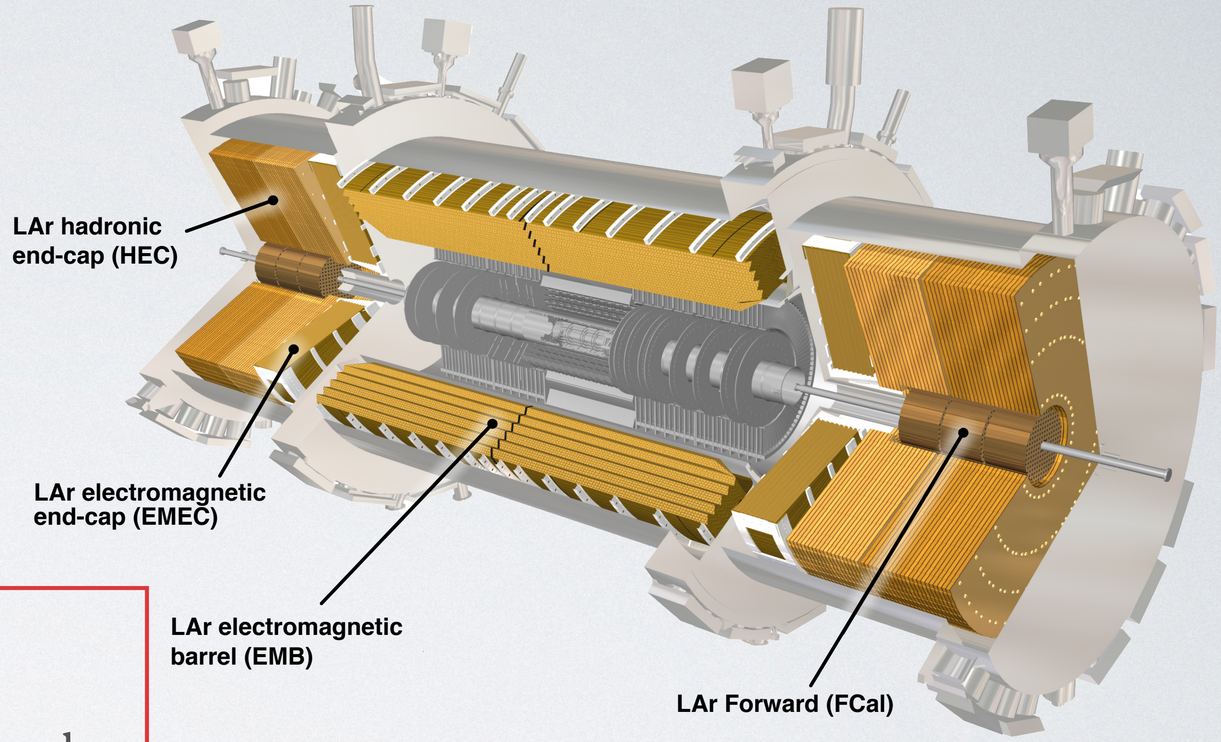
- During HL-LHC, luminosity will reach 5-7 times the nominal value. Average number of interactions per bunch crossing can reach up to 200.
- ATLAS LAr calorimeters electronic read-out system will be upgraded during LS3. Trigger read-out is being upgraded currently during LS2. Physical detector will remain unchanged.
- The LAr upgrade aims to provide the necessary radiation hardness and make the read-out chain compatible with future ATLAS trigger read-out system.

ATLAS Liquid Argon (LAr) Calorimeter

- Sampling calorimeter using LAr as active material

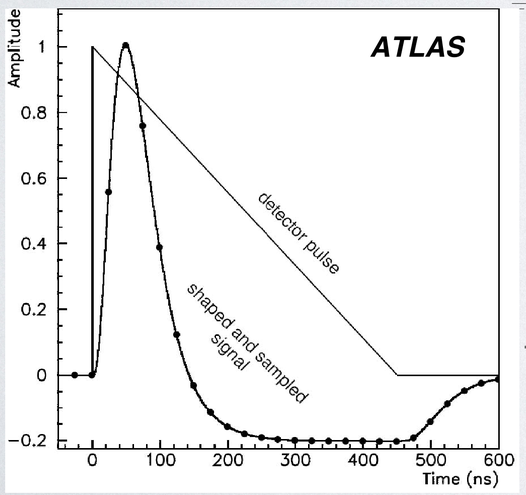


HEC: Parallel plate design using copper plates



EMB & EMEC: Accordion-like structure with absorber lead plates, enabling a full azimuthal coverage

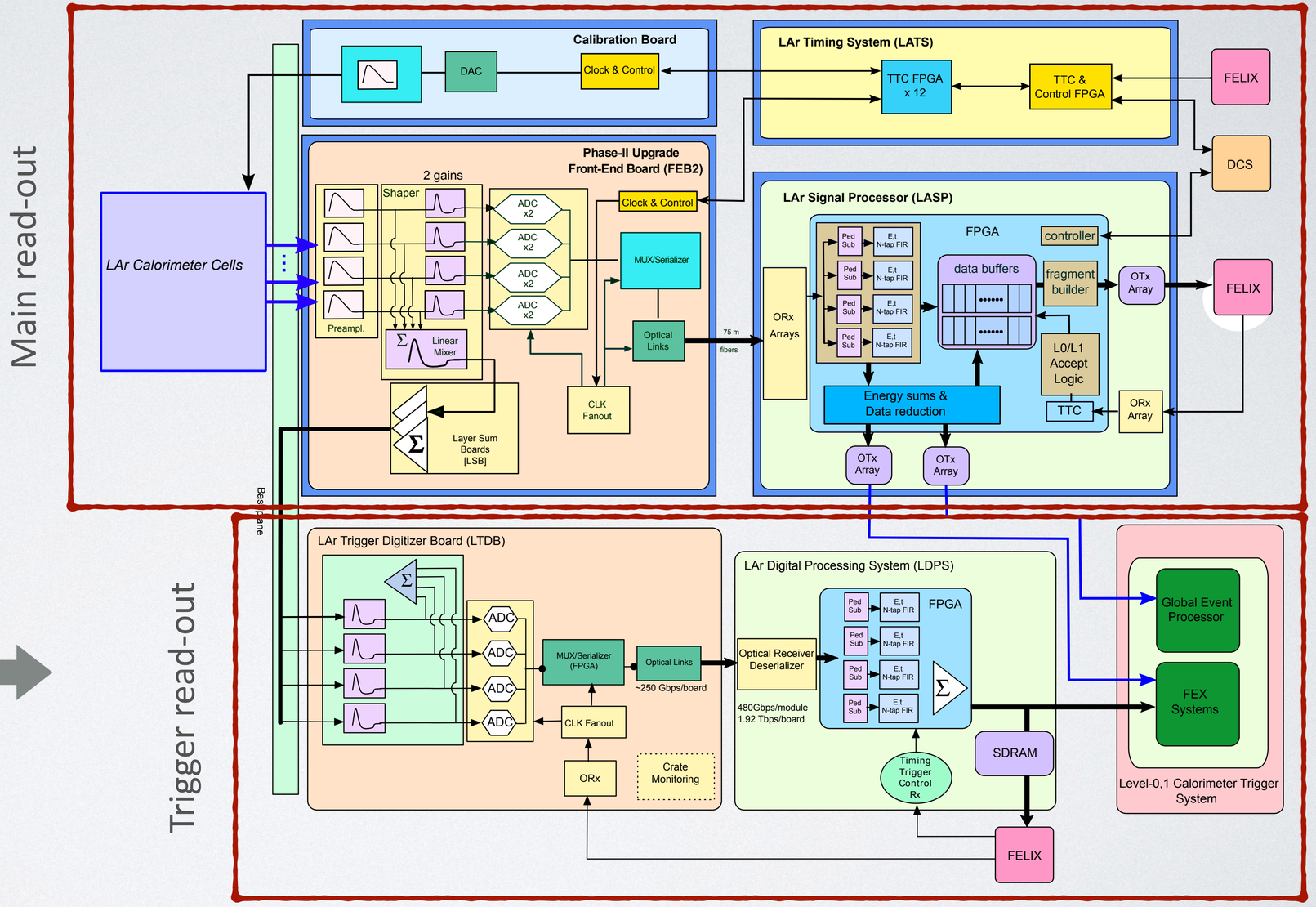
FCal: paraxial electrode structure with copper and tungsten as absorber



→ CR-RC² shaper is used to create the bipolar output.

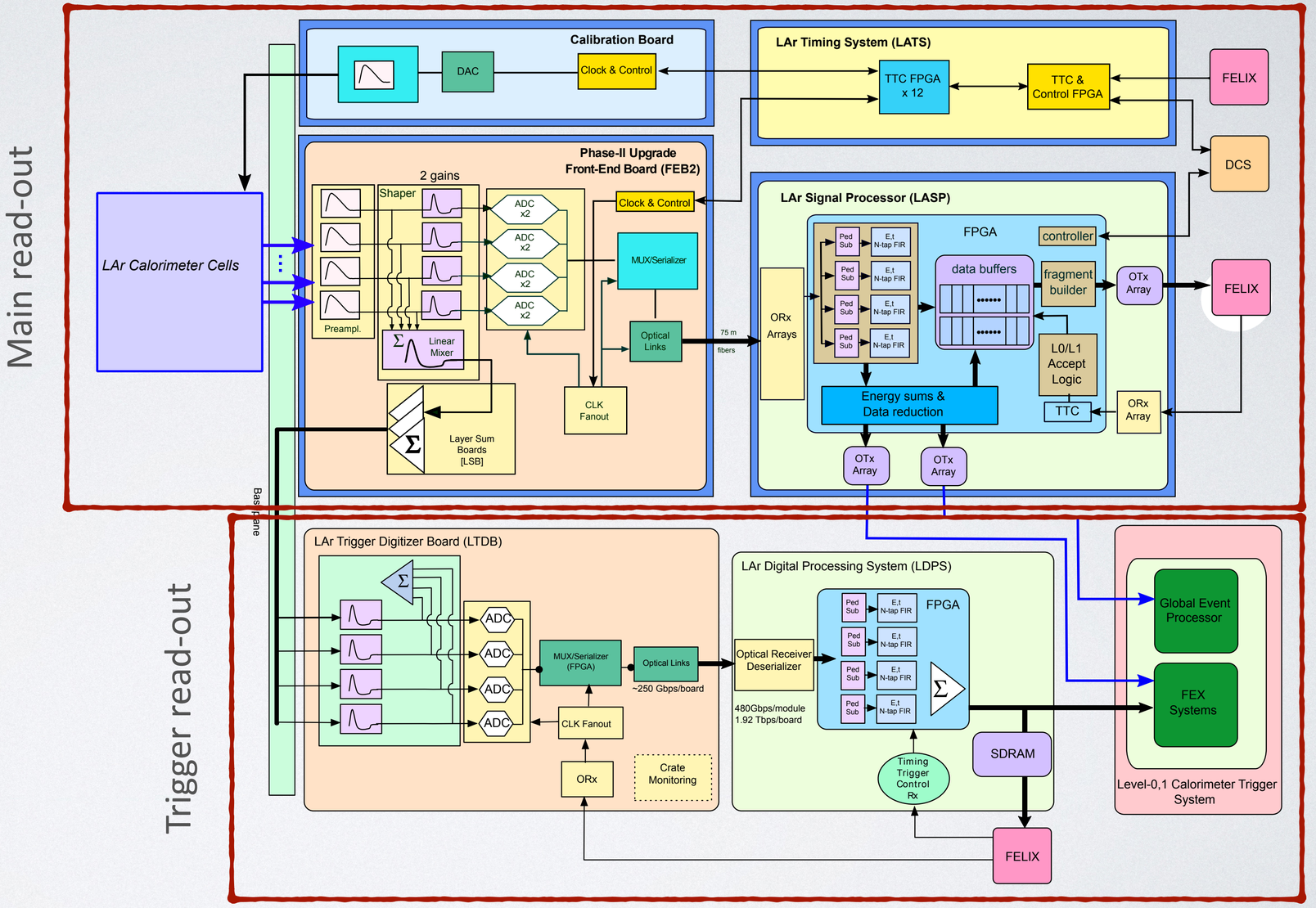
Overview of LAr HL-LHC upgrade

Trigger read-out path is currently being upgraded during LS2 and will remain operational during HL-LHC.



Overview of LAr Phase-II upgrade

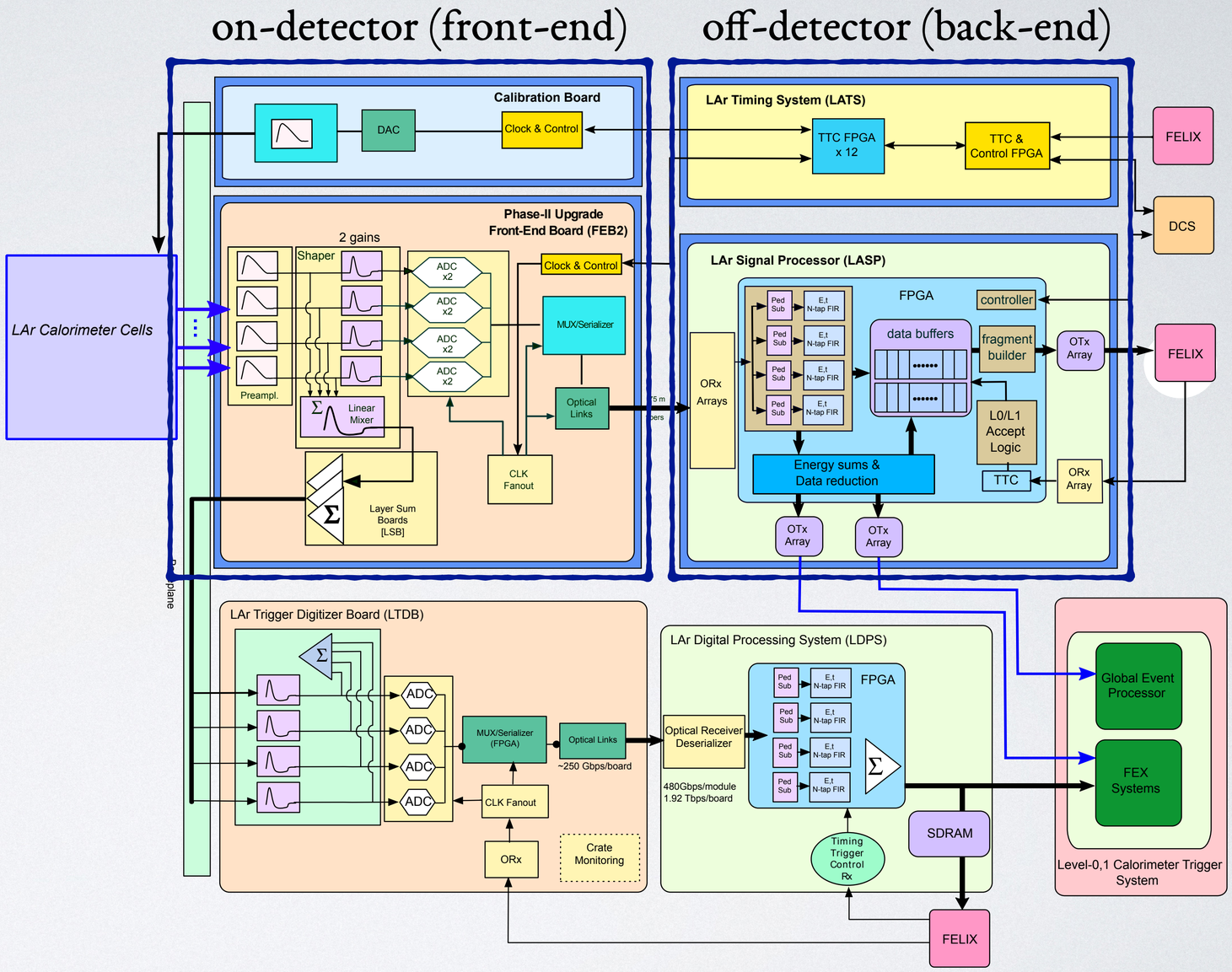
Main read-out will be updated during LS3.



Overview of LAr Phase-II upgrade

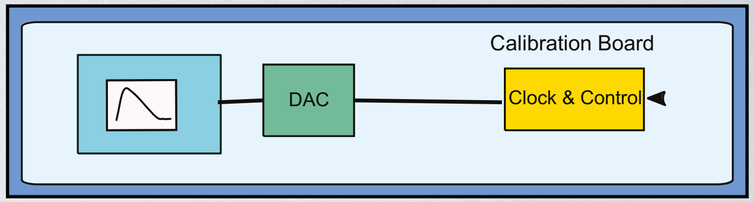
Main read-out will be updated during LS3.

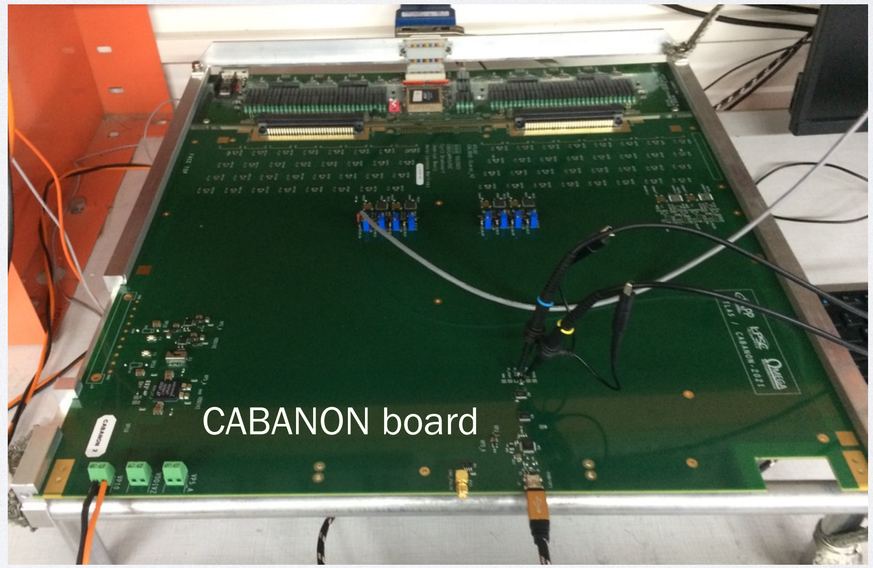
- Free-running scheme: All analog signals will be digitized and sent off-detector at 40 MHz.

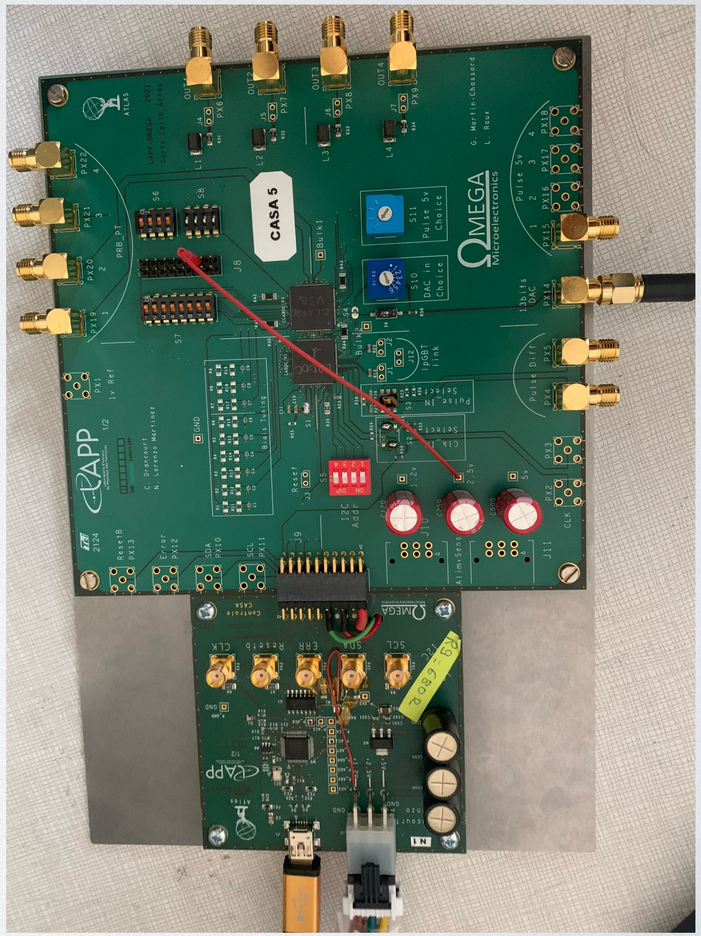


Calibration board

- Injects signals similar to ionization pulses directly into calorimeter cells for calibration of read-out electronics
- Requirements:
  - Integral non-linearity < 0.1%, pulse rise time < 1 ns, 16-bit dynamic range and radiation tolerance of 1.8 kGy
- CLAROCv3 + LADOCv1:
  - CLAROCv3 : Integrated ASIC, HV-CMOS (XFAB 180 nm), 4 high frequency (HF) switches to pulse up to 4 calibration channels
  - LADOCv1: TSMC DAC chip & I2C
  - CASA test board: to test CLAROCv3 + LADOC
- 32 channel (8 ASIC) calibration prototype board (CABANON) is produced and is currently undergoing various tests.

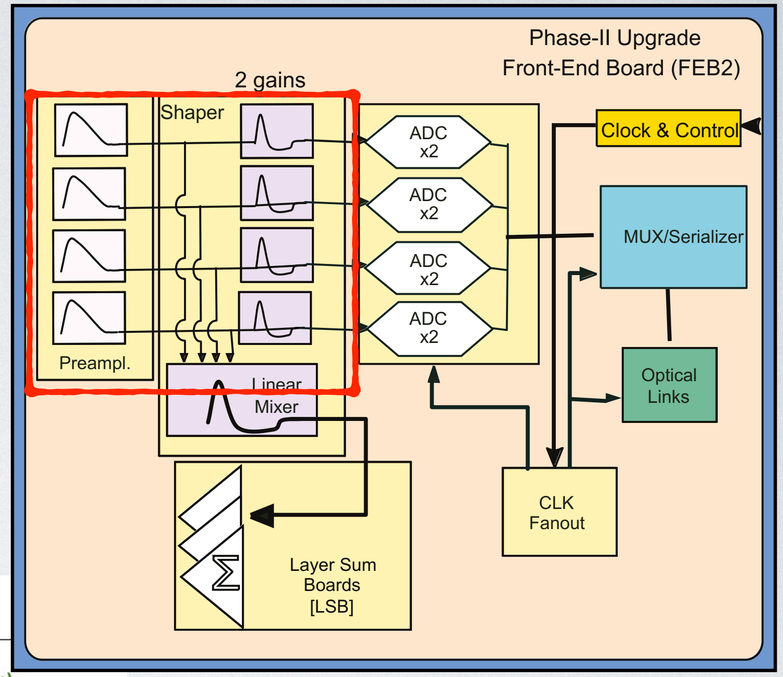






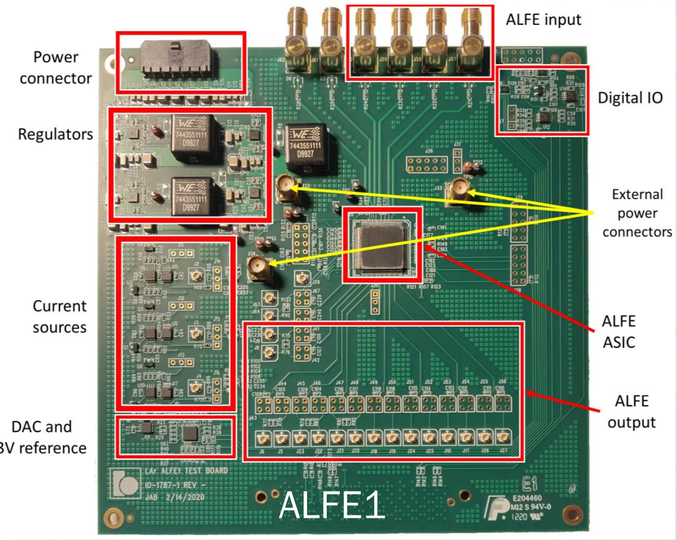
Preamplifier/Shaper

- Performs amplification and bipolar shaping of calorimeter signals
- Both preamplifier and shaper implemented on same chip
- Requirements:
  - Summing 4 channel signals with linearity < 0.2%, CR-RC^2 shaping, low and high gain output for each channel with ratio~23, radiation tolerance up to 1.8 kGy
- Two ASICs, ALFE and LAUROC, were developed and evaluated. The former was selected based on its lower noise levels.
- ALFE: 130 nm TSMC CMOS
  - Differential outputs to ADC
  - v1 satisfies irradiation requirements and analog specifications
- For HEC, polarity of amplified signals is inverted. → HEC-specific preshaper ASIC to correct for inverted polarity: HPS
  - Design based on existing preshaper+ALFE/LAUROC



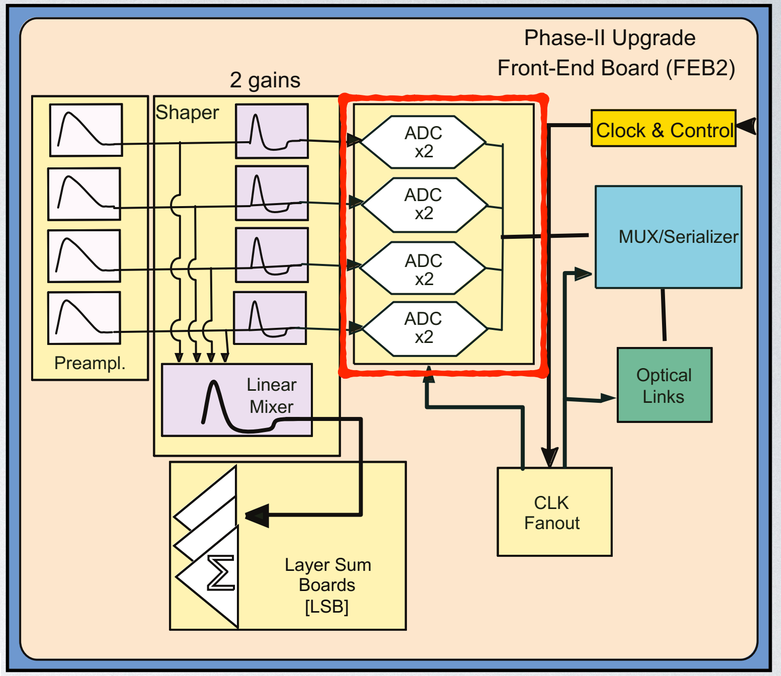
ALFE1 vs ATLAS LAr SPECIFICATIONS

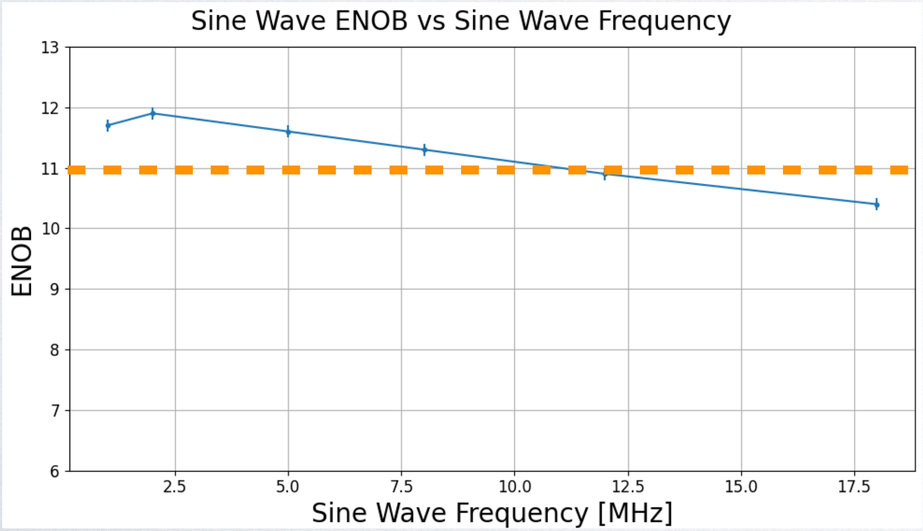
	Specifications		ALFE1 (measurements)
Input Impedance	25 Ω / 50 Ω ± 5%	V	25 Ω / 50 Ω ± 20%
Input impedance tol.	± 5% up to 20 MHz	V	± 5% up to 50 MHz / 30 MHz
Input current range	10 mA / 2 mA	V	11.25 mA / 2.4 mA
Output range	0.1 – 1.1 V	V	
Output P DC LVL	300 mV ±150 mV	V	300 mV +300 mV/-60 mV
Output N DC LVL	900 mV ±150 mV	V	900 mV -300 mV/+60 mV
Shaping	CR-RC^2	V	
High Gain / Low Gain ratio	22 tol. ±5	V	~ 21 (for 25Ω and 50Ω)
Peaking times	45 ns / 40 ns ±5 ns τ steps	V	45 ns / 40 ns
INL HG	±0.2 %	V	< ±0.045%
INL LG	±0.5 % / ±5%	V	< ±0.16% / < ±0.53%
ENI HG	< 350 nA$^{@50\ ns}$ / < 120 nA$^{@45\ ns}$	V	**< 141.5 nA$^{@46\ ns}$ / < 45.4 nA$^{@38\ ns}$**
XTK	< 0.5% $^{HG-HG}$, < 0.5% $^{LG-LG}$, <11% $^{HG-LG}$	V	< 0.14% $^{HG-HG}$, < 0.33% $^{LG-LG}$, < 0.4% $^{HG-HG}$
PSR CH	10+ dB below 1 MHz	V	15+ dB below 1 MHz
Output load	20 pF (10 pF)*	V	20 pF
Total Power Consumption	< 650 mW	V	< 596 mW (no Trigger Sum)

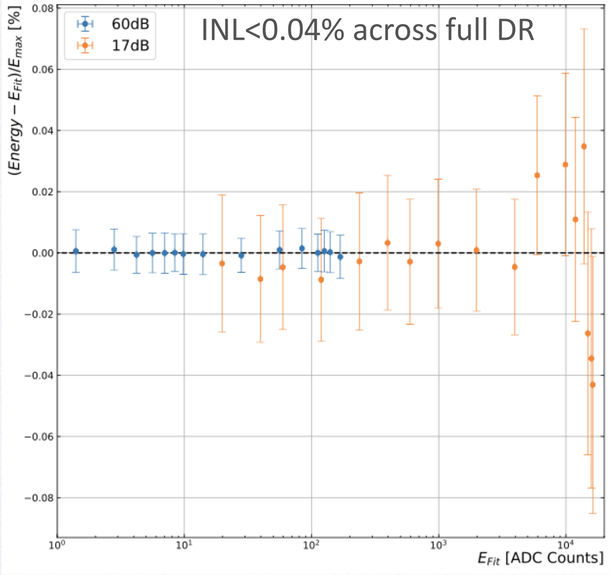


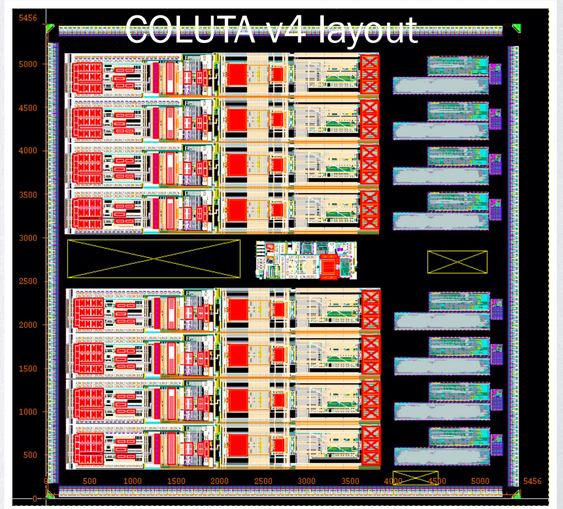
Analog-to-digital convertor

- Digitizes analog signals at 40 MHz with two gains
- Requirements:
  - 14 bit dynamic range, ENOB > 11 bits
- 8 ADCs/ASIC: 4 calorimeter channels at 2 gains
- COLUTAv4:
  - 65 nm custom CMOS
  - 14-bit Multiplying DAC (MDAC) + 12-bit Successive Approximation Register (SAR)
- Analog parts on COLUTAv3 meet resolution and radiation hardness requirements. Some improvements planned for I2C radiation hardness.
- COLUTAv4 ready for submission in September 1st run.



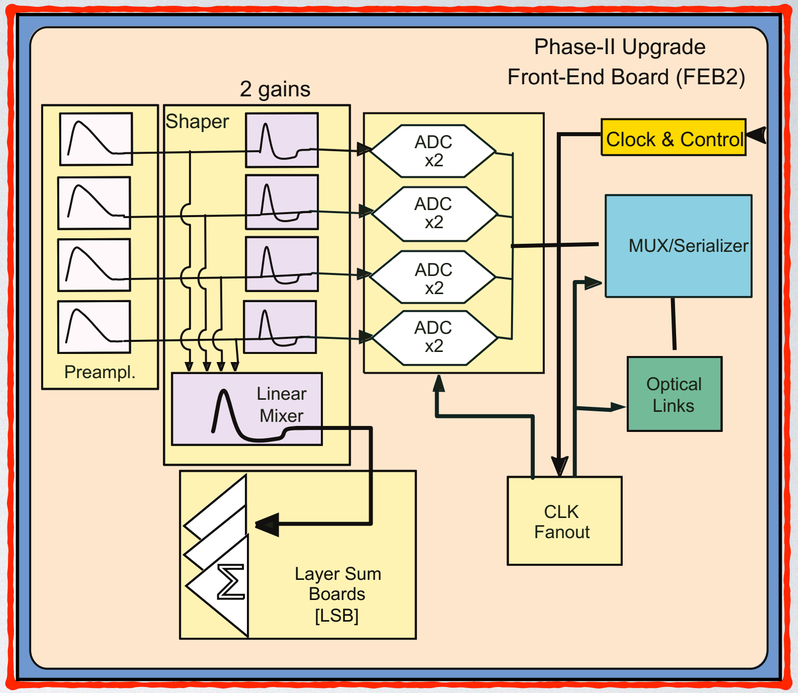


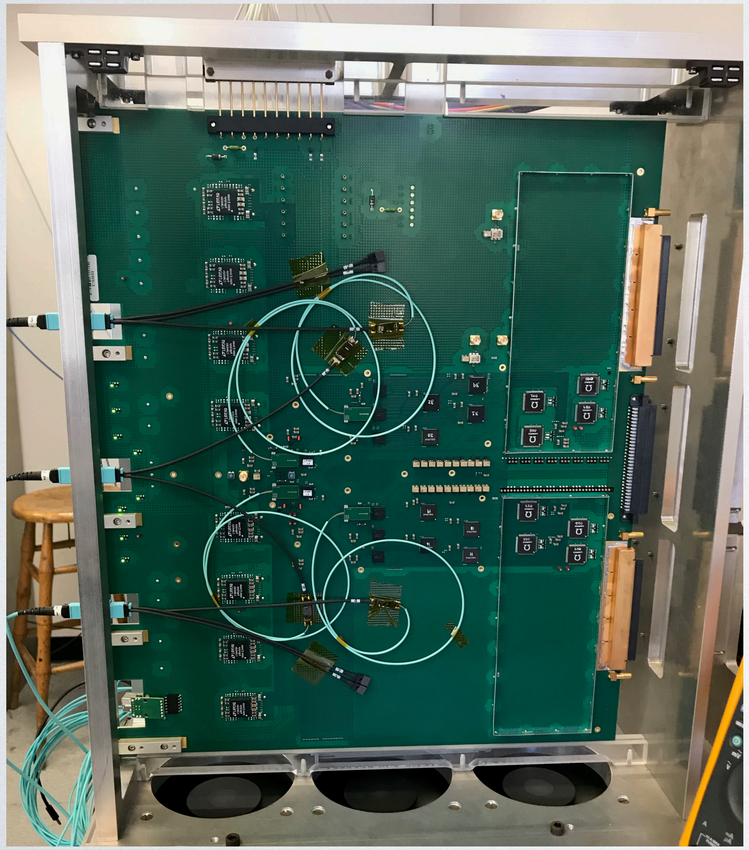




Front-end board (FEB2)

- Integrate several custom components and ultimately read-out 128 calorimeter cells per board
- Provide clock distribution and control, configuration and monitoring functions
- Also including Layer Sum Boards

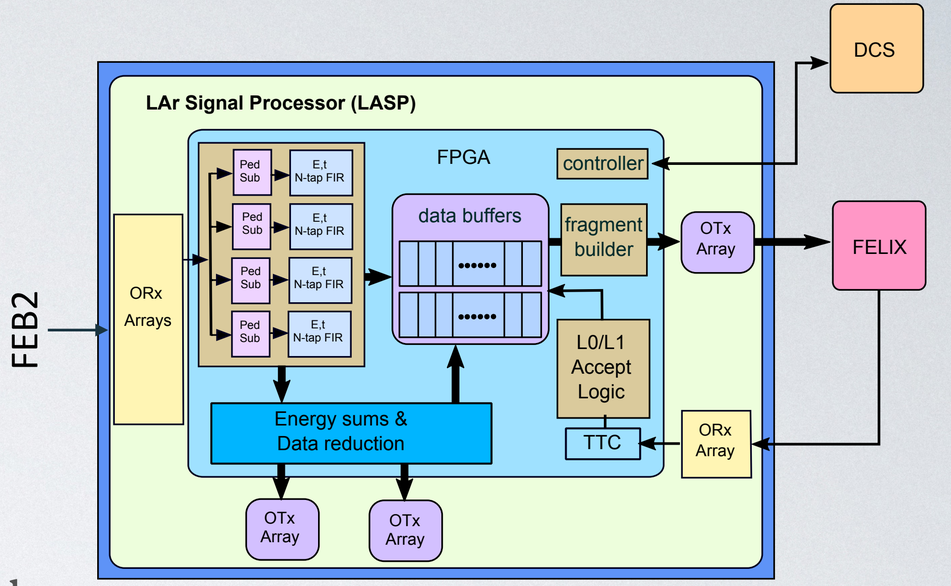


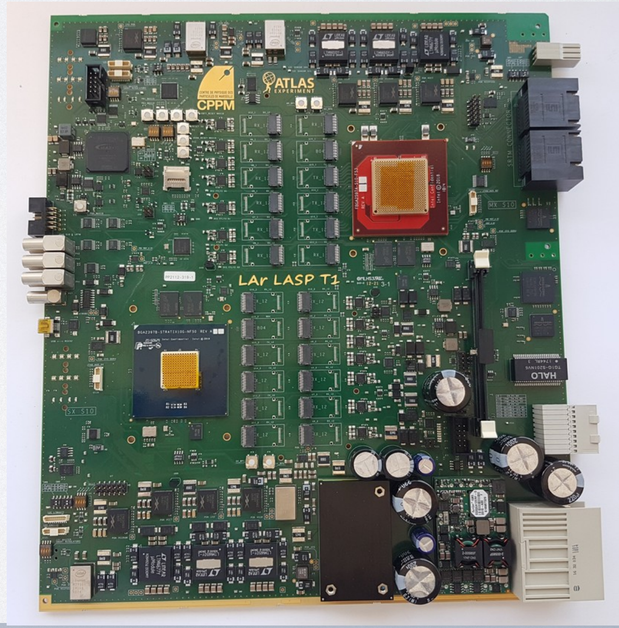


- Slice test board:
  - Represents a “slice” of the final FEB2
  - Goal: to demonstrate multi-channel performance, bi-directional control links and radiation tolerant power
  - Integrate pre-prototype PA/shaper, ADC and lpGBT data serializer to read out 32 channel signals
  - Able to successfully read out signals from all 32 channels → ie the front-end read-out chain is functional
  - Control and read-out links are validated

LAr Signal Processor (LASP)

- Digital signal processing, buffering and transmitting data to trigger and data acquisition (TDAQ)
  - Includes gain selection and application of the algorithm used to calculate signal energy and deposition time
- Each FPGA (Stratix 10) handles input from 4 FEBs (corresponding to 512 calorimeter channels). Output from FPGA is sent to TDAQ at 25 Gbps.
- LASP test board:
  - Includes two processing FPGAs (Stratix-10), one control FPGA (MAX10) and 12 FireFly transceiver modules
  - Test board with interposers in place of FPGAs is tested and all functions are confirmed as operational.
  - Test board with FPGAs to be produced soon.

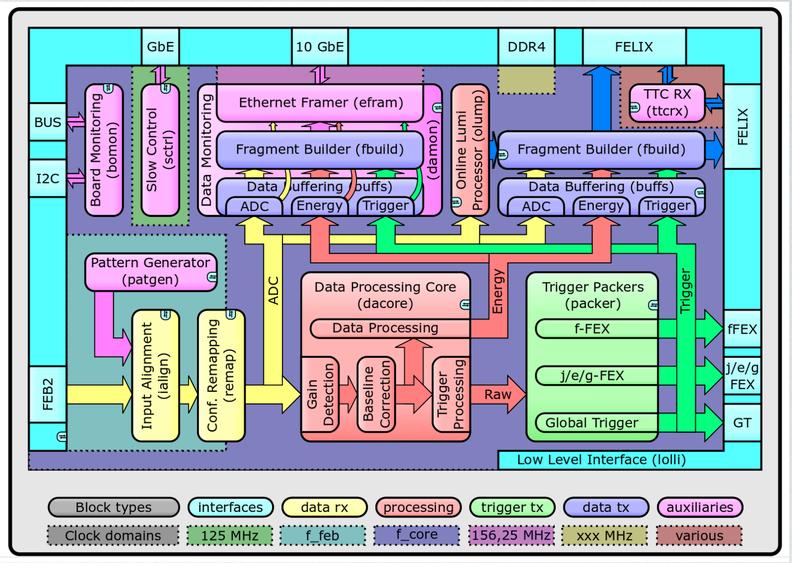


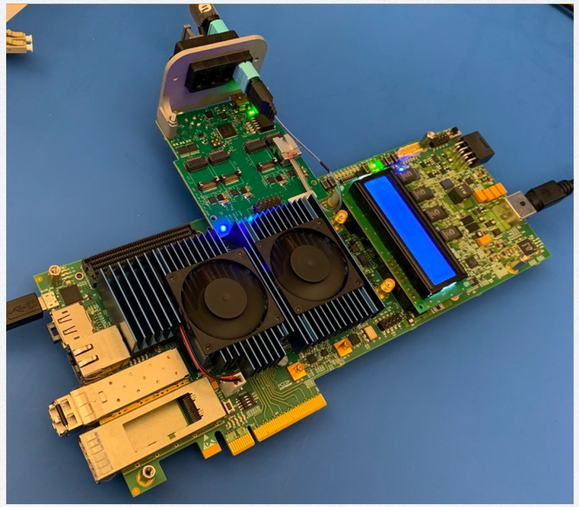


LAr Signal Processor (LASP)

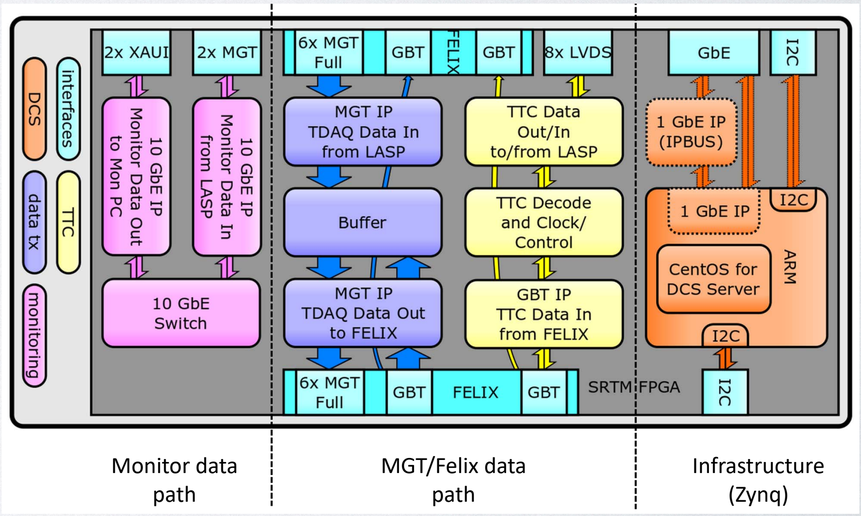
- Alongside the LASP board is a smart RTM (SRTM) which helps with monitoring and provides electro-optics
  - First test board is available and system infrastructure functionality is validated.
- LASP and SRTM firmware (FW) development is ongoing.
- There are ongoing studies concerning implementation of ANNs on FPGAs for energy reconstruction (to replace the previously used optimal filtering algorithm).
  - Simulations have yielded promising results.
- Mezzanine board for Intel devkit are produced to create a “LASP slice”.
  - Setup including LASP and FEB slices is to be tested soon.

LASP FW block diagram



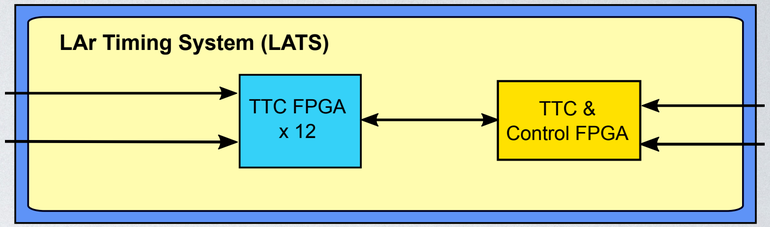


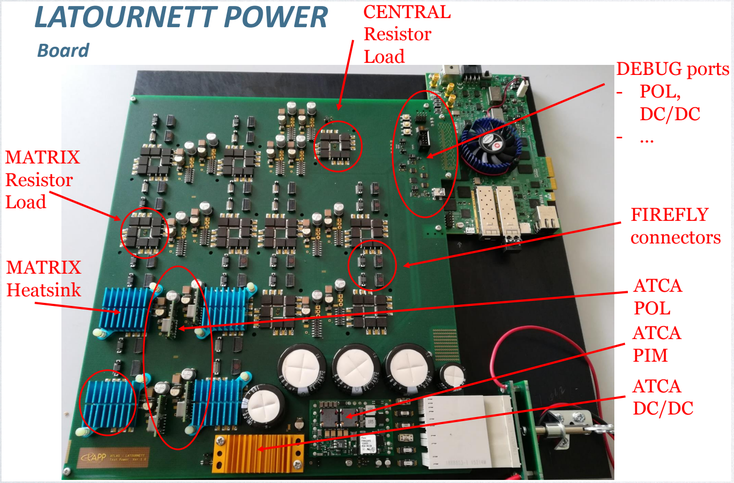
SRTM FW block diagram



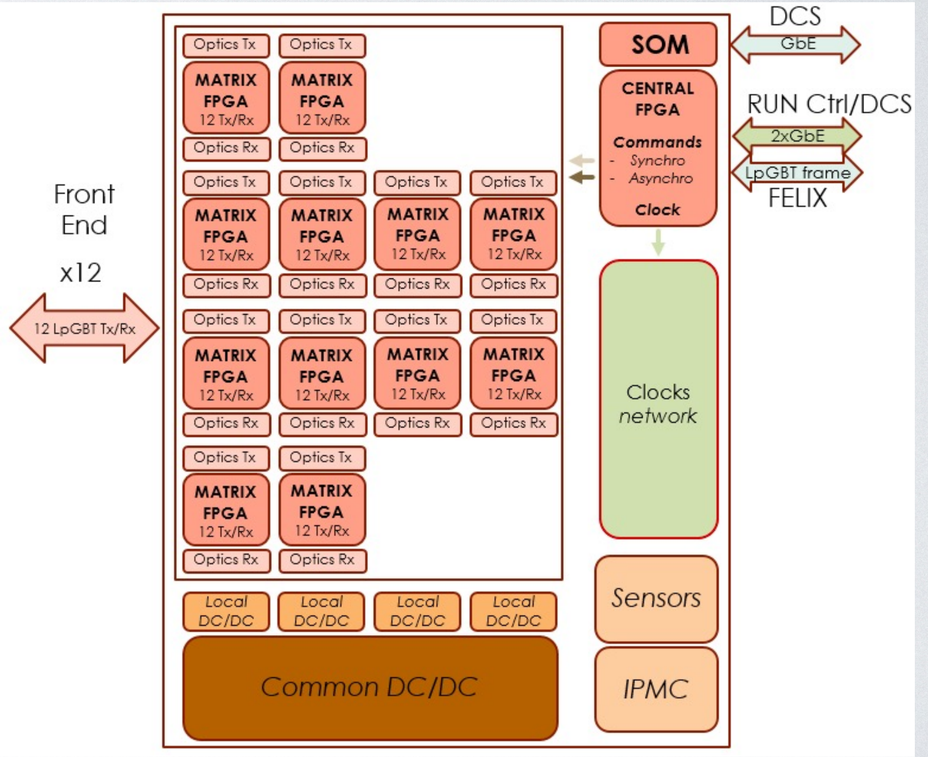
LAr Timing System

- Distribution of TTC signals and configuration and monitoring of FEB2 and calibration boards
- Dedicated clock and control distribution implementation on ATCA blade
- LATOURNETT design:
  - Central FPGA connected to TDAQ
  - Matrix FPGAs connected to front-end
  - System on module embedding OPCUA
  - IPMC for reading critical sensors





- Power board:
  - Board imitating the power tree on LATOURNETT
  - Initial tests are performed, v2 development in progress
- FW in development.



Summary

- ATLAS LAr calorimeter will be upgraded for the HL-LHC to accommodate high expected radiation levels and to be compatible with the future trigger read-out.
- This involves development and extensive testing of custom electronic components.
  - All custom ASICs are at prototype stage.
- We have started integrating and testing different components of the new read-out system.
  - Integration tests have been successful so far.
- On track for timely installation during LS3

Questions/Comments/Concerns?