CMOS Sensors – From a physicists Point of view

24.02.21

Lennart Huth

Fortnightly SiDet R&D Meeting

Outline

- Requirements on pixel sensors
- Basics silicon detector & CMOS principle
- Recent R&D to improve performance
- A future pixel at DESY

Why pixel sensors

In general…

- Reconstruction of particle trajectories at e.g. collider
  - **Vertex/momentum resolution** → small pixels/strips
  - **Pile up** → time resolution
  - **Minimize impact on particle**→ little material
  - **Survive at a collider** → Radiation hardness
- Silicon sensors well established in the last 40 years solving numerous challenges:
  - Detector mechanics
  - Data rates
  - Radiation dose at the LHC
  - Powering concepts
  - …

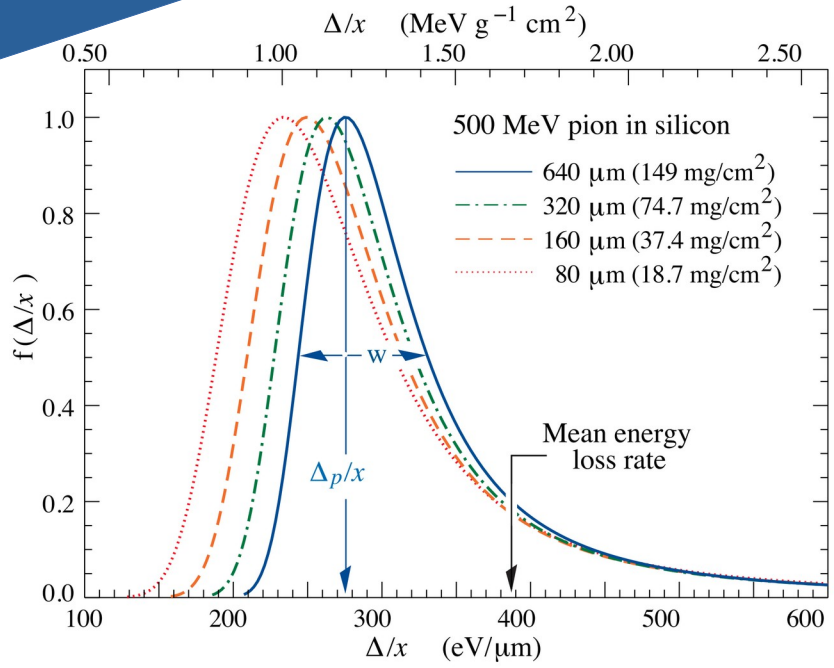
…and in the future

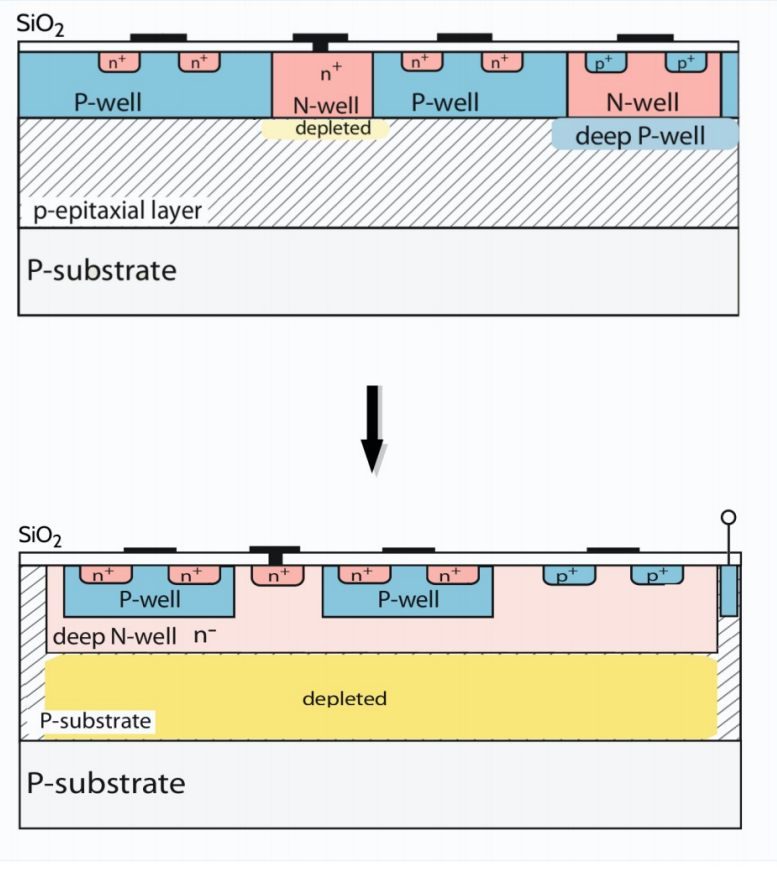
- Next generation of detectors (particle and nuclear physics) need
  - **Finer pitch** → power, channel density
  - **Faster timing** → power
  - **Less material** → thin
- All in one impossible with existing sensors
- We need to
  - Lower the power budget
  - Compress the data on chip to compensate channel density
  - Higher in-pixel intelligence

The ideal pixel tracker

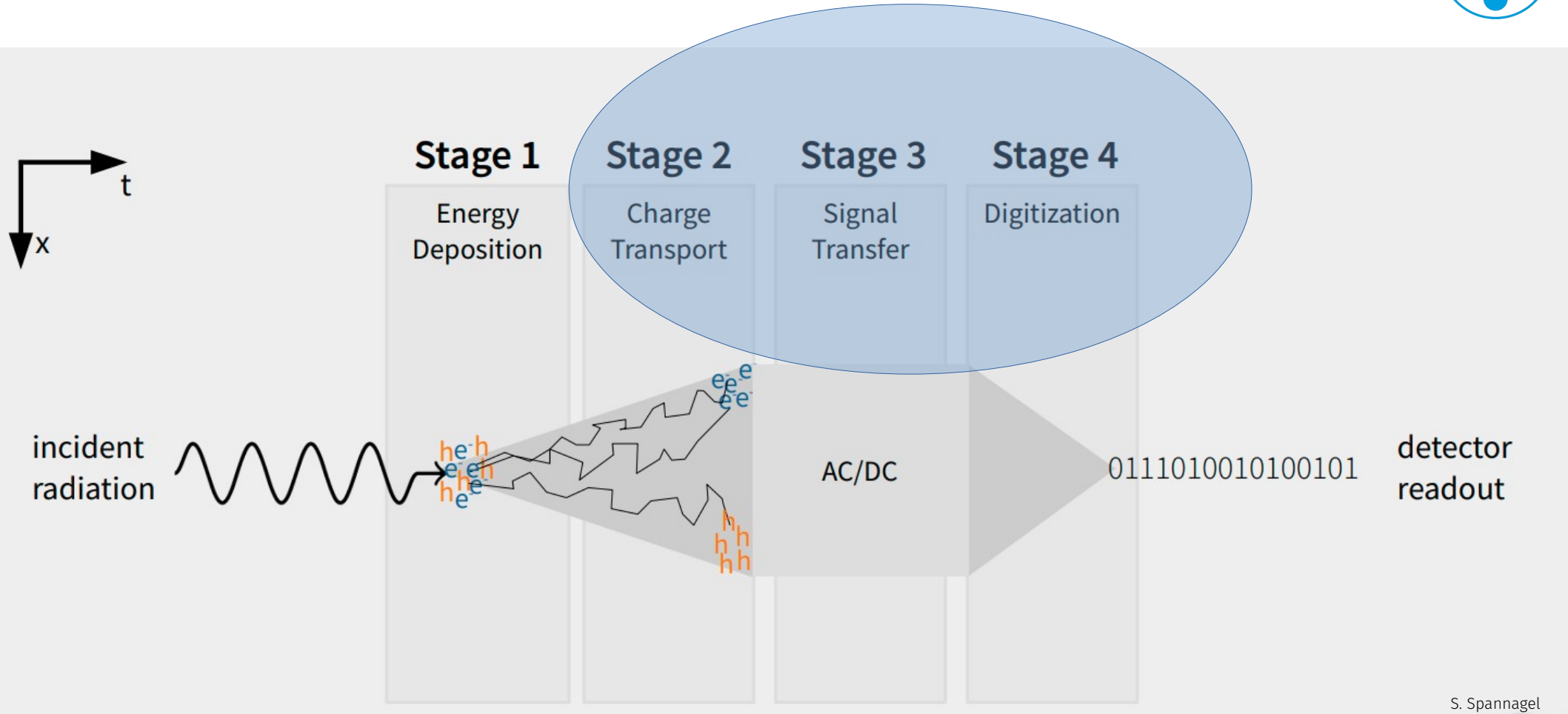
• Infinitesimal position resolution	→ Reduce pixel size, measure charge, engineer fields
• Infinitesimal time resolution	→ Fast collection of charge, engineer fields
• No interaction with detected particle	→ Minimize the material budget
• No power consumption	→ Use power pulsing, etc
• Floating	→ Lightweight mechanics, little cooling, sensor stitching

Charge Collection & CMOS Sensors





A pixel sensor in a nutshell

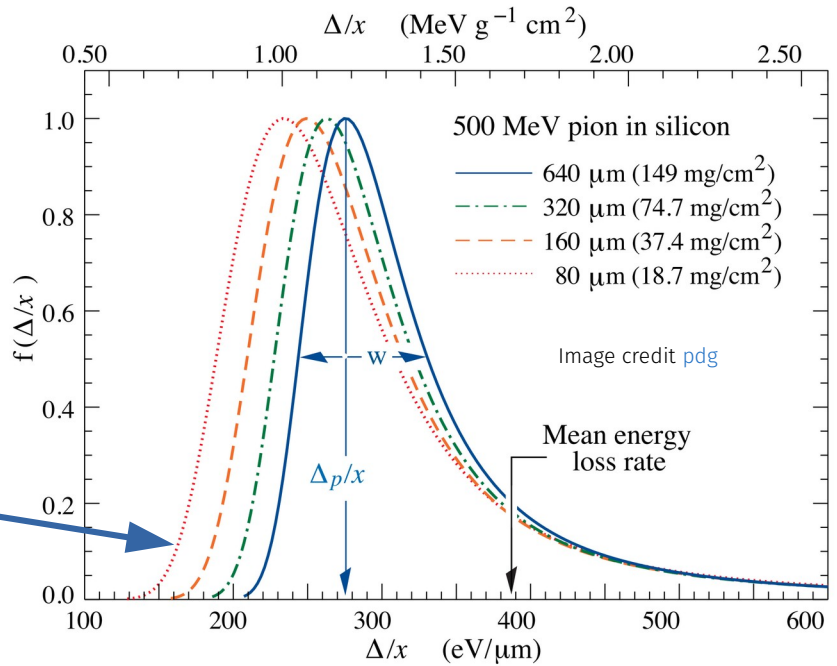


Charge deposition

- Ionization **Bethe-Bloch**, create electron-hole pairs (ehp)
- Stochastic process, on average 80 ehp per um for a minimum ionizing particle
- Asymmetric distribution

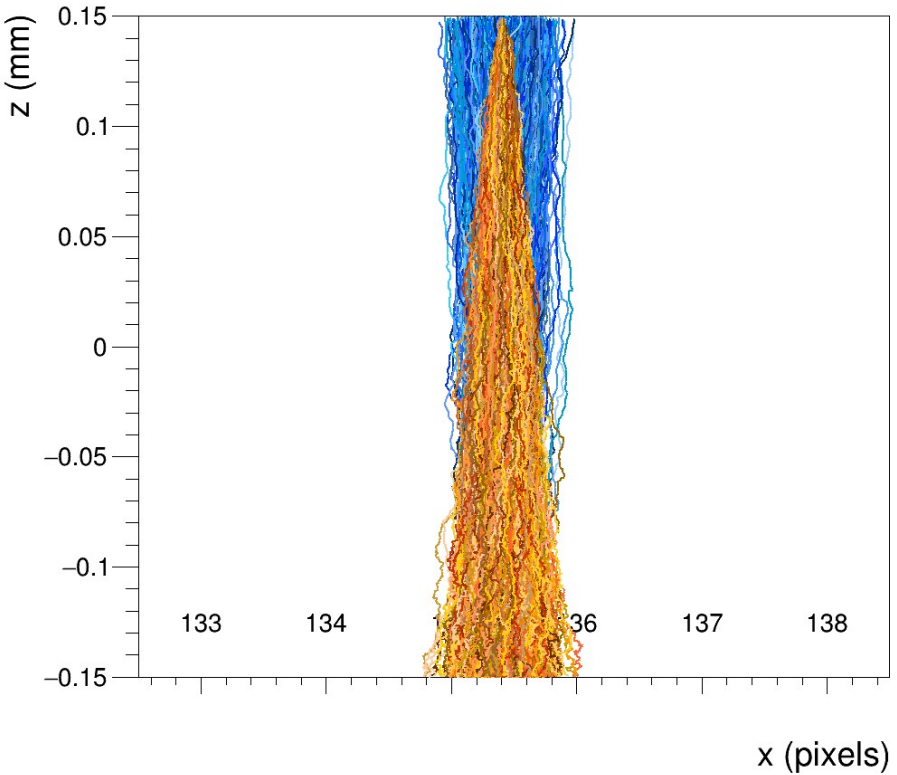
  → MPV<<Mean

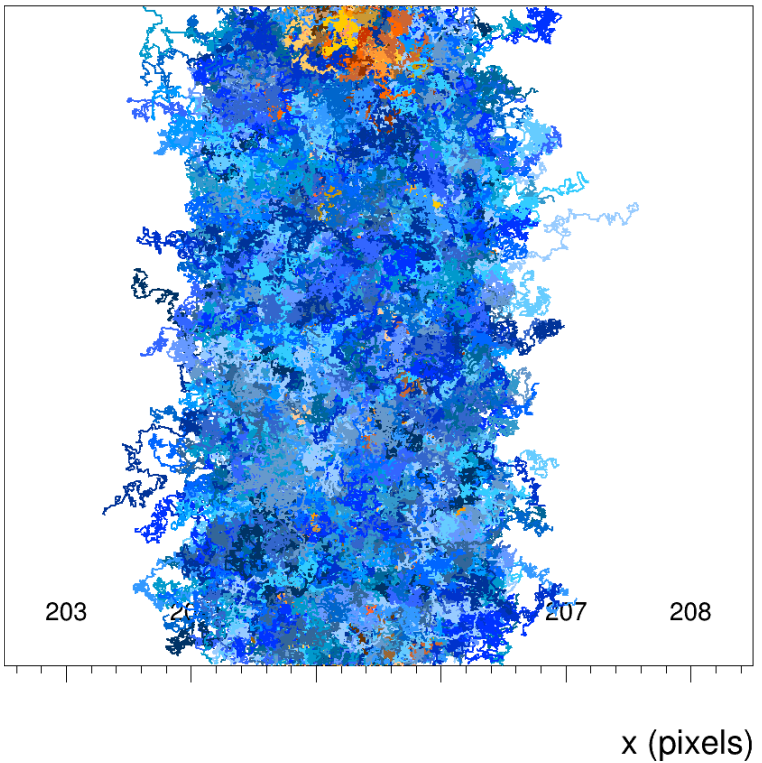
  → lower tail is critical
- Fluctuations larger for thin active layers (**Bichsel/Landau-Vavilov**)
- In addition: Secondaries, deltas,...
- For a pixel sensor, we need to be able to see ¼ of the minimal deposited charge



Charge Transport: Drift vs Diffusion

Charge spread larger for diffusion → better interpolation, but slower

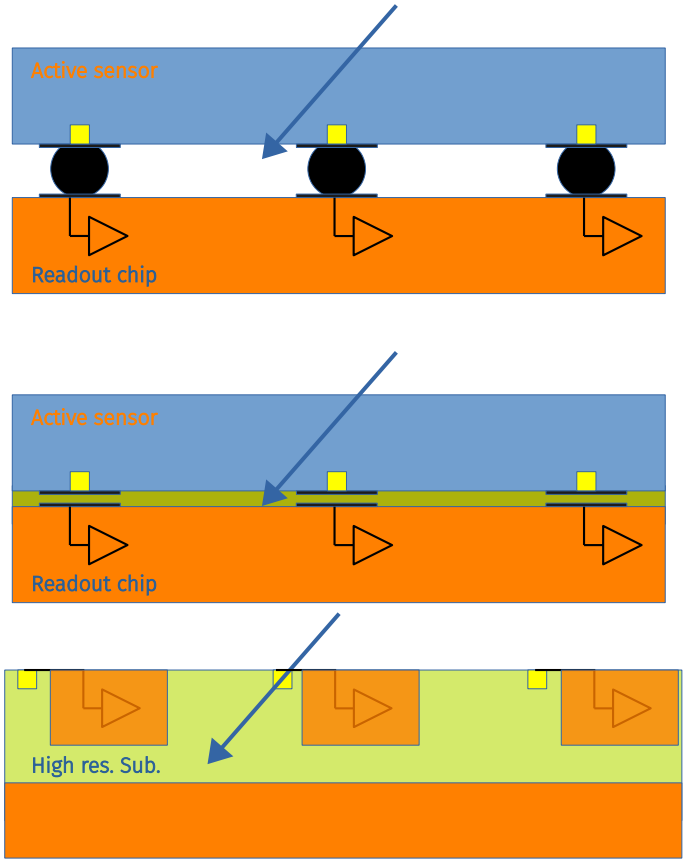




100 ns

Charge transfer and processing

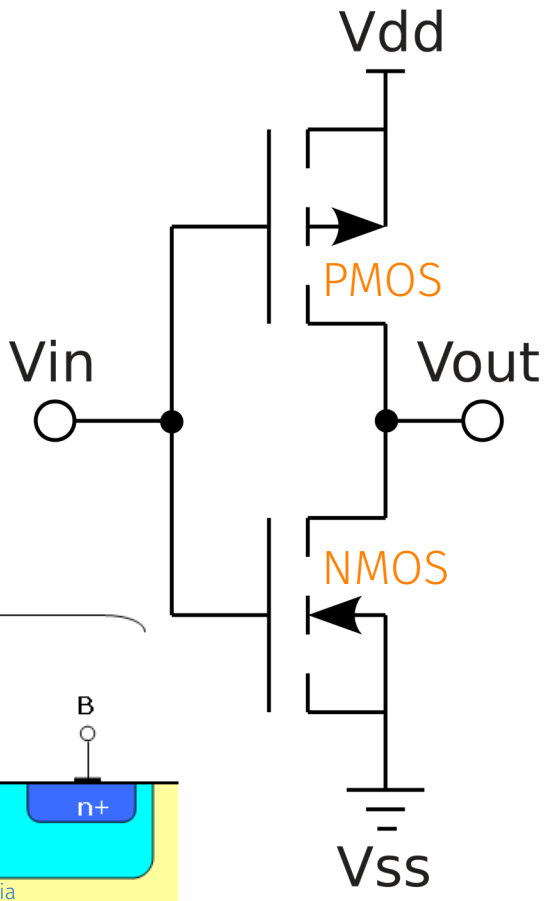
- Collected charge has to be transferred to front-end via:
  - Bump-bonds (DC)
  - Glue, Si02 (AC)
  - Monolithic sensor (DC, simple on ASIC line)
- CMOS based front-end electronics for
  - Amplification
  - Charge measurement
  - Digitization
  - Data transmission
- Support structures, cooling, etc (ignored from now on)



Processing information

- **C**omplentary **M**etal **O**xide **S**emiconductor
- Standard for ASIC/chip design
- Combination of PMOS and NMOS FET
- Example: Inverter
  - → Vin 1→NMOS switches→Vout=Vss
  - → Vin 0→PMOS switches→Vout=Vdd
- Only current drawn while switching
  → power efficient
- CMOS used to amplify, digitize and process charge inputs in HEP

>99% of all ASICs are CMOS



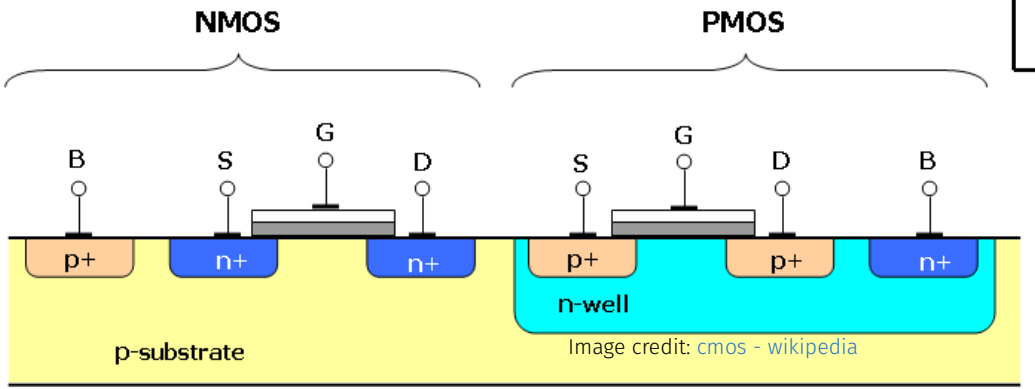
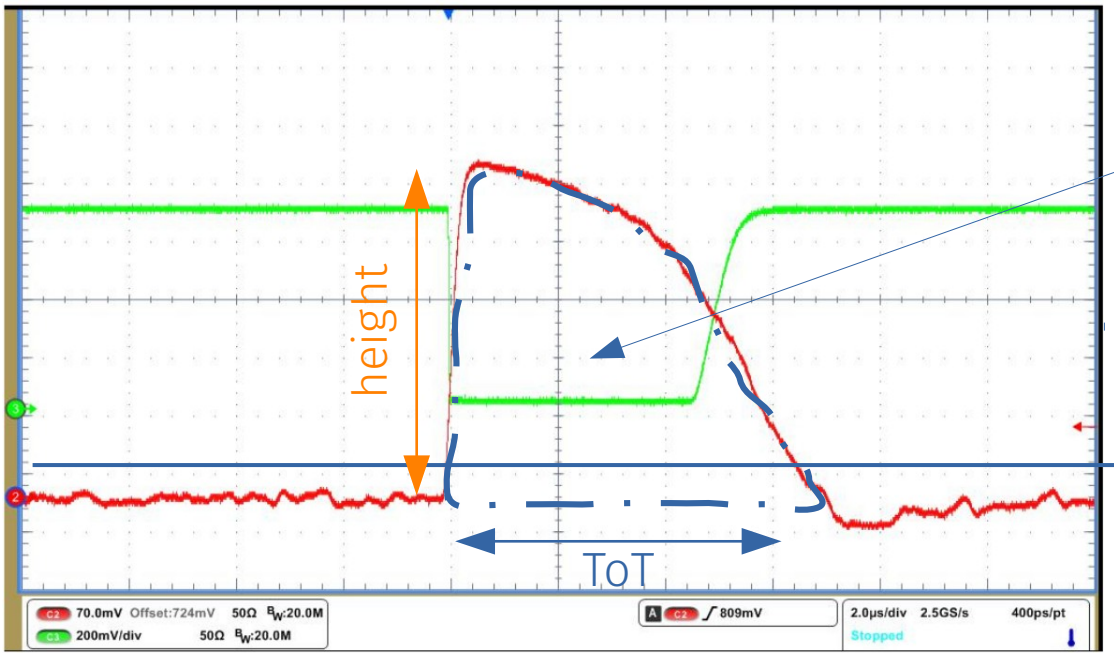


Image credit: cmos - wikipedia

Precisely measuring charge/time

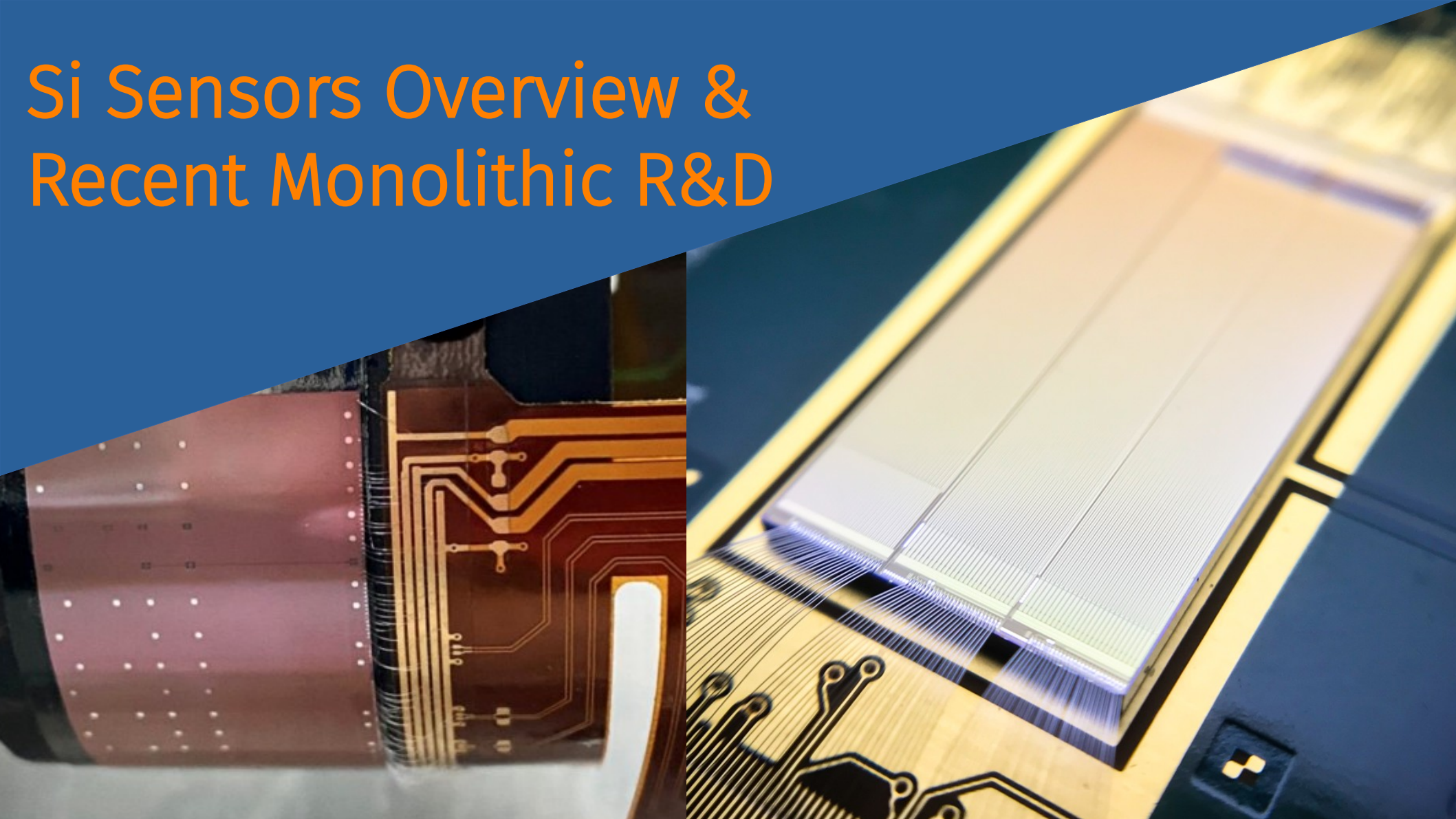
Prcise time measurement: low threshold and fast sampling



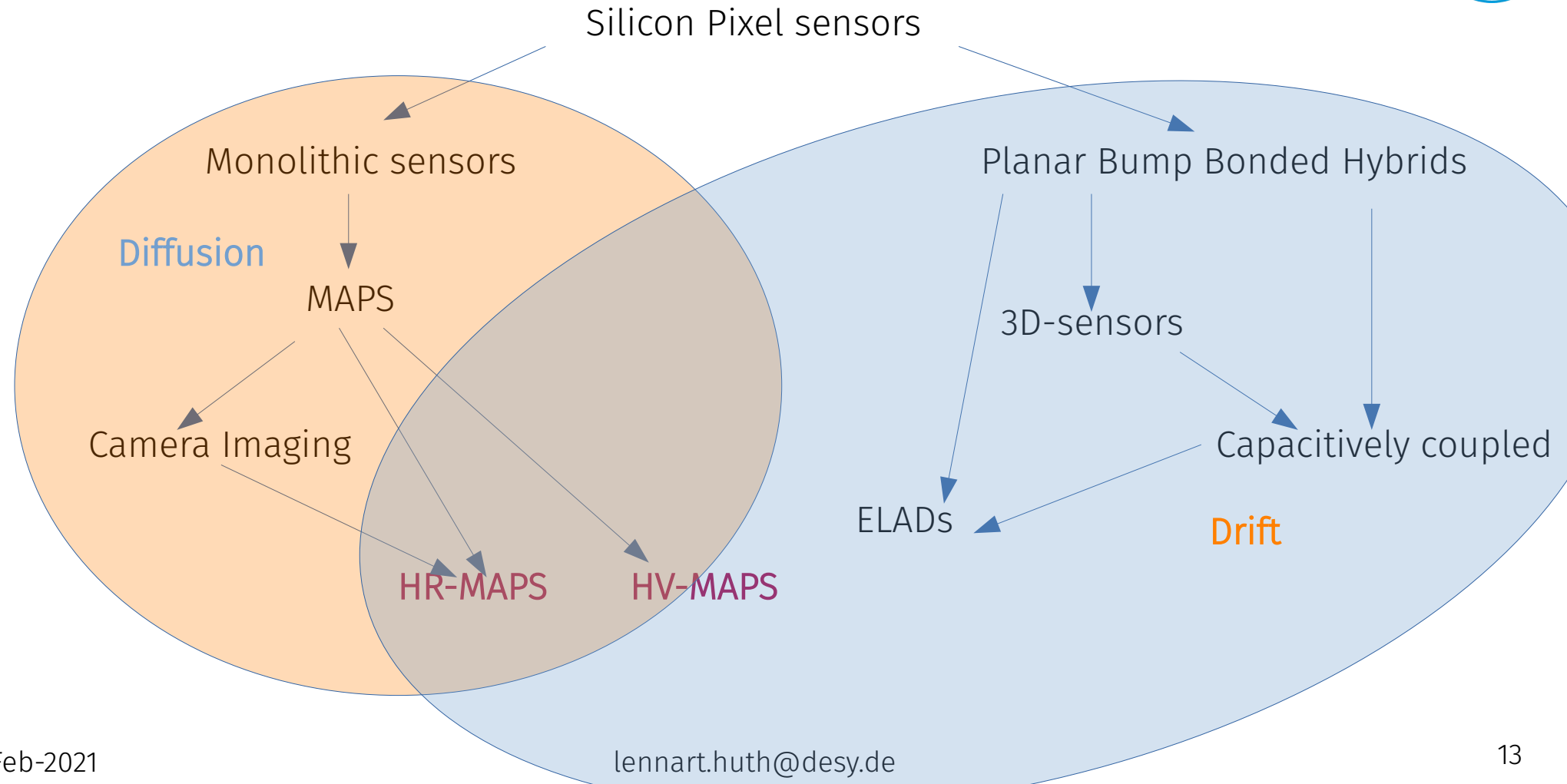
- Full charge integration → complex, ADC on chip is large
- Pulse height → needs also and ADC
- Time-over-threshold → simply sample both edges of discriminated pulse, but noise influenced → no need for much additional logic, but also prone to noise

All above methods have pro and cons, choose depending on target

Si Sensors Overview & Recent Monolithic R&D



Silicon CMOS Sensors Family Tree

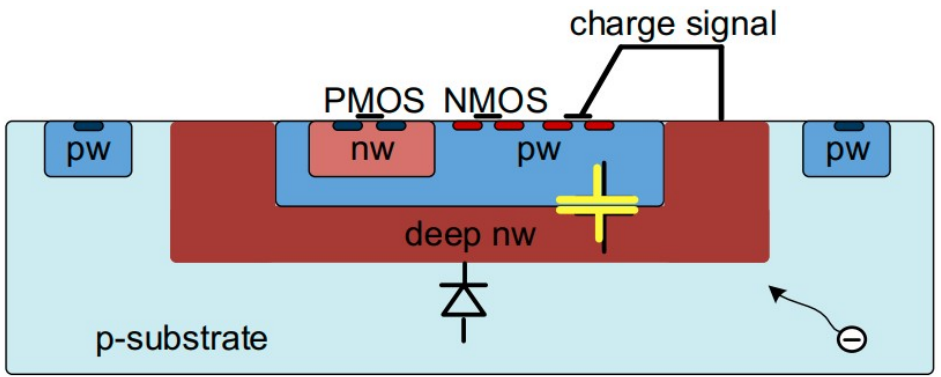


lennart.huth@desy.de

Monolithic sensors

HV-CMOS: Large fill factor

- AMS/TSI 180nm **HV-CMOS**
- Large detector capacity
  - Higher noise
  - Charge sensitive amplifier & higher analog power
- Short drift distances
  - Rad hard
  - Better timing



HR-CMOS: Small fill factor

- TJ 180nm **imaging** process, LF-150nm, GF-120nm,...
- Small detector capacity
  - Lower noise
  - *Simple* voltage amplifier & low power consumption
- Drift distance depends on impact position
  - Less rad hard
  - Timing worse

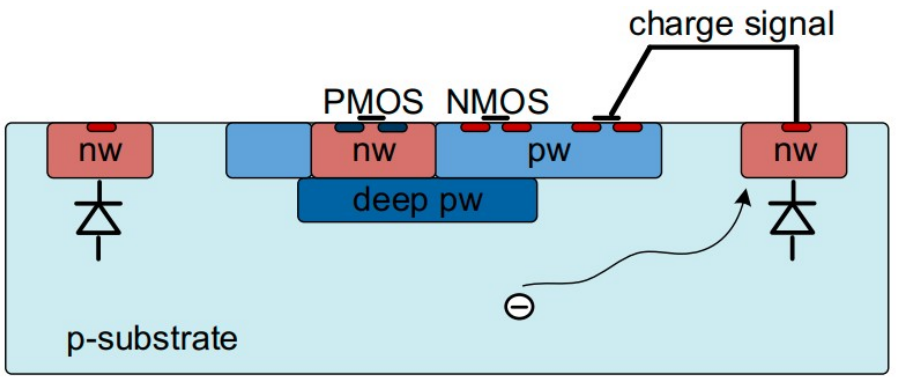
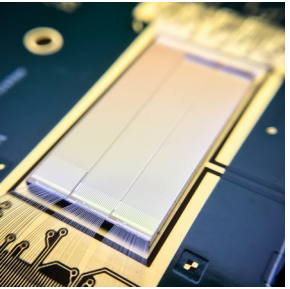
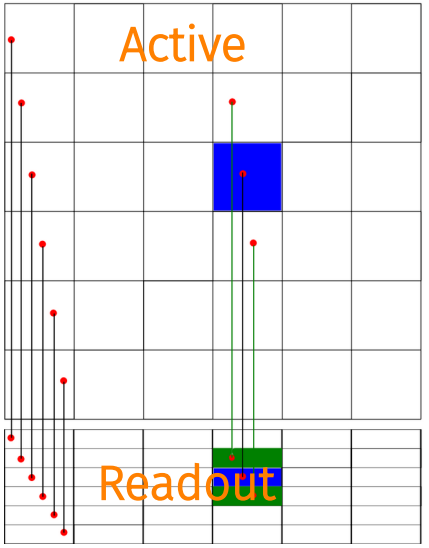


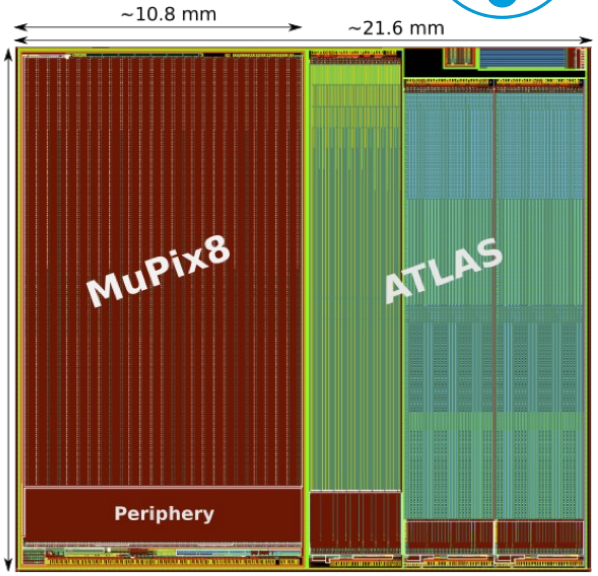
Image credit: N. Wermes

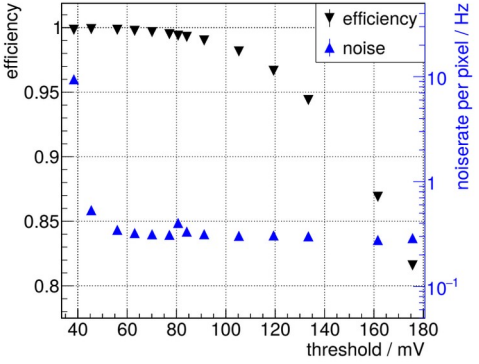


MuPix/ATLASPix Family

- AMS/TSI 180nm HV-CMOS
- Developed at KIT by I. Peric
- Large number of sensors available.
- Column drain readout architecture with partner cell in periphery
- 99.9% efficient, time res <5ns, radiation hard
- Zero suppressed self triggered readout state-machine



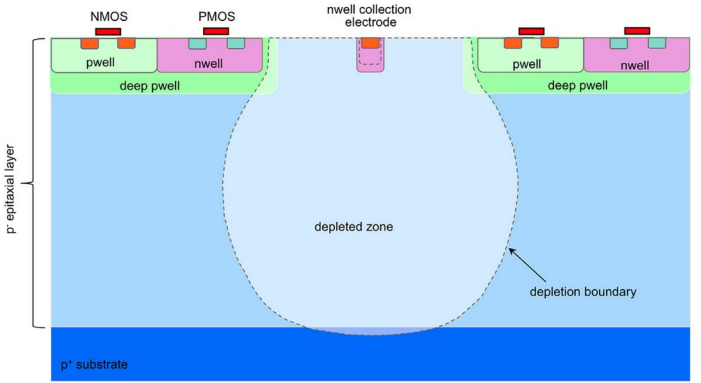




lennart.huth@desy.de

ALPIDE/Monopix Family

- TJ 180nm & LF 150nm
- Small collection diode
- Process modification to improve depletion
- Low analog power consumption
- Rad hard. Tricky, but realized with pCz substrate



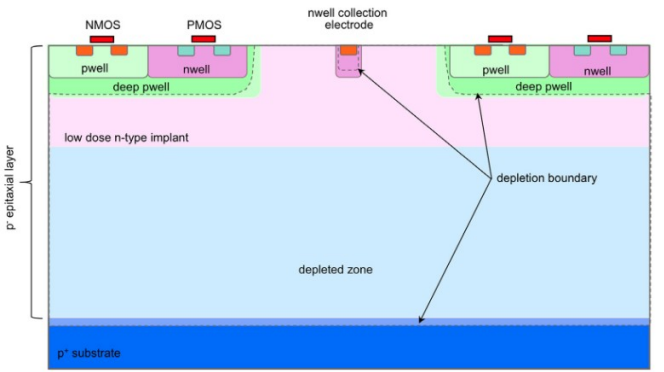
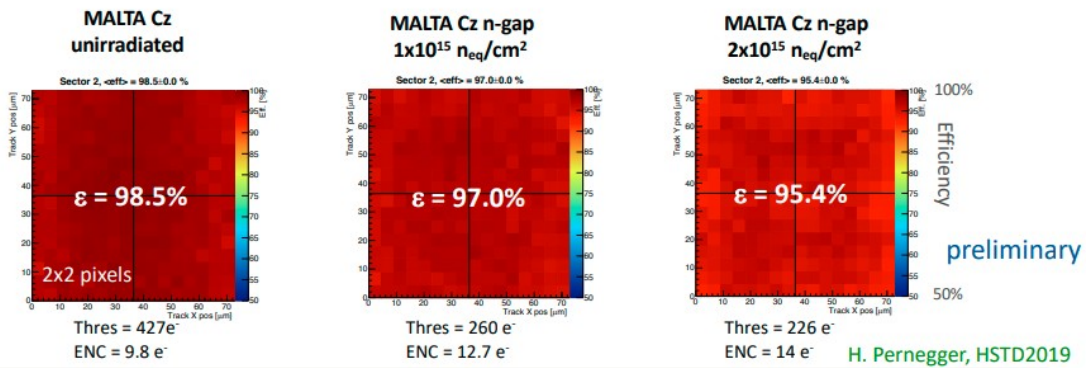
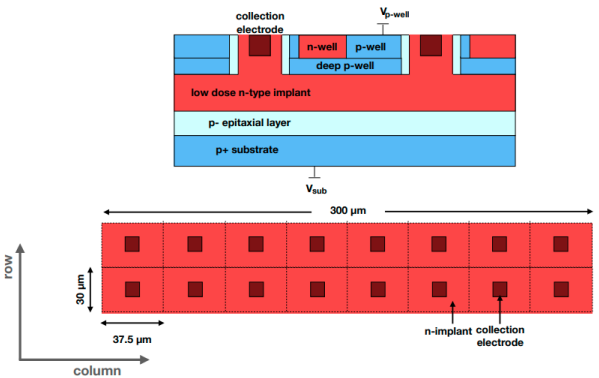


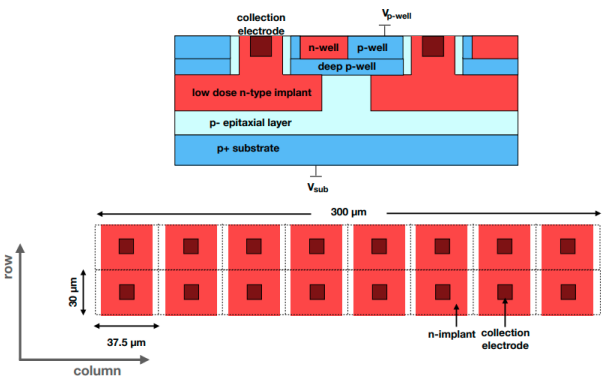
Image credit:
A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance

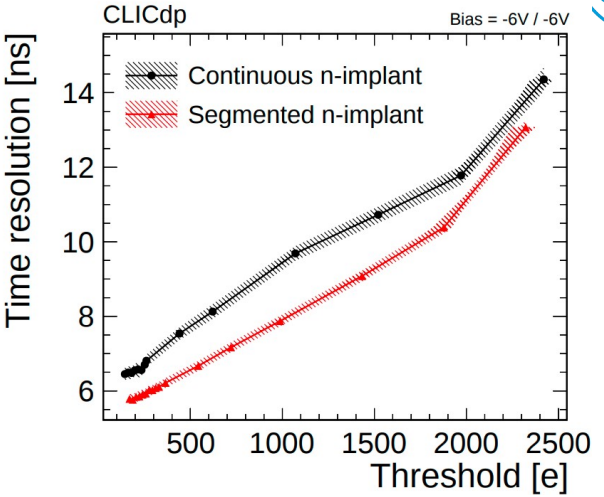


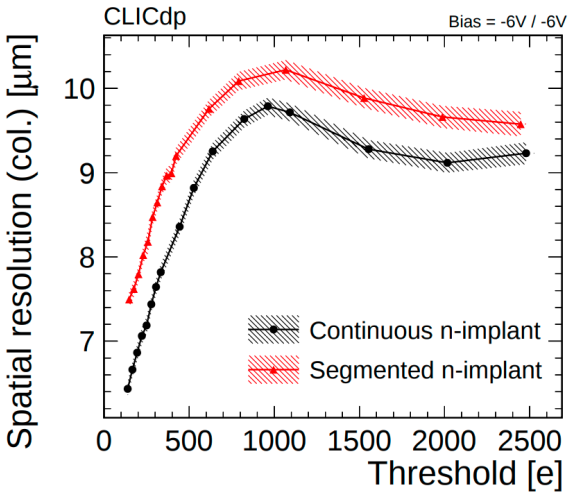
Time Resolution in fine pitch

- CLICTD sensor study in TJ180nm
- Add a trench to the n-type blanket
- More charge in a single pixel
  - → faster threshold crossing
  - → better timing
  - → But spatial resolution is reduced
- Spatial resolution reduced







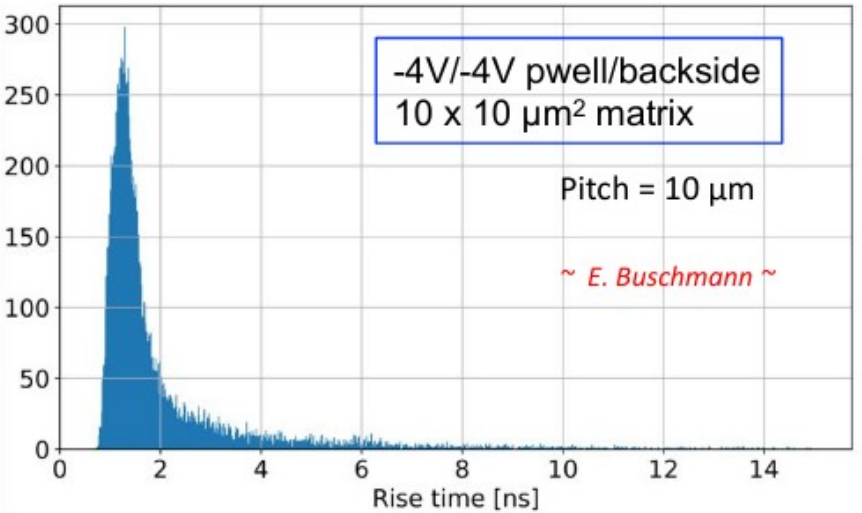


lennart.huth@desy.de

Going even further - FASTpix

- Up to now: Trade between lateral field and detector capacitance
- Detailed TCAD/Monte-Carlo studies to test the concepts before submission
- Hexagonal pixels → less charge sharing → faster & more efficient
- Optimization of deep n-well shape
- Rise times below 1 ns even for a 10um pitch sensor
- New challenges on readout speed/ on-chip TDCs
- CERN Detector Seminar, M. Munker

Rise time distribution measured with source, FASTpix re-optimised process:



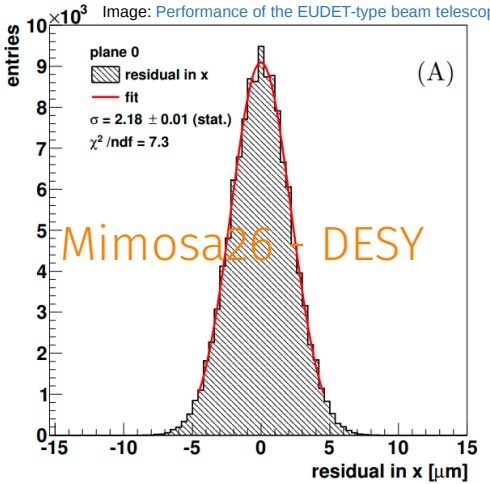
Position Resolution

- Brute force method:
  - Reduce pixel size, but
    - More channels
    - Less space for electronics
    - Higher power consumption
    - Larger clusters → higher hit rate
- Precisely measure deposited charge
  - Pulse-height/ToT
  - Full waveform readout?
  - Lower detection thresholds
- Charge deposited by particle in narrow cylinder around trajectory

  → Drift collection, barely any chance for larger clusters in planar like sensors

  → Optimizing the E-field for charge sharing, the **E**nhanced **La**teral **D**rift concept (Jansen, Velyka, Spannagel) also for monolithic CMOS sensors?

  → Optimizing n-blanket layer to optimize charge sharing



Current developments have pitches down to 30um
→ Not sufficient to reach resolution of MIMOSA-26

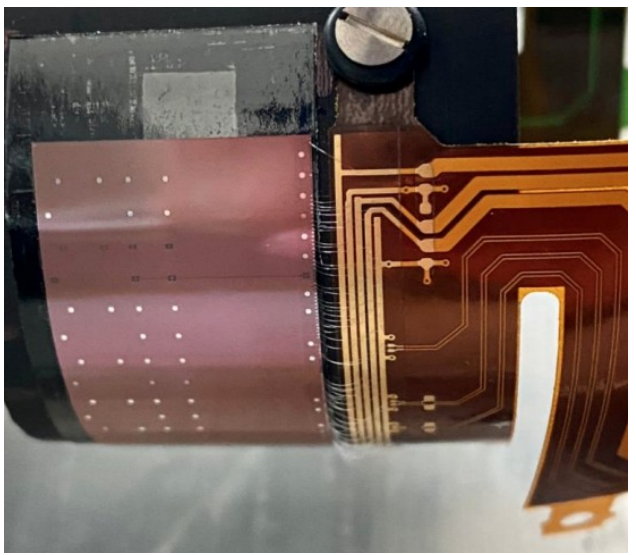
Consider moving to a more diffusion based sensor with a very thin depletion layer → the power of interpolation.

But this would be again rather slow.

Material Budget

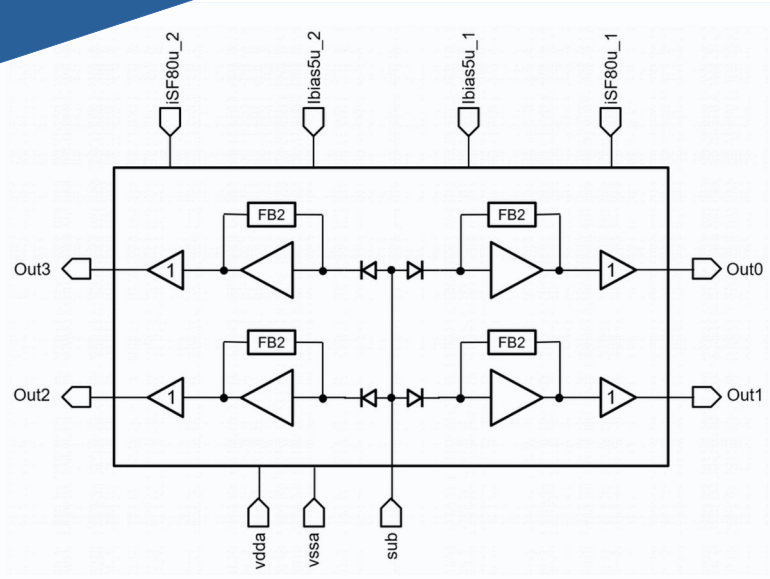
- We cannot do much about the density of silicon:
  - → Reduce thickness,
    - 50um is a *standard*, how far can one go?
    - Less active depth
    - Less charge to collect
- Further increases the need for low noise/high amplification readout circuitry
- Crucial for future vertexing detectors
  - → Monolithic approaches

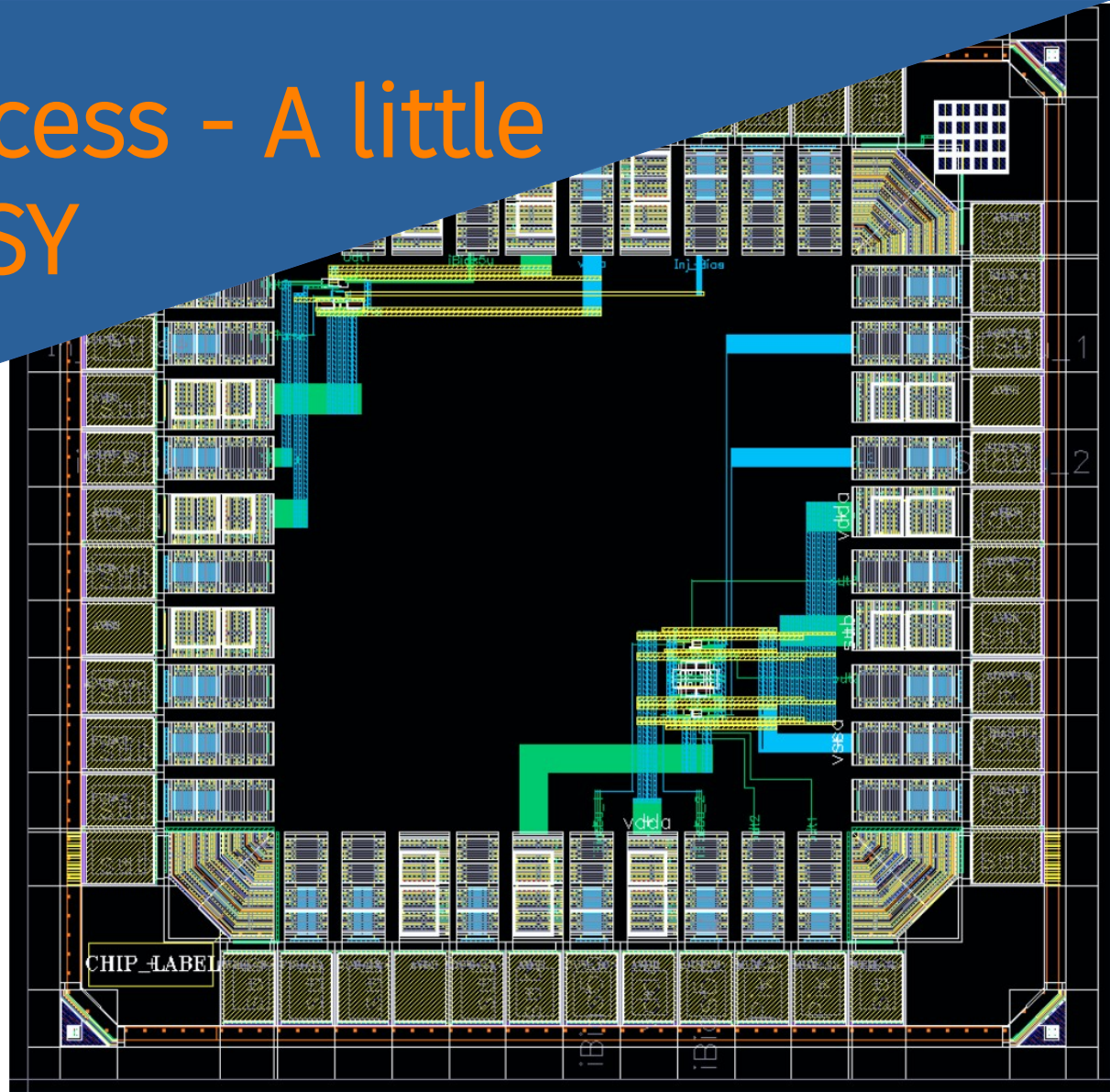
- Reduction of support material
  - → wafer sized chips/stitching
  - → ALICE ITS3 concept



Image

65nm imaging process - A little bit of future at DESY





From 180nm to 65nm

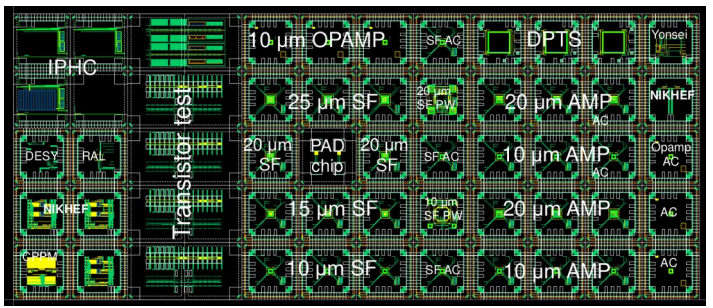
- Higher logic density possible → more on chip intelligence (at least factor 4 for our porcess)
- New process → long lifetime & support
- Reduced power consumption → less cooling required (1.8V → 1.2V)
- Smaller structure intrinsically more rad hard.
- Demanding requirements by CLIC, ILC, FCC hard to match with current technologies
- Digital logic will become more complex: Power pulsing, data compression, clustering on-chip,...
- CIS-processes required to deplete active volume

But:

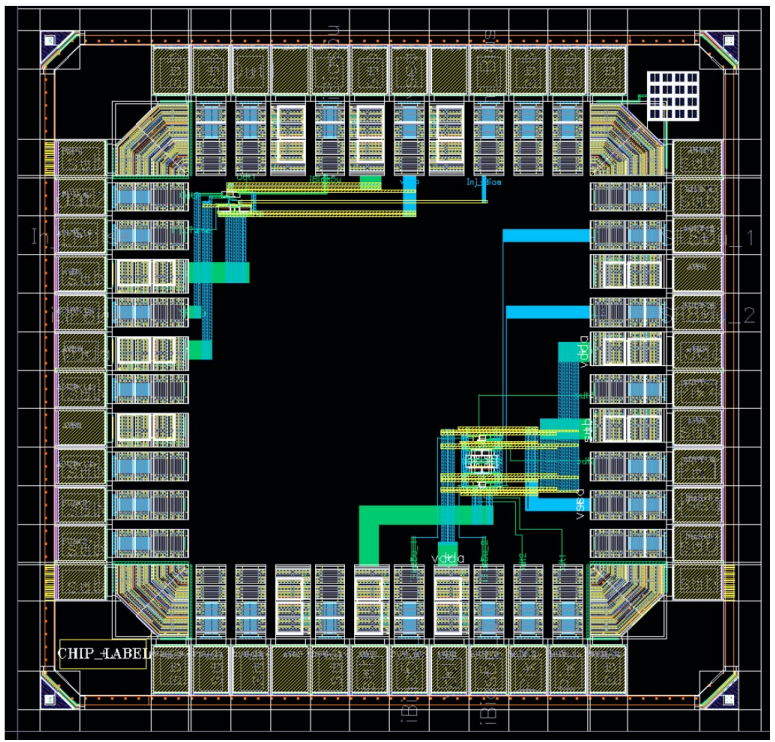
- Completely unknown process
- Cutting edge technology → process still in development
- Rather expensive
- Need to start from scratch:
  - Test uniformity within chip
  - Predictability
  - Is the production reliable
  - What's fraction of issued chips
  - How much can we manipulate the process to fit our needs
  - Very basic transistor tests

Design Status

- First test chip is designed (C. Reckleben/FE)
- First custom CSA in this technology
- 4 pixels, Pitch 16um
- Already in production, Expected back this summer
- Small part of shared run with:
  - Transistor test structures,
  - Analog test pixels
  - Rolling shutter matrix
  - Front-end amplifiers
  - LVDS signaling tests
- Readout system in development: Caribou DAQ system with custom chip board (Work in progress)



1.22mm



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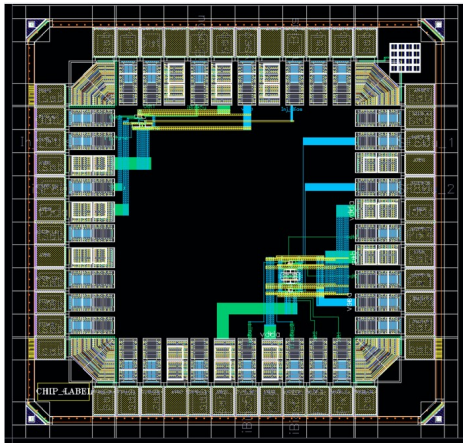
lennart.huth@desy.de

Take away



- CMOS sensors will be a key technology for future trackers
- Demanding requirements cannot be matched with existing pixel sensors
- A lot of research ongoing
- ELADs & 65nm developments at DESY
- Moving away from simply scaling to process engineering & system-on-chip concepts
- Simulation studies more and more important
- Many topics not included

There is not (yet) one solution for all challenges and improving one parameter typically trades another one.

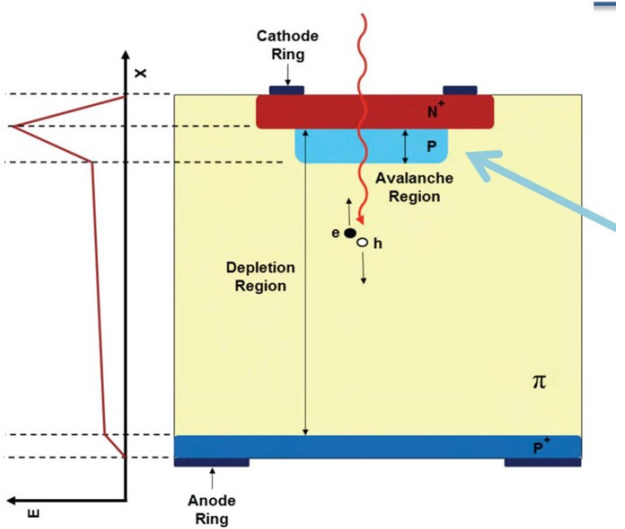
Backup

Time resolution

$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{Jitter}^2 + \sigma_{TDC}^2$$

Can be optimized for any CMOS sensor

- Bichsel/Landau-Vavilov flcutuations limiting resolution
- Need to be sensitive to the very first electrons collected
- Adding an avalanche layer close to collection electrode
- “LGAD”-principle
  - Current status/details would be a topi of itself, maybe another presentation i this forum?
  - A few 10 ps possible



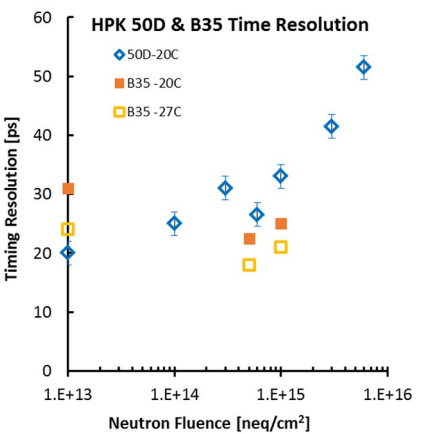
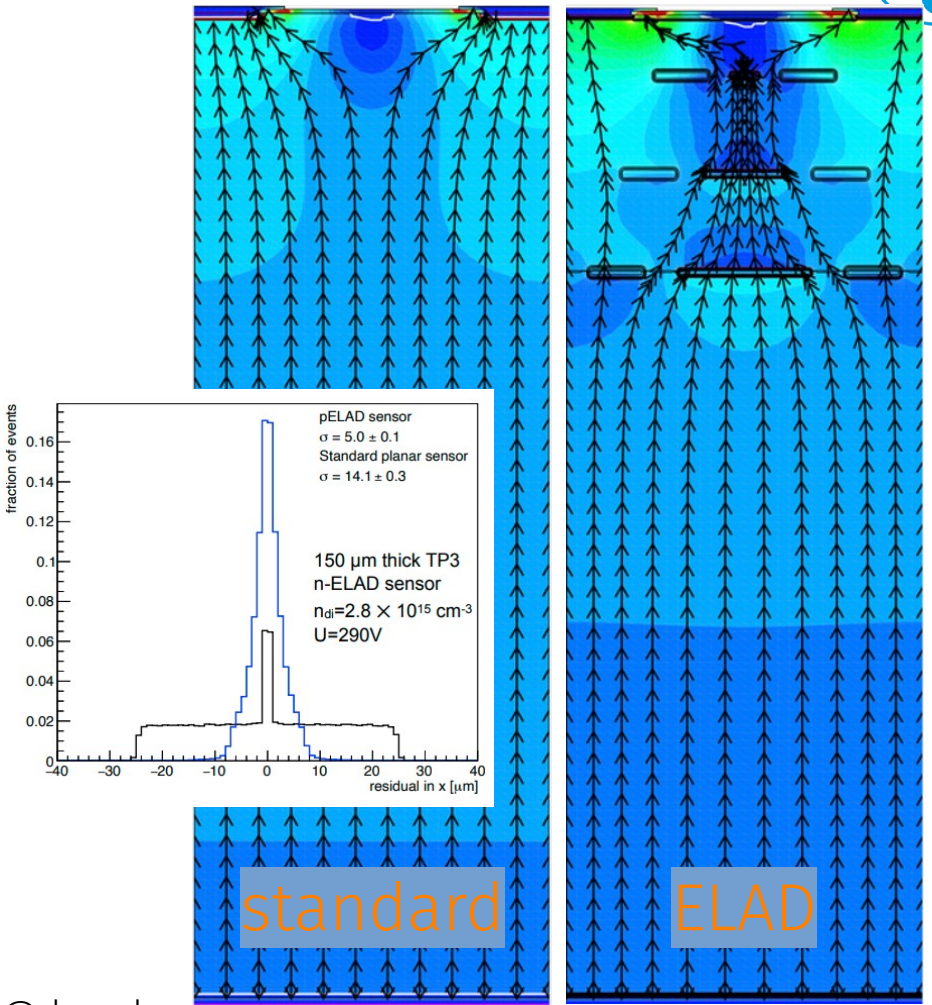


Image credits: Hartmut F-W Sadrozinski

Hybrid sensors I - ELADs

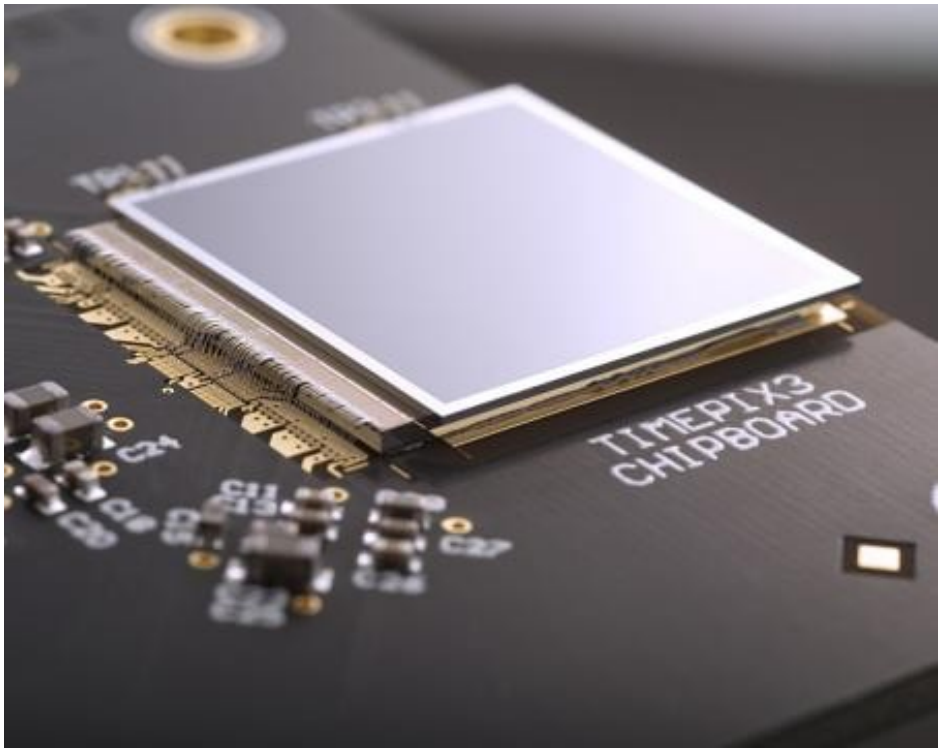
- Enhanced-LAteral-Drift (ELAD)
- Actively enhancing the charge sharing between 2 pixels, by manipulating the sensors bulk
  - Ideal scenario: Linear dependence of charge sharing between two pixels
  - Improves resolution without penalty of high channel and hit counts
- Extensive simulation studies with TCAD/Allpix2 proof feasability
- No sensors yet
- Concept can be connected to any readout ASIC that matches the pixel pitch → highly flexible
- Developments by **Hendrik Jansen**, **Anastasiia Velyka** and **Simon Spannagel** @ DESY



Hybrids

Timepix4 (just an example)

- 200ps time resolution
- 55um pitch
- 256x256 pixels
- < 500 Mhits/s
- 20.48 Gbit/s data rate
- ToT with energy resolution < 1keV
- Significantly more complex as monolithic sensors at the moment.



Collecting charge

- P and N doped silicon in contact
  - → Depletion region, increased with a bias
  - → strong electric field
  - → Extension of depletion zone depends on relative doping concentration

- **Signal** is induced by motion of e/h paris.
  - Two types of particle motion:
    - → **Drift**: Along the electric field lines, fast
    - → **Diffusion**: Temperature dependent random walk with ~ 100nm free path length
- Signal formations completed when all charge **reaches electrode** or **recombines**.