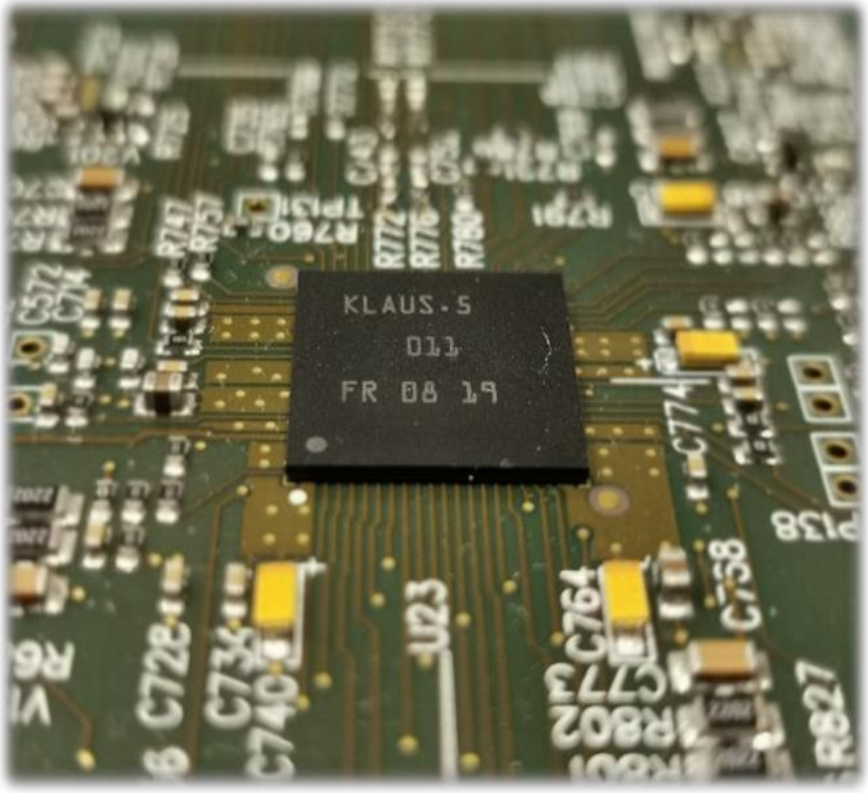
BMBF Scintillator R&D // CALICE AHCAL
Heidelberg status report



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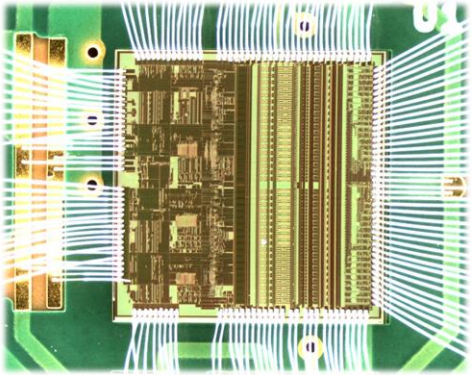
Main developments

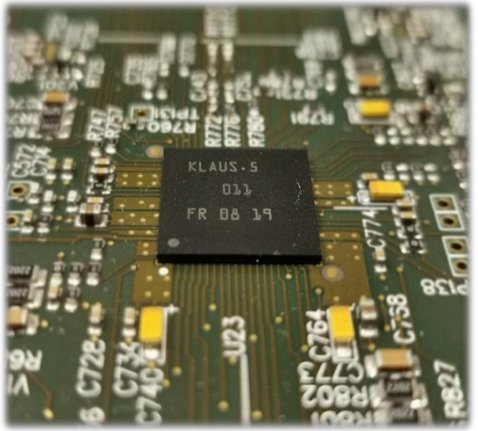
Development of readout electronics

- KLauS ASIC design
- Packaging
- Characterization & Test beam measurements



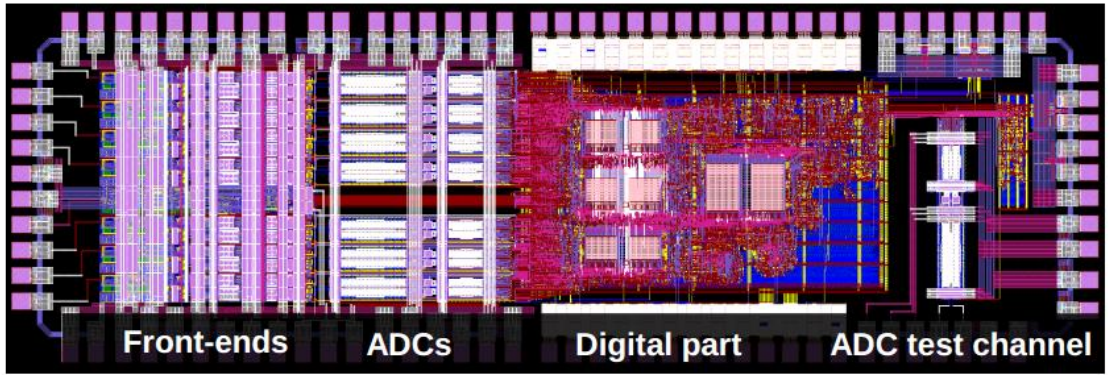
HBU with KLauS

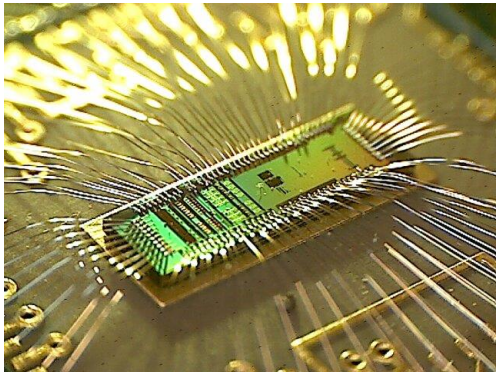
- DIF Firmware developments
- Software for Control & ASIC configuration
- Standalone DAQ & EUDAQ Integration



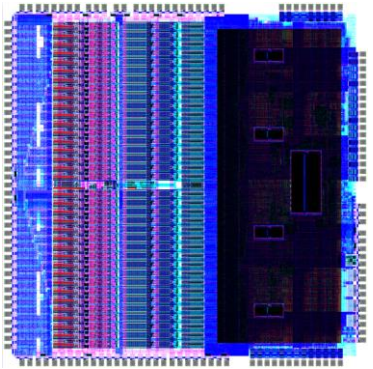
KLauS ASIC development

7-channel KLauS4 prototype (2016)





- SiPM readout solution developed for CALICE AHCAL & ScECAL
- Target low gain SiPMs (10µm pixel, ~1mm² area. Charge range 15fC – 150pC)
- UMC 180nm mixed-mode CMOS technology
- Low power, Power pulsing capable (~25uW @ 0.5% duty cycle)
- Current version KLauS6 with 36 channels
- Analog front-end + ADC + TDC + Digital circuits



KLauS6 (5x5 mm²)

KLauS6 - The last puzzle piece

Dedicated TDC implemented

- Allows to digitize with required timing resolution.
- PLL at 160MHz (40MHz input clock) generates 16 phases
- → **200 ps / bin**
- Coarse counter extends **dynamic range** to **~15ms**
- Fast lock → Power pulsing capable
- Low power: < 2uW/ch with 0.5% duty cycle

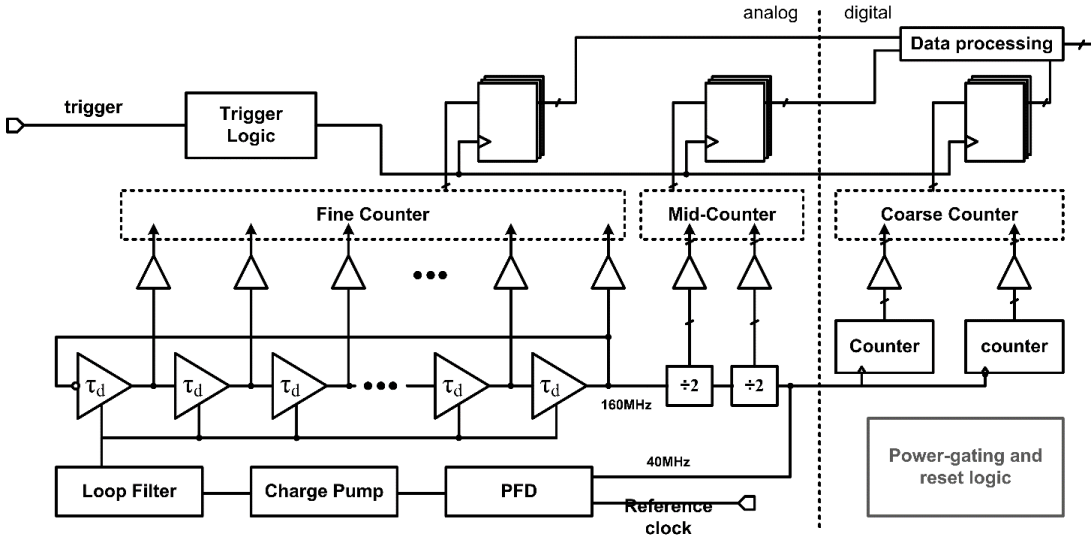
Characterization studies started in Q2 / 20

- Production delayed due to error in production

Measured Time resolution very close to intrinsic limit

Minor digital bugs observed

- TDC data was partially corrupted
- Fixed in recent submission “6b”
- Under test since May

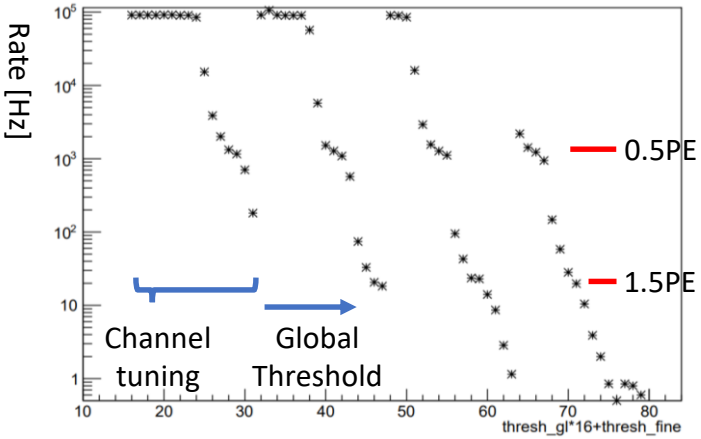


KLauS6b – First results

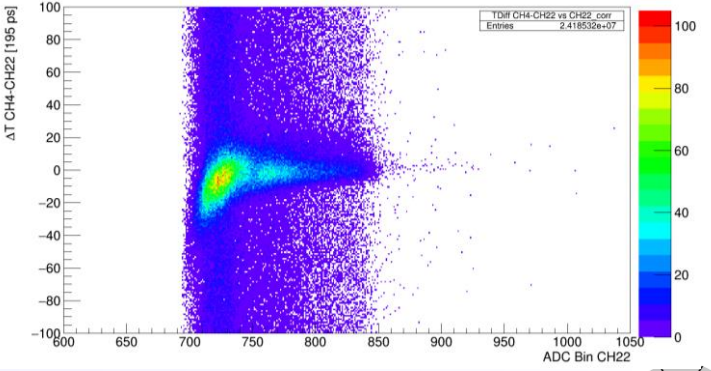
- Lab measurements have shown to cure the found effects
  - Calibration (SiPM bias DACs, hold delays, trigger threshold scans):

    nominal performance as in previous versions
  - Improvements implemented have expected effect (Threshold tuning range)
- Beam time @DESY together with mu3e-tile until Yesterday
  - 2+2 Layers of 25um and 15um MPPCs
  - Focus on time measurement capabilities
  - Timing for MIPs and with Tungsten
  - Power pulsing including TDC
  - Time resolution heavily affected by energy cut and timewalk corrections

Trigger Rate using internal scaler / Threshold adj.

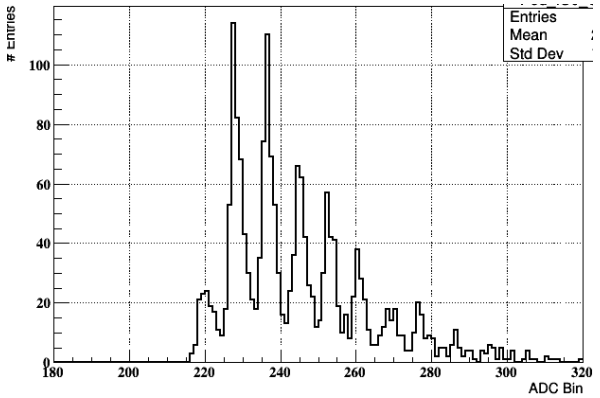


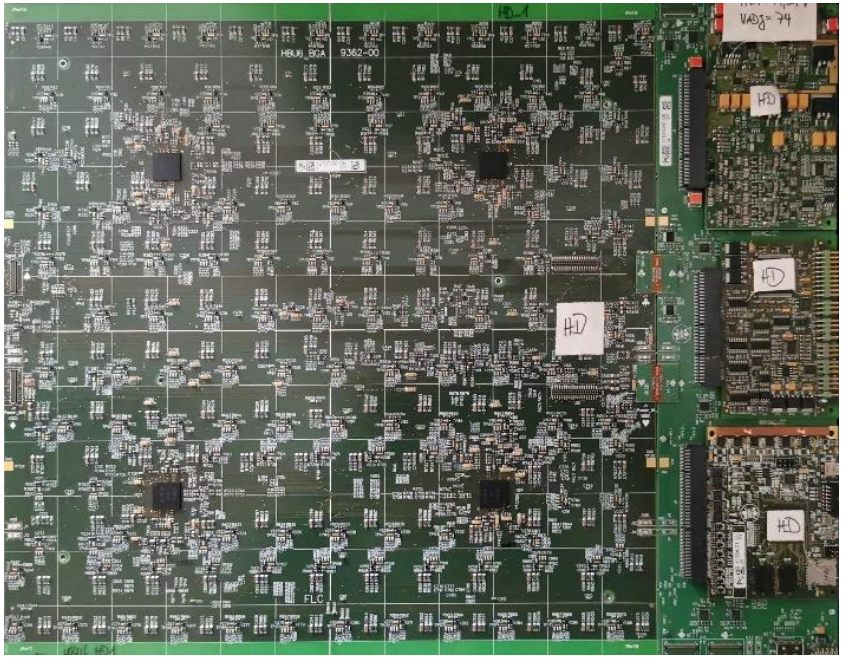
MIPs: Time walk as function of charge



CALICE AHCAL HBU

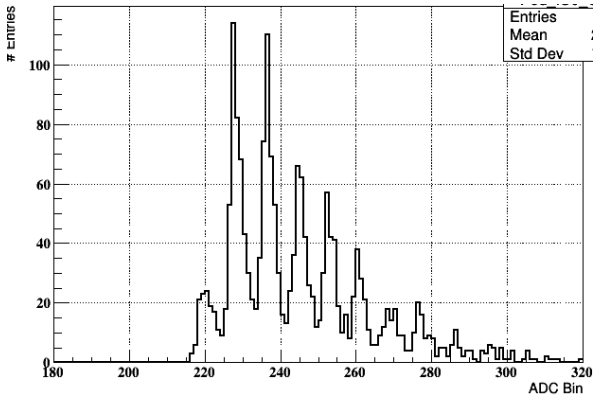
- KlauS5 has been (BGA-) packaged; also KLauS6 is available now
- AHCAL-HBU variant developed by DESY + HD
  - One board with KLauS5 exists, 15um MPPCs equipped
  - Basic functionality was already shown by Zhenxiong & Mathias

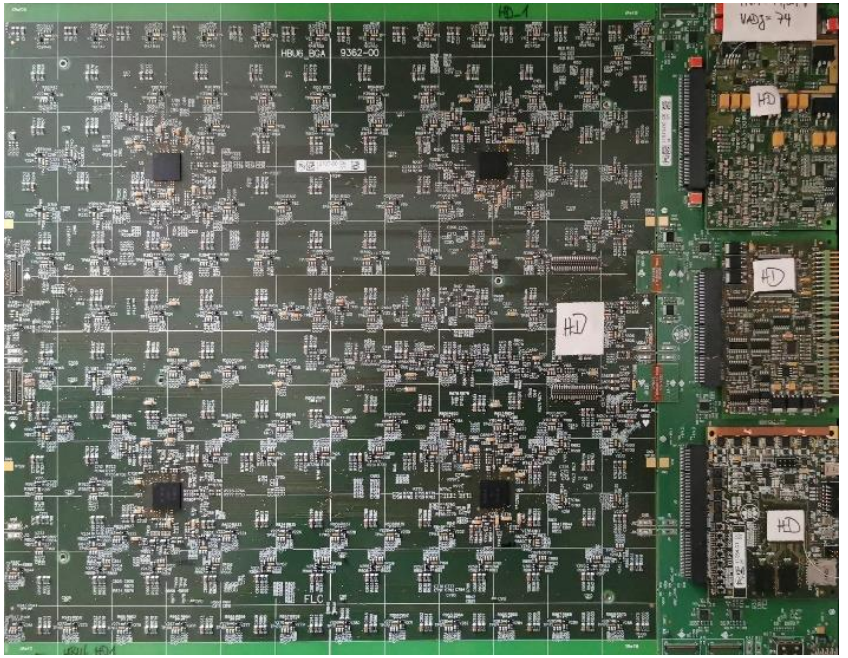




CALICE AHCAL HBU

- Integration of DAQ in full AHCAL system (LDA+CCC)
  - Work on DIF firmware finished, working smoothly
  - Existing DAQ & Software (KIP) adopted for single-board operation
  - DAQ HBU commissioning until full integration is finished
  - also used for ASIC configuration in multi-layer system





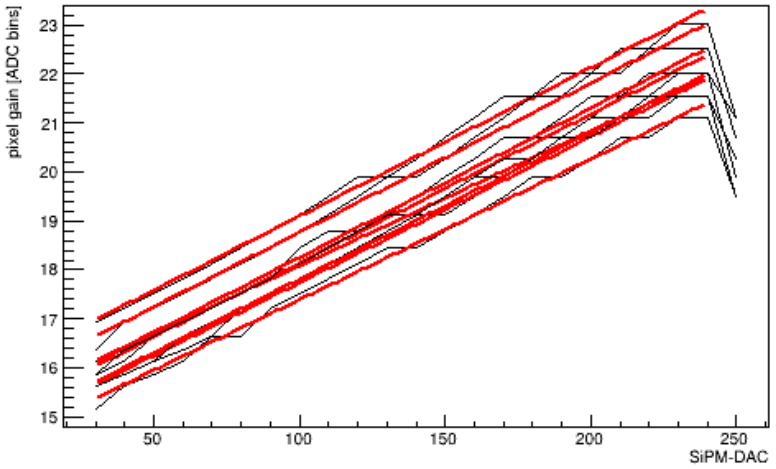
HBU Commissioning

ASIC Parameter Optimization procedures same as single setup:

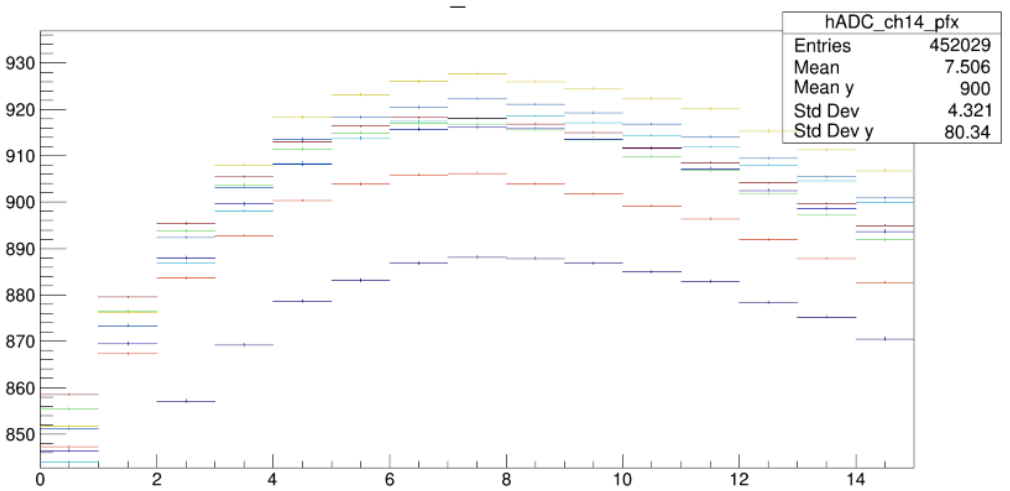
Hold delays, SiPM bias DACs, … mostly automatic processes

Works in beam and with LED-System

SiPM gain adjustment per channel



Hold delay Tuning

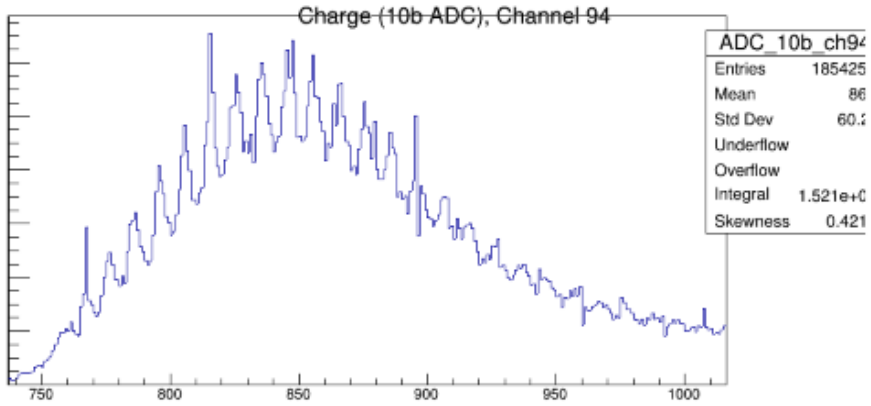


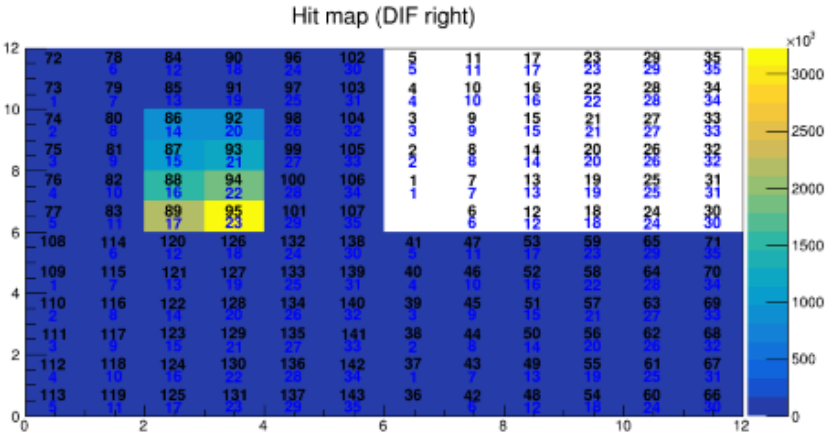
KLauS-HBU at DESY

In beam at DESY until Yesterday

- One KLauS5 HBU, one Spiroc2E HBU *Thanks to Jiri and Katja for the support
- Data taken with standalone DAQ
- Common runs with both HBUs, Synchronized by CCC and common LDA

- EUDAQ can read the data! Event building will be done next
  - Stable data taking with two HBUs over ~14 hours -> Data to be analyzed



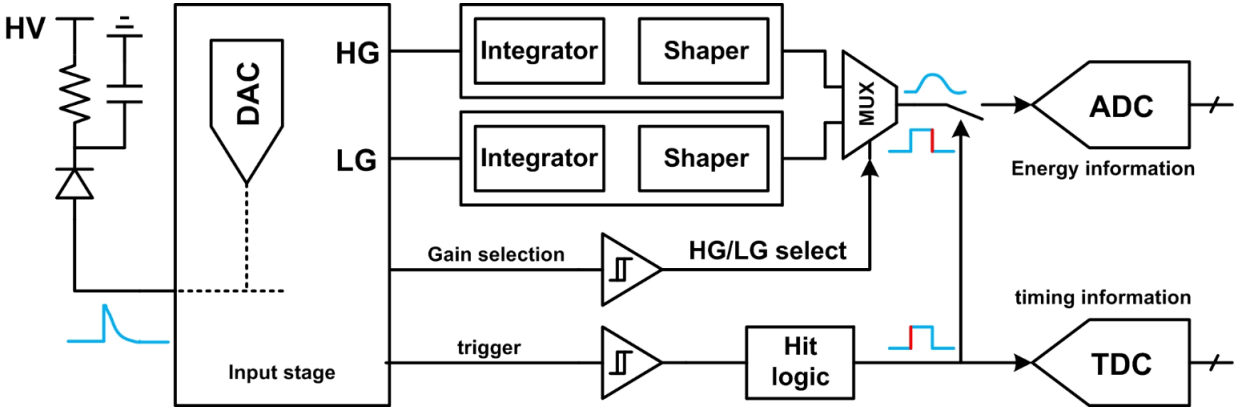


Summary

- Major developments on the KLauS-Chip
  - All required blocks implemented and working nicely
  - Development: (Close to) final version
  - KLauS5 & 6 are BGA-packaged, KLauS6b planned -> Mandatory for HBU integration
- KLauS-HBU
  - Currently one HBU with KLauS5
  - Board tested and working
  - DAQ Integration for standalone setup and common running with CCC+LDA

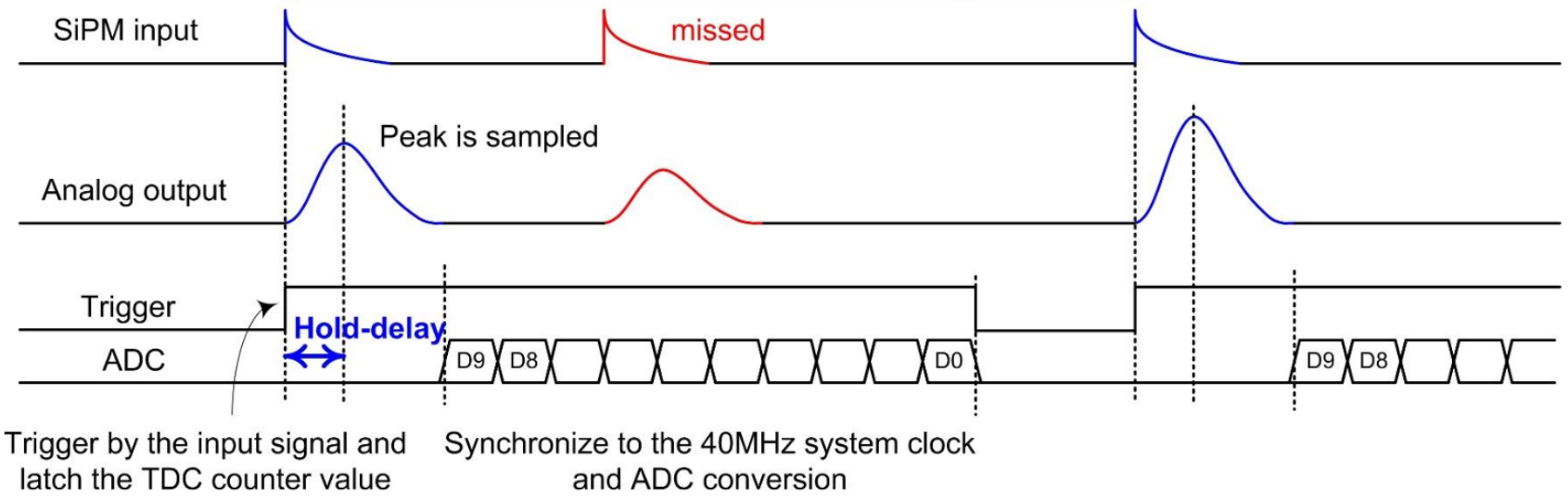
- KLauS6b and the HBU have been tested in beam – Promising first looks into data.
  - We plan to build more HBUs with KLauS6
  - AHCAL Technical prototype, dedicated timing test-beams with HBUs,…
  - Work on software integration for analysis is needed

KLauS Channel – building blocks



- Input stage → Buffer & distribute signal current, SiPM bias voltage tuning (~2V range)
- 2 integration branches → Different charge range (HG, LG)
- 2 comparators blocks → Timestamp & ADC start, charge range selection (auto-gain)
- SAR ADC
  - **10-bit** mode – SiPM spectra for 25µm pixels and above; MIP quantization
  - **12-bit** ADC – Single pixel spectra for small gain SiPMs (pipelined 8b SAR stage)
- TDC for time stamp recording
  - Since KLauS6: ~195ps bins , ~13ms dynamic range (nominal input clock 40MHz)

Hit digitization



Conversion started after time-comparator fires

- Sample time stamp in TDC latches
- Configurable hold delay (~100ns) to sample peak
- ADC conversion, gain bit sampling
- Busy released after conversion is finished, ready for new hit → typical dead time ~500ns (10b ADC mode)

Full chain: Automatic-gain selection

Full chain (Front-end + ADC) linearity measurement using 10-bit ADC

Combine data from HG and LG branches

- HG: small dynamic range, high resolution
- LG: large dynamic range, lower resolution

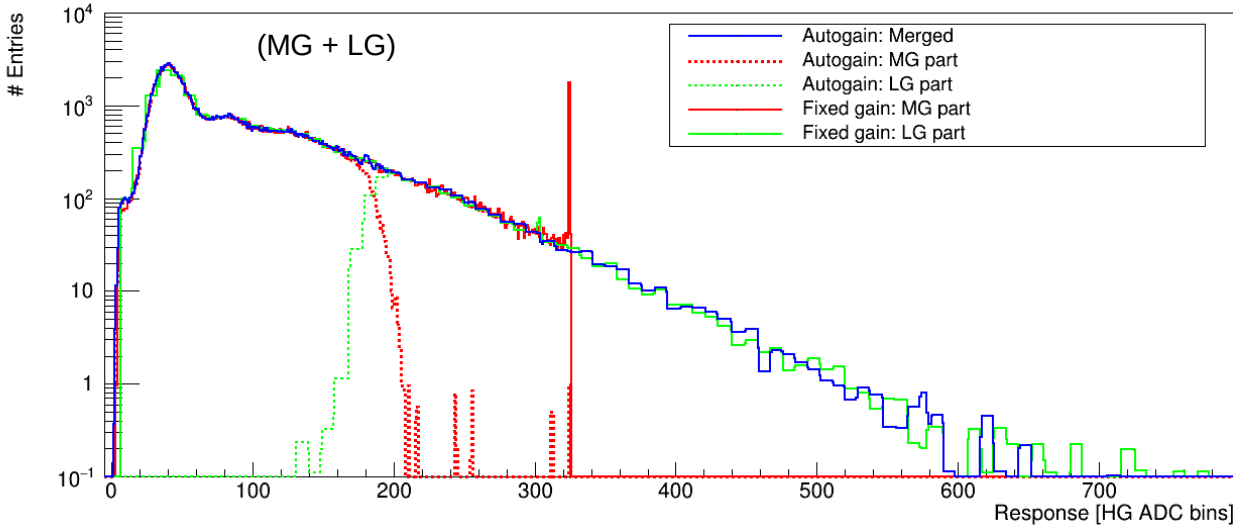
Merge using gain selection bit

Intercalibration factor determined from response in overlapping region – not inferring linearity

Similar method can also be exploited using response to MIPs

INL deviations << 1% FSR

Electrons at DESY: Auto-gain mode & Individual contributions



KLauS6 testbeam setup

Single wire-bonded KLauS6b chip on testboard

Raspberry Pi readout

HBU-style LED system for calibration

In total four layers equipped, two species:

- 15um & 25um pitch MPPCs
- 3 Tiles mounted on each Layer
- Tungsten absorbers for some runs

Setup for DESY test-beam