Prototype Design of Timing and Fast Control in the CBM experiment

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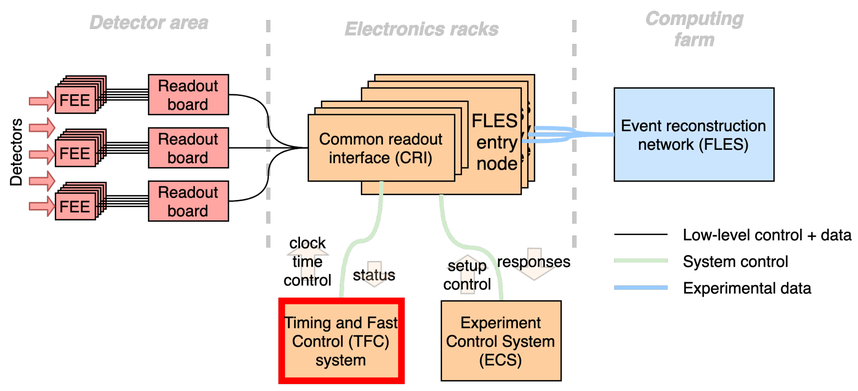
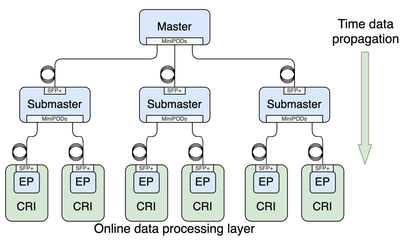
1. Data Acquisition System



- **GBTx**-based readout
- **Self-triggered** front-end electronics
- **1 TB/s** data stream from FEE to FLES

- CRI boards mounted as **PCIe** cards
- **Free-streaming** data processing
- **Online** event reconstruction

2. Timing and Fast Control



TFC mission:

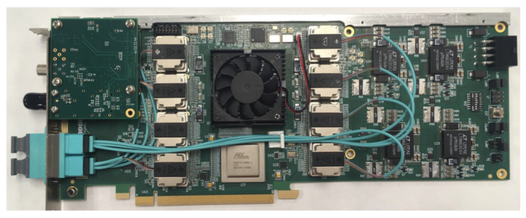
- **Distribution** of a 40 MHz **system clock** to data acquisition electronics
- System-wide **time synchronisation**
- Latency-optimised deterministic **data transmission** path for fast control

System highlights:

- Master and Submaster nodes support **up to 48 and 47 downlink connections** respectively
- Three **node classes**: master, submaster and endpoint
- TFC nodes are interconnected with **4.8 Gb/s optical links**
- **Transport clock - 120 MHz**
- **64-bit timestamp** counters

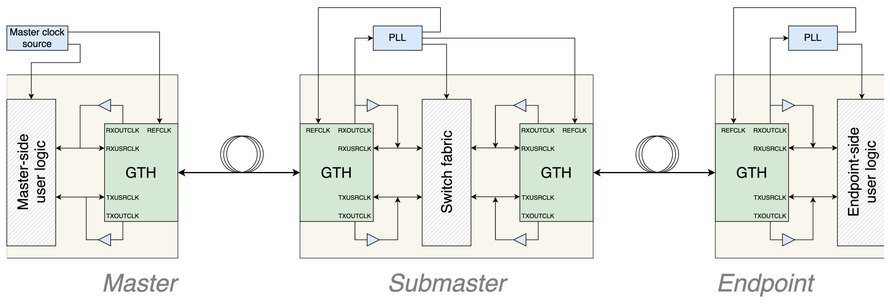
3. Hardware platform

FPGA board: BNL-712, TTC-PON mezzanine



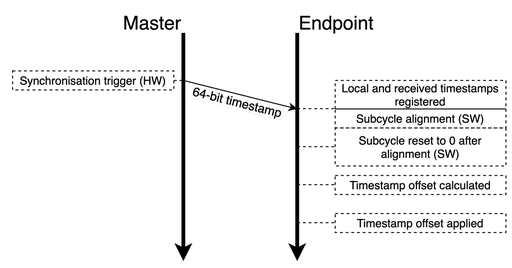
- Xilinx Kintex UltraScale **XCKU115** FPGA
- **48 optical links** (MiniPOD, SFP+ (mezz.))
- **Si5345** MGT-enabled jitter-cleaning PLL
- **PCIe** Gen-3 16-lane

4. Clock distribution



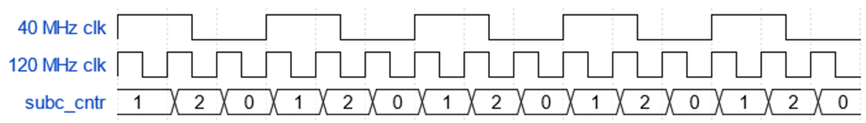
- System clock is propagated across the network in a **cascaded** fashion
- Each non-master node **recovers** clock from the incoming optical link
- The recovered clock is **forwarded to** the hardware **jitter-cleaning PLL** (Si5345)
- Jitter-cleaned clock is **reused** for optical **transmission** and as a **local system** clock

5. Prototype time synchronisation scheme

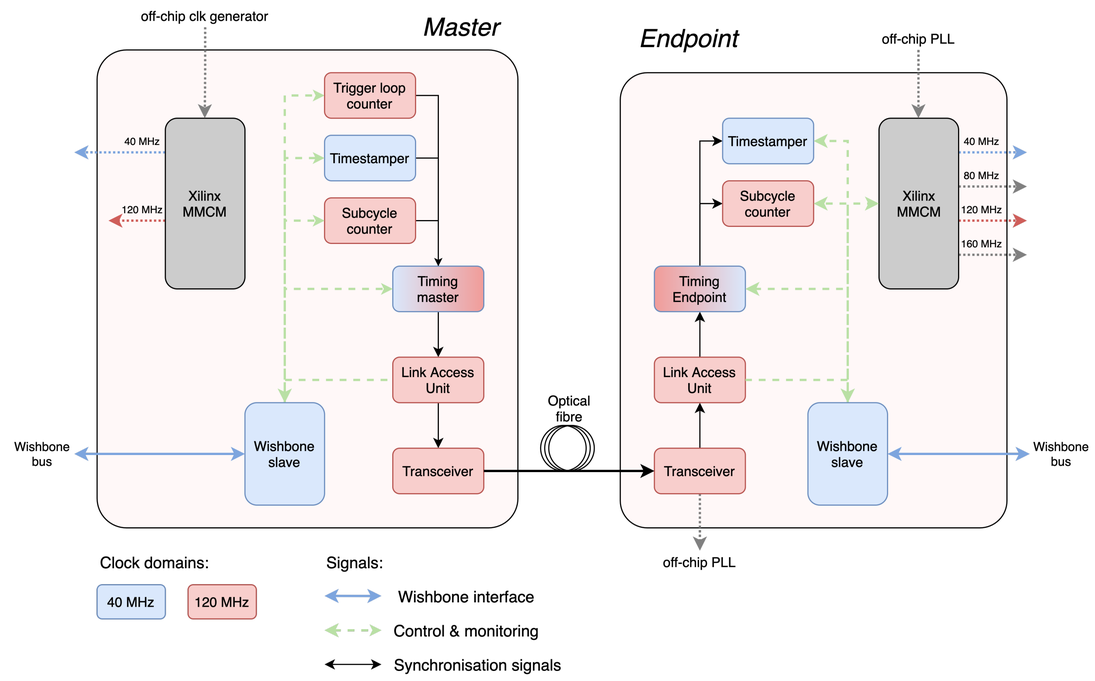


- System reference timestamp is periodically **broadcast** by the master node
- Endpoint calculated **relative** time offset
- Local 40 MHz system clock is **aligned** with the first received frame
- Clock phase and time corrections are **offloaded to software**

- Position of 40 MHz clock edge is recovered using a subcycle counter
- Start of the received reference message marks the system-wide subcycle 0



6. FPGA core architecture



Master core:

- 64-bit timestamp is transmitted with 1 ms period
- Transmission starts on subcycle 0
- Transmission period is configurable from 1 μs to 35 s

Endpoint core:

- Various user clocks are generated and phase-aligned
- Generated clock phase is configurable with 18.6 ps steps

Common features:

- Low-level link initialisation and fault recovery (hot-plug)
- Link status is monitored over Wishbone
- Rx and Tx clock domain crossings are implicitly handled by the Link Access Unit
- Link access prioritisation for future fast control

7. Prototype setup

- Forward timestamp propagation scheme
- 120 MHz TFC transport clock, 40 MHz experiment-wide system clock
- Cascaded clock propagation scheme
- System clock synchronisation with a subcycle counter
- Extensive integration tests to start in July