The Caribou Readout System for Pixel Detectors

Fortnightly SiDet R&D Meeting
24 March 2021

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Motivation

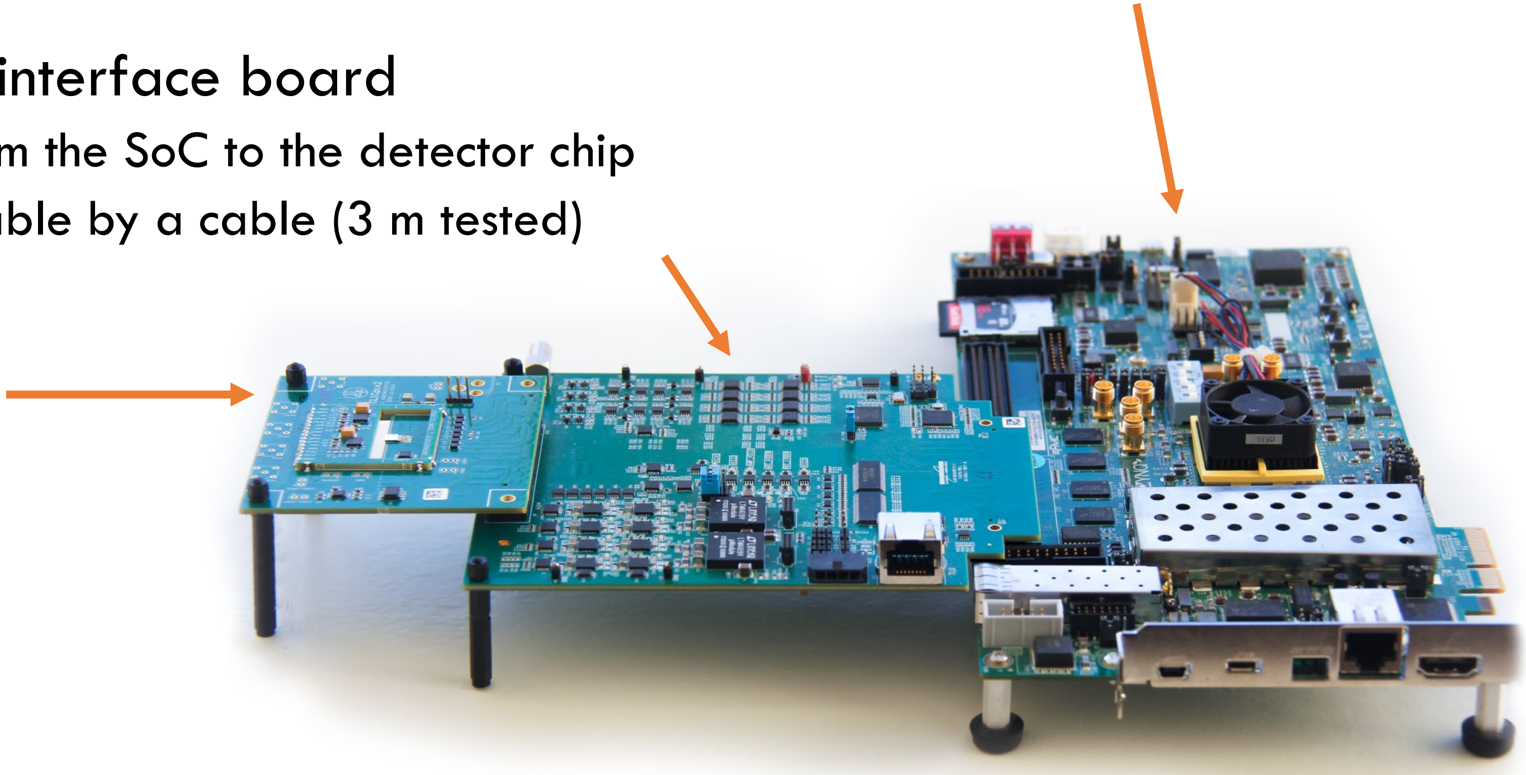
- A similar concept of readout, control and power is used in most silicon pixel detectors
  - Differs in voltage levels, number of channels (data/voltage) or protocol
- A new detector-specific DAQ system is usually developed for each new detector (or an existing one is modified)
  - Time-consuming process of HW/FW/SW development
  - No innovative functionality
- A versatile DAQ system can speed-up development
  - Common HW and SW core and interface
  - For detector development and tests

Caribou

- Open source hardware, firmware and software for laboratory and high-rate beam tests
- Maintained by collective effort of developers from:
  - Brookhaven National Lab
  - CERN
  - DESY
- Minimizes device integration effort
  - Reduces time to get first data from a new detector

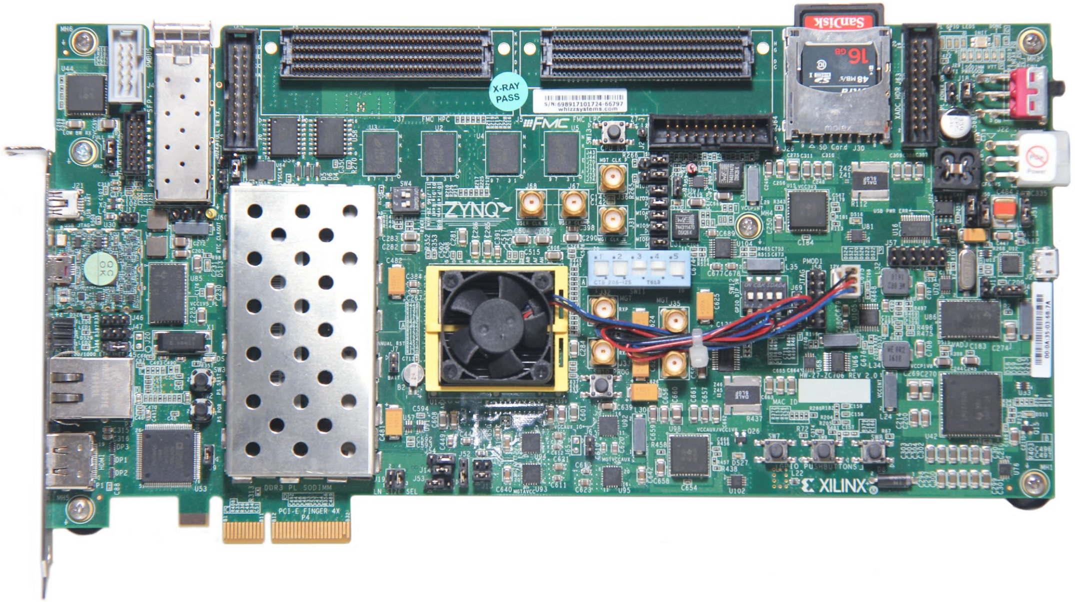
Caribou hardware architecture

- SoC board (e.g. Xilinx ZC706)
  - An embedded CPU runs DAQ and control software
  - An FPGA runs custom hardware blocks for data processing and detector control
- Control and Readout (CaR) interface board
  - Provides physical interface from the SoC to the detector chip
  - CaR – SoC connection extendable by a cable (3 m tested)
- Application-specific detector carrier board
  - Detector chip
    and passive components only



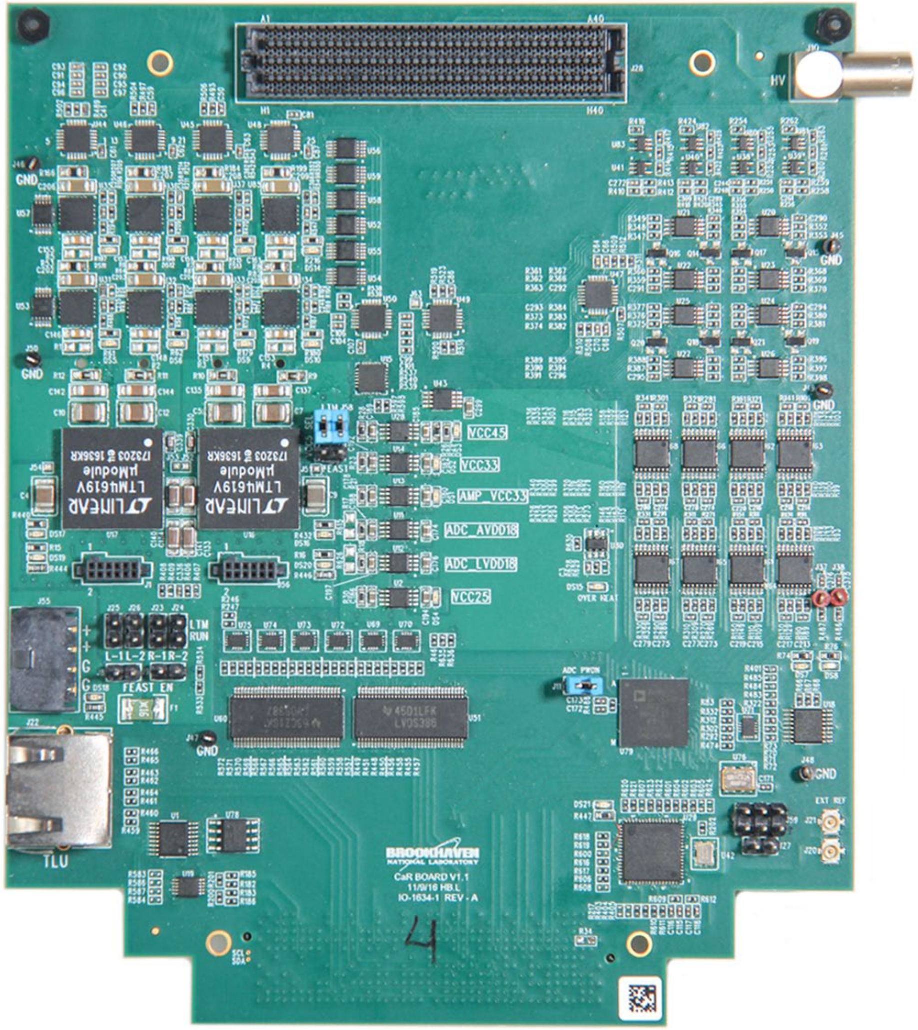
FPGA/SoC board

- Xilinx ZC706 (**Zynq-7000 SoC**) is currently supported
- Embedded ARM CPU:
  - Runs a Yocto-based **Linux**
  - Standalone machine **connected via Ethernet**
  - Remote **SSH** connection available
  - Runs **DAQ software** (“Peary”)
  - Can run **data analysis** (quality monitoring) locally
  - Data can be stored locally (SD card, disk)
    or sent over network (NFS, EUDAQ, …)
- FPGA fabric:
  - Runs lower layers of communication protocols
  - Can (pre)process data in hardware



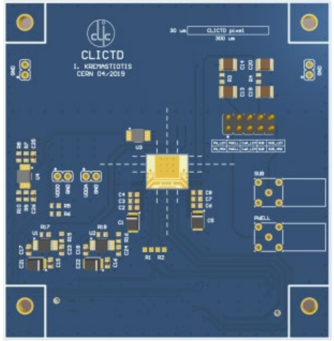
Control and Readout (CaR) board

Power	• 8 adjustable **power supplies** with monitoring • external **HV input**
Analog I/O	• 8 inputs to **12-bit ADC**, 50 kSamples/s • 16 inputs to **14-bit ADC**, 65 MSamples/s • 4 programmable **injection pulsers** • 32 adjustable **voltage references** • 8 adjustable **current references**
Digital I/O	• 8 full-duplex **high-speed links** (0.8-12 Gb/s) • 17 bidirectional **LVDS links** (<1.1 Gb/s) • 10/14 **output/input links**, adjustable level • **TLU** interface
Clocking	• Programmable low-jitter **clock generator** with **external** (TLU) **reference**
Interface	• **FMC** interface to FPGA board • 320-pin SEARAY interface to detector chip

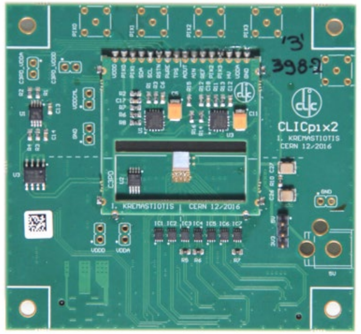


Detector carrier board (chip board)

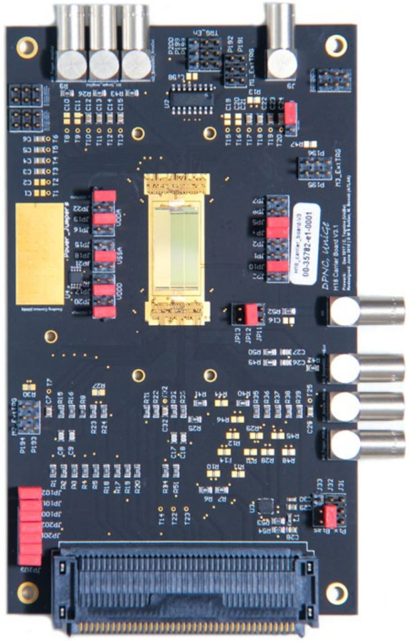
- Detector specific
  - The **only** physical **hardware** to be made **for a new detector**
  - Passive and detector-specific components only
- Selection of already supported detectors and chipboards:



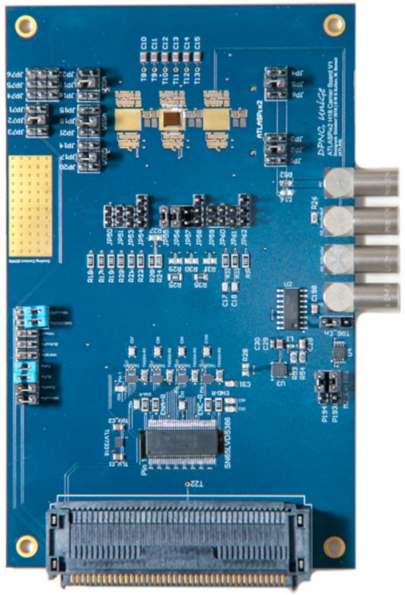
CLICTD



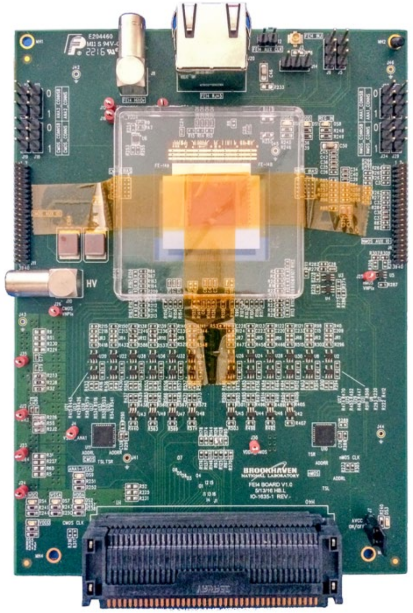
C3PD
CLICpix2



ATLASPix

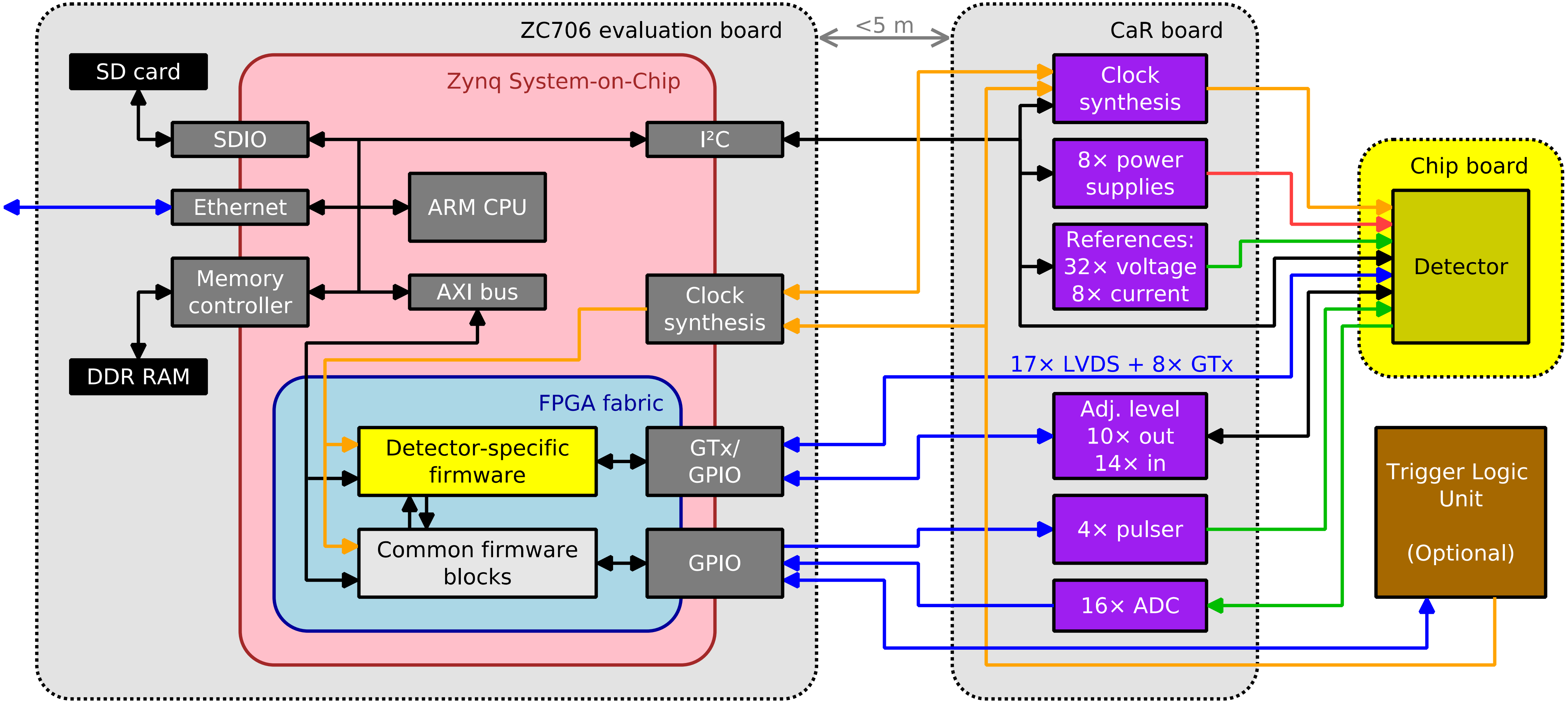


ATLASPix2



H35Demo
FEI4

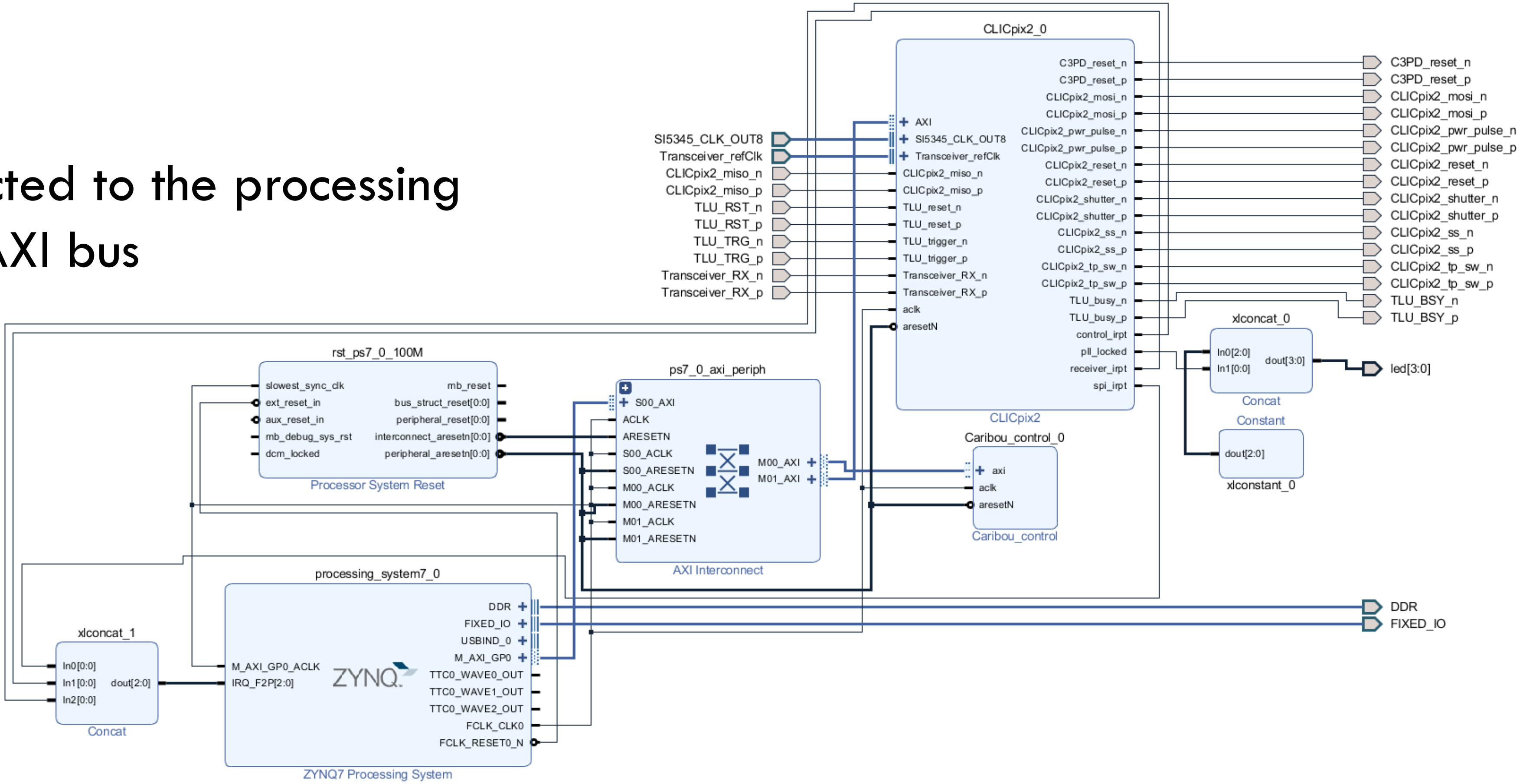
Caribou hardware architecture schematic



— digital differential — digital single-ended — analog — clock — power

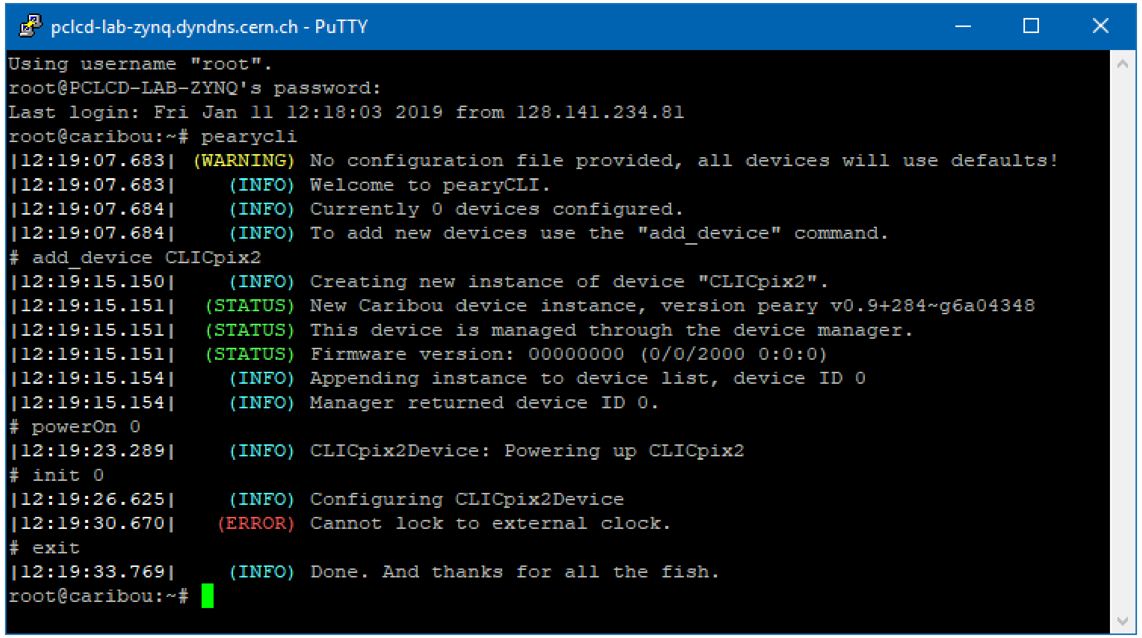
Caribou FPGA Firmware

- An **interface** between CPU (SW) and a detector (HW)
- User needs to create or adjust detector-specific modules
  - Data transfer
  - Detector control
- Modules are connected to the processing system through an AXI bus



Caribou software – Linux

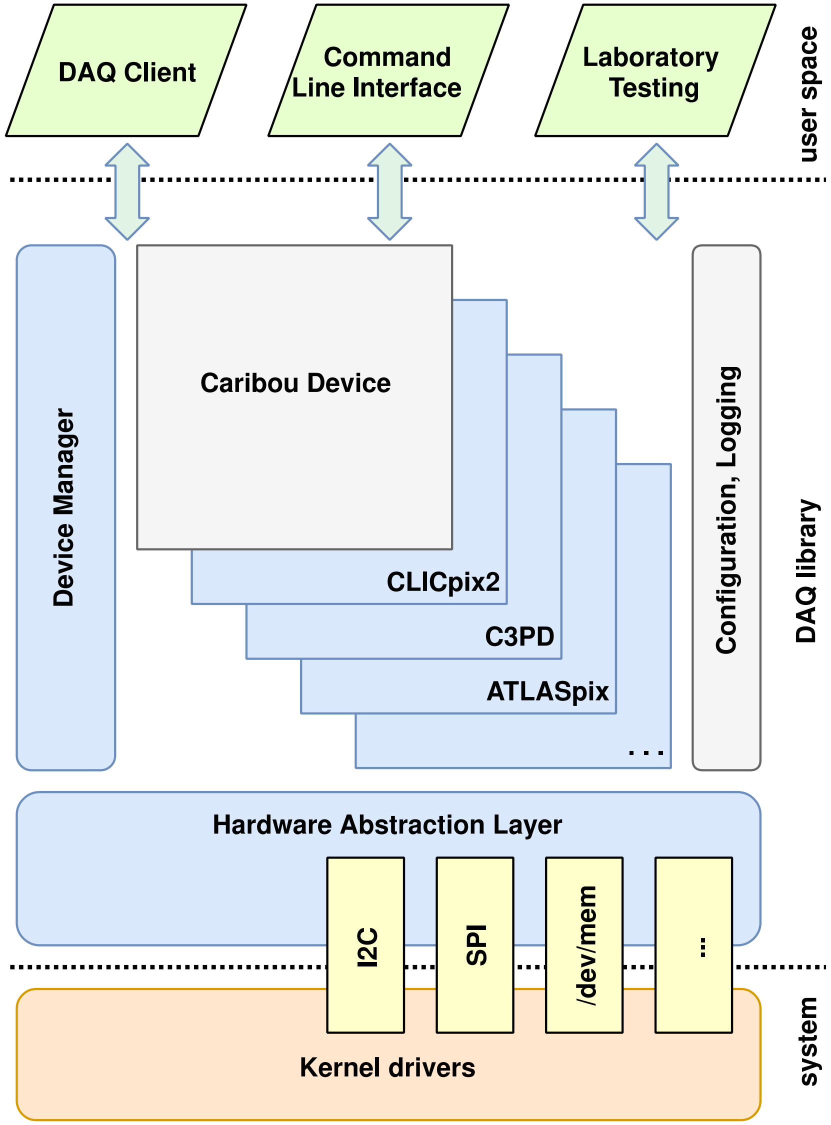
- **Custom** Yocto-based **Linux** distribution
- **OpenEmbedded** build system
- Using **Yocto** reference embedded distribution (called **Poky**)
  - Adding some **standard Linux packages** (ssh, python, git, NTP etc.)
  - Using community-developed **layer for Xilinx**
  - ZC706 (meta-xilinx)
  - Adding **custom layers** with own software and recipes to **build** an **SD card image** (meta-caribou)
- OS boots from SD card
  - One boot partition with bitsream and boot configuration (e.g. MAC address)
  - Second partition with Linux root filesystem



```
Using username "root".
root@PCLCD-LAB-ZYNQ's password:
Last login: Fri Jan 11 12:18:03 2019 from 128.141.234.81
root@caribou:~# pearycli
|12:19:07.683| (WARNING) No configuration file provided, all devices will use defaults!
|12:19:07.683|    (INFO) Welcome to pearyCLI.
|12:19:07.684|    (INFO) Currently 0 devices configured.
|12:19:07.684|    (INFO) To add new devices use the "add_device" command.
# add_device CLICpix2
|12:19:15.150|    (INFO) Creating new instance of device "CLICpix2".
|12:19:15.151|  (STATUS) New Caribou device instance, version peary v0.9+284~g6a04348
|12:19:15.151|  (STATUS) This device is managed through the device manager.
|12:19:15.151|  (STATUS) Firmware version: 00000000 (0/0/2000 0:0:0)
|12:19:15.154|    (INFO) Appending instance to device list, device ID 0
|12:19:15.154|    (INFO) Manager returned device ID 0.
# powerOn 0
|12:19:23.289|    (INFO) CLICpix2Device: Powering up CLICpix2
# init 0
|12:19:26.625|    (INFO) Configuring CLICpix2Device
|12:19:30.670|   (ERROR) Cannot lock to external clock.
# exit
|12:19:33.769|    (INFO) Done. And thanks for all the fish.
root@caribou:~#
```

Caribou software – DAQ

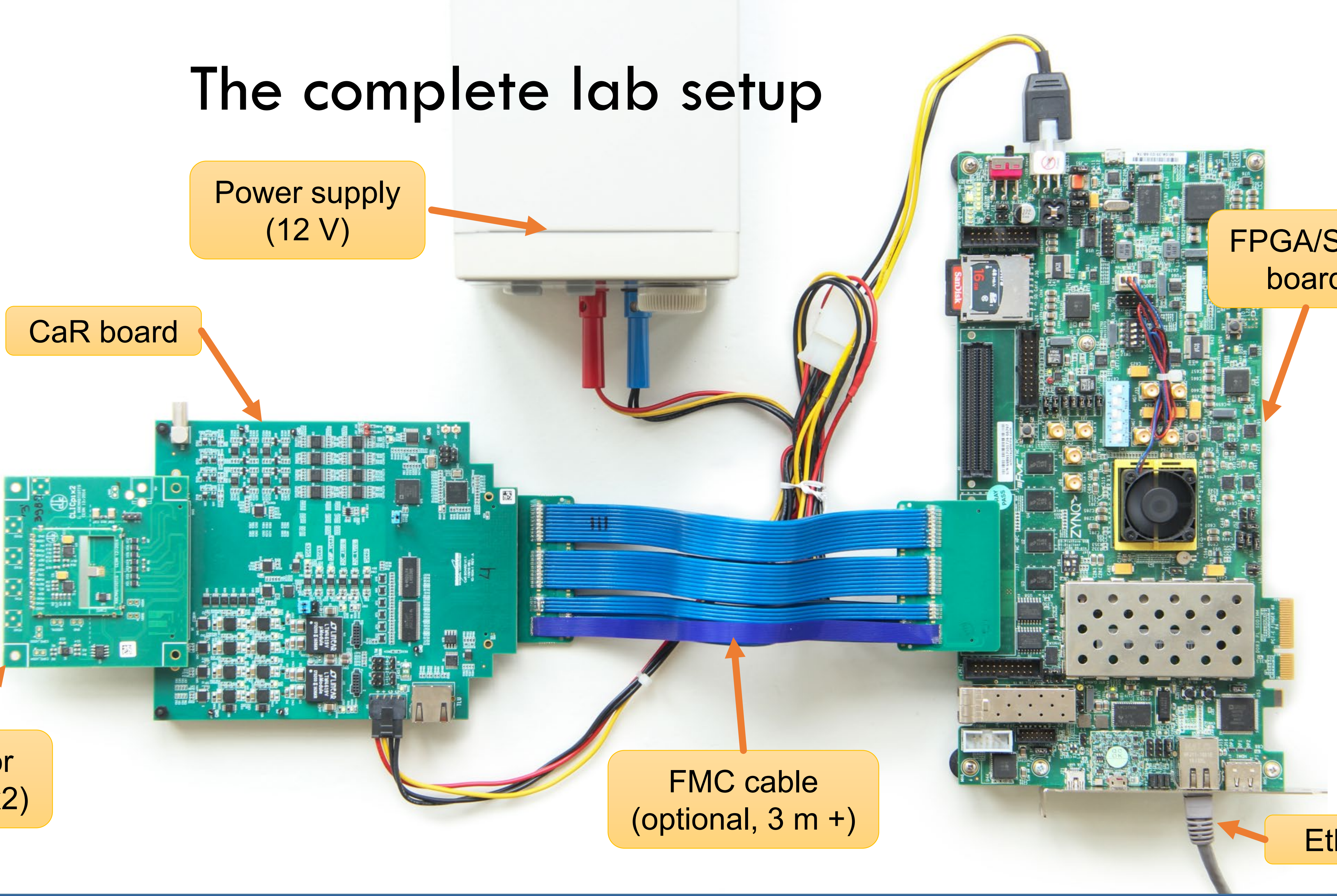
- DAQ **software framework for Caribou** (Peary):
  - Hardware Abstraction Layer (HAL)
    - **Interface** between SW and HW
    - Allows **handling peripherals** as objects in C++
  - Functions to control CaR board
    - Set/measure voltages, capture ADC, …
  - Device management
    - Multiple devices/detectors in parallel
  - Command line interface (CLI)
  - Client interface for integration with a superior DAQ
    - EUDAQ producer is implemented
  - Compatible with 32-bit and 64-bit systems



How to implement a new detector

- Hardware:
  - Design and produce a **chipboard –** route chip signals to suitable pins on CaR connector
- FPGA firmware:
  - Create or modify **FW blocks:**
    - to handle the control signals for the detector
    - to receive detector data and push it to FIFO
- Software (Peary):
  - Define **mapping** of:
    - Generic names of **CaR board peripherals** to detector-friendly names (`Vout_3 → VThrPix`)
    - Addresses of your **detector-specific registers** in FPGA to variable/object names
  - Create a module with **detector-specific functions** (`configure`, `startDAQ`, …)

The complete lab setup



Power supply (12 V)

CaR board

FPGA/SoC board

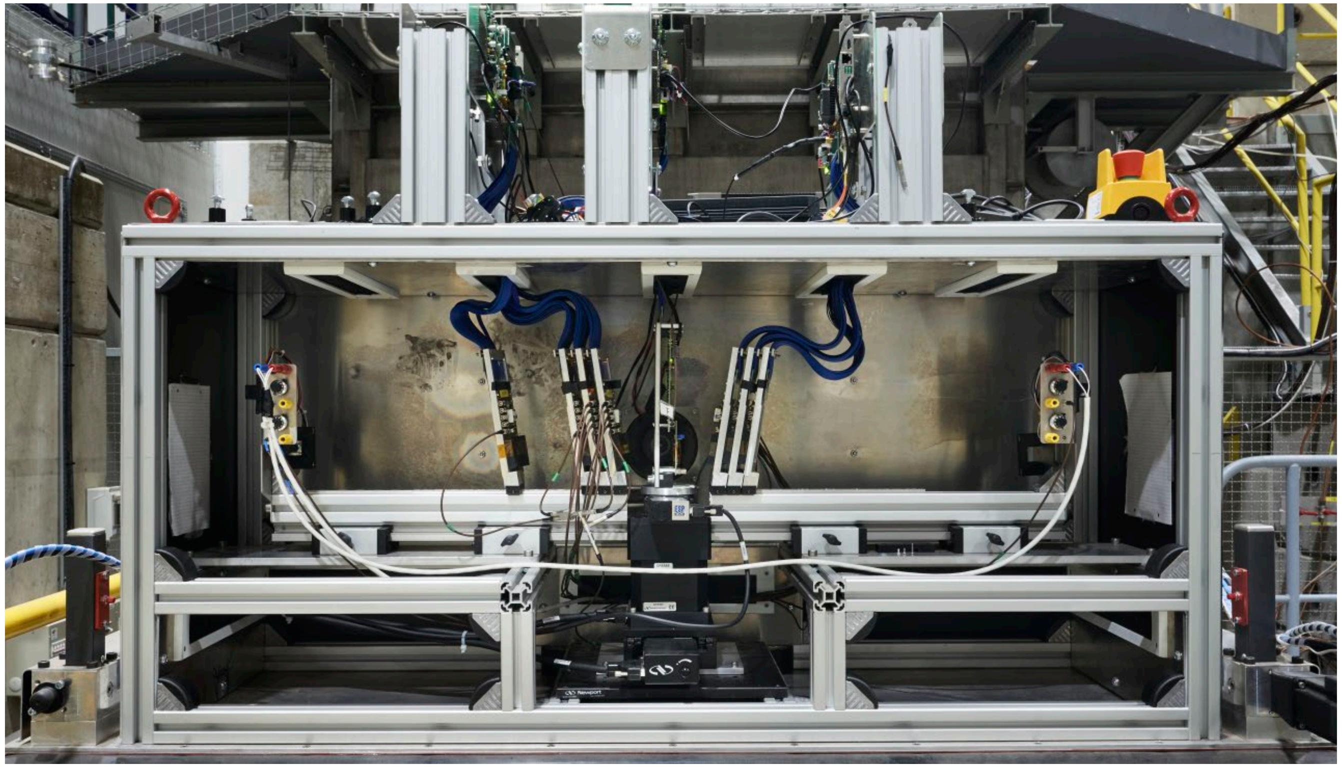
Detector (CLICpix2)

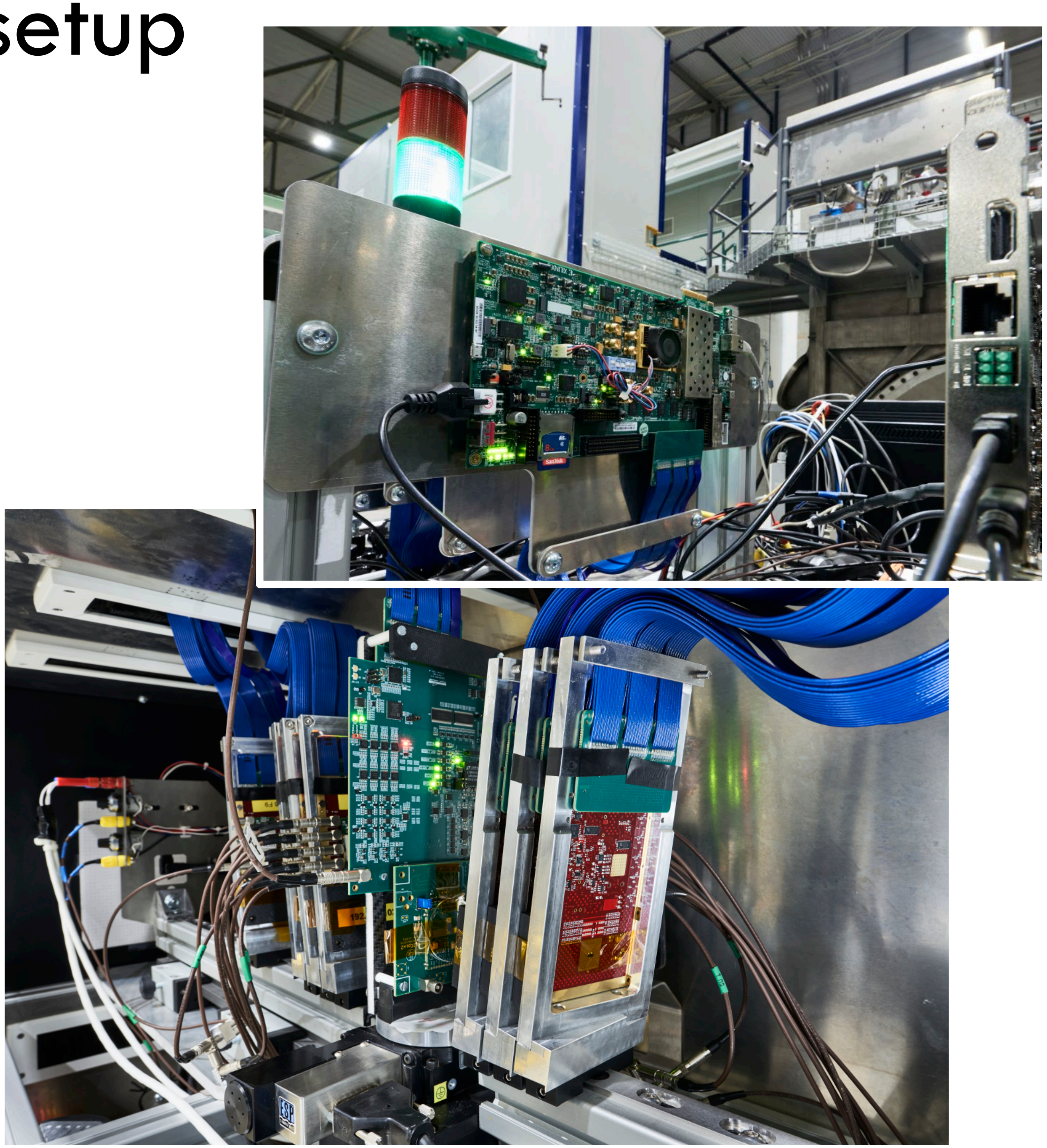
FMC cable (optional, 3 m +)

Ethernet

Testbeam setup

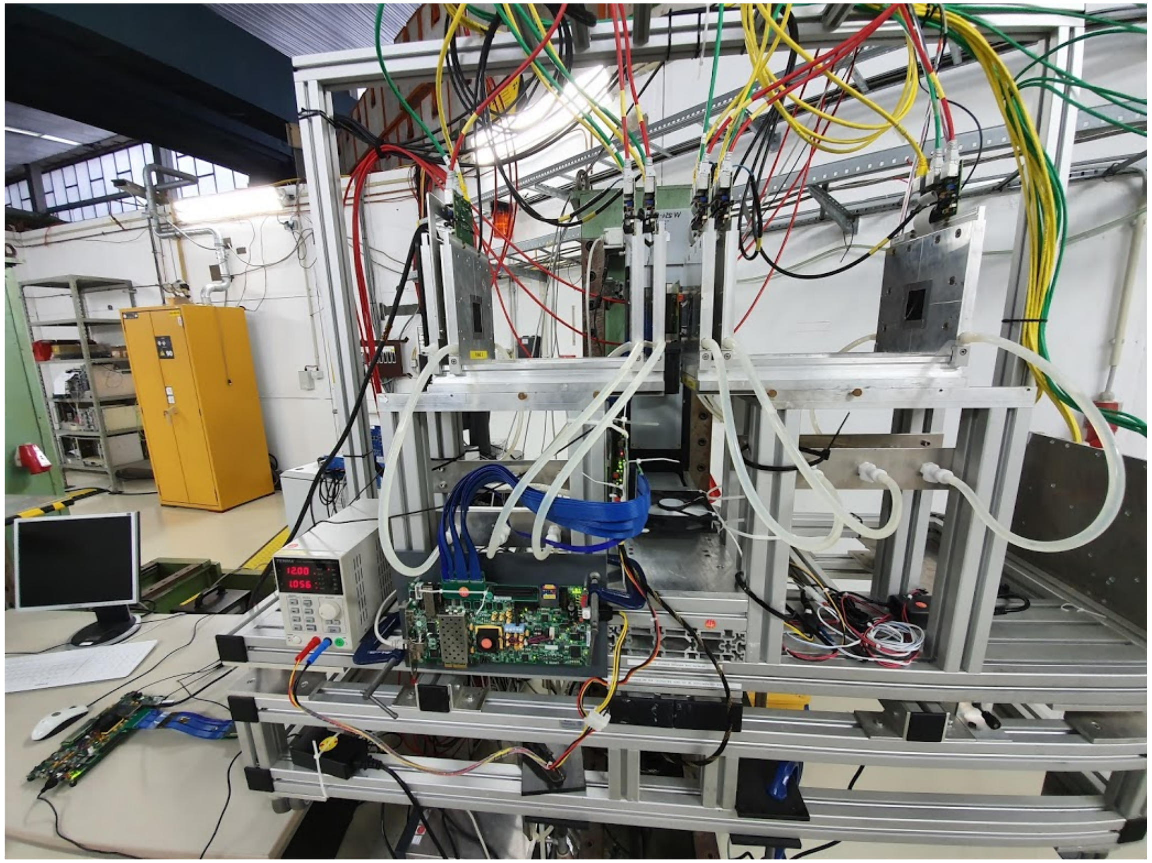
- CLIC Telescope in North Area (SPS, CERN)

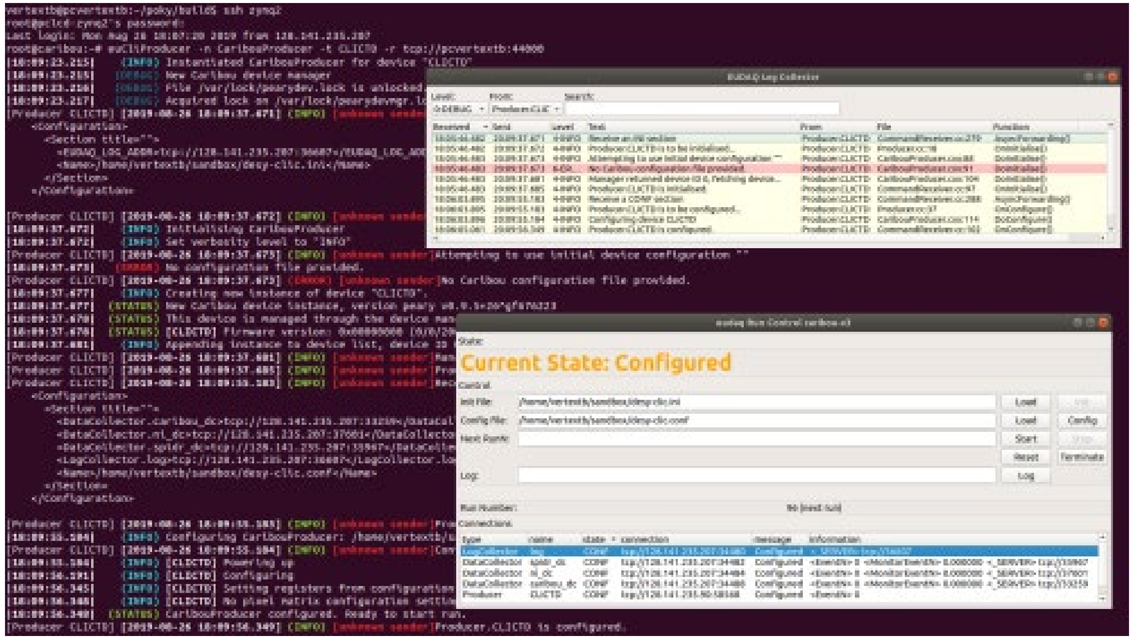




Testbeam setup

- EUDET Telescope at DESY II
  - Integrated with EUDAQ





```
vertextb@pcvertextb:~/poky/build$ ssh zynq2
root@pclcd-zynq2's password:
Last login: Mon Aug 26 10:07:20 2019 from 128.141.235.207
root@caribou:~# euCliProducer -n CaribouProducer -t CLICTD -r tcp://pcvertextb:44000
|10:09:23.215|      (INFO) Instantiated CaribouProducer for device "CLICTD"
|10:09:23.215|     (DEBUG) New Caribou device manager
|10:09:23.216|     (DEBUG) File /var/lock/pearydev.lock is unlocked
|10:09:23.217|     (DEBUG) Acquired lock on /var/lock/pearydevmgr.lo
[Producer CLICTD] [2019-08-26 10:09:37.471] (INFO) [unknown sender]
    <Configuration>
      <Section title="">
        <EUDAQ_LOG_ADDR>tcp://128.141.235.207:36687</EUDAQ_LOG_ADD
        <Name>/home/vertextb/sandbox/desy-clic.ini</Name>
      </Section>
    </Configuration>

[Producer CLICTD] [2019-08-26 10:09:37.472] (INFO) [unknown sender
|10:09:37.472|      (INFO) Initialising CaribouProducer
|10:09:37.472|      (INFO) Set verbosity level to "INFO"
[Producer CLICTD] [2019-08-26 10:09:37.473] (INFO) [unknown sender]Attempting to use initial device configuration ""
|10:09:37.473|     (ERROR) No configuration file provided.
[Producer CLICTD] [2019-08-26 10:09:37.473] (ERROR) [unknown sender]No Caribou configuration file provided.
|10:09:37.477|      (INFO) Creating new instance of device "CLICTD".
|10:09:37.477|    (STATUS) New Caribou device instance, version peary v0.9.1+20^gf878223
|10:09:37.478|    (STATUS) This device is managed through the device man
|10:09:37.478|    (STATUS) [CLICTD] Firmware version: 0x00000000 (0/0/20
|10:09:37.481|      (INFO) Appending instance to device list, device ID
[Producer CLICTD] [2019-08-26 10:09:37.481] (INFO) [unknown sender]Man
[Producer CLICTD] [2019-08-26 10:09:37.485] (INFO) [unknown sender]Pro
[Producer CLICTD] [2019-08-26 10:09:55.183] (INFO) [unknown sender]Rec
    <Configuration>
      <Section title="">
        <DataCollector.caribou_dc>tcp://128.141.235.207:33230</DataCol
        <DataCollector.ni_dc>tcp://128.141.235.207:37601</DataCollecto
        <DataCollector.spidr_dc>tcp://128.141.235.207:35967</DataColle
        <LogCollector.log>tcp://128.141.235.207:36687</LogCollector.lo
        <Name>/home/vertextb/sandbox/desy-clic.conf</Name>
      </Section>
    </Configuration>

[Producer CLICTD] [2019-08-26 10:09:55.183] (INFO) [unknown sender]Pro
|10:09:55.184|      (INFO) Configuring CaribouProducer: /home/vertextb/s
[Producer CLICTD] [2019-08-26 10:09:55.184] (INFO) [unknown sender]Con
|10:09:55.184|      (INFO) [CLICTD] Powering up
|10:09:56.291|      (INFO) [CLICTD] Configuring
|10:09:56.345|      (INFO) [CLICTD] Setting registers from configuration
|10:09:56.348|      (INFO) [CLICTD] No pixel matrix configuration settin
|10:09:56.349|    (STATUS) CaribouProducer configured. Ready to start run.
[Producer CLICTD] [2019-08-26 10:09:56.349] (INFO) [unknown sender]Producer.CLICTD is configured.
```

EUDAQ Log Collector

Received	Sent	Level	Text	From	File	Function
10:05:46.482	20:09:37.471	4-INFO	Receive an INI section	Producer.CLICTD	CommandReceiver.cc:279	AsyncForwarding()
10:05:46.482	20:09:37.472	4-INFO	Producer.CLICTD is to be initialised...	Producer.CLICTD	Producer.cc:18	OnInitialise()
10:05:46.483	20:09:37.473	4-INFO	Attempting to use initial device configuration ""	Producer.CLICTD	CaribouProducer.cc:88	DoInitialise()
10:05:46.483	20:09:37.473	6-ER...	No Caribou configuration file provided.	Producer.CLICTD	CaribouProducer.cc:91	DoInitialise()
10:05:46.483	20:09:37.481	4-INFO	Manager returned device ID 0, fetching device...	Producer.CLICTD	CaribouProducer.cc:104	DoInitialise()
10:05:46.483	20:09:37.485	4-INFO	Producer.CLICTD is initialised.	Producer.CLICTD	CommandReceiver.cc:97	OnInitialise()
10:06:01.895	20:09:55.183	4-INFO	Receive a CONF section	Producer.CLICTD	CommandReceiver.cc:288	AsyncForwarding()
10:06:01.895	20:09:55.183	4-INFO	Producer.CLICTD is to be configured...	Producer.CLICTD	Producer.cc:37	OnConfigure()
10:06:01.896	20:09:55.184	4-INFO	Configuring device CLICTD	Producer.CLICTD	CaribouProducer.cc:114	DoConfigure()
10:06:03.061	20:09:56.349	4-INFO	Producer.CLICTD is configured.	Producer.CLICTD	CommandReceiver.cc:102	OnConfigure()

euduq Run Control caribou-x3

State:

Current State: Configured

Control

Init File: /home/vertextb/sandbox/desy-clic.ini

Config File: /home/vertextb/sandbox/desy-clic.conf

Next RunN:

Log:

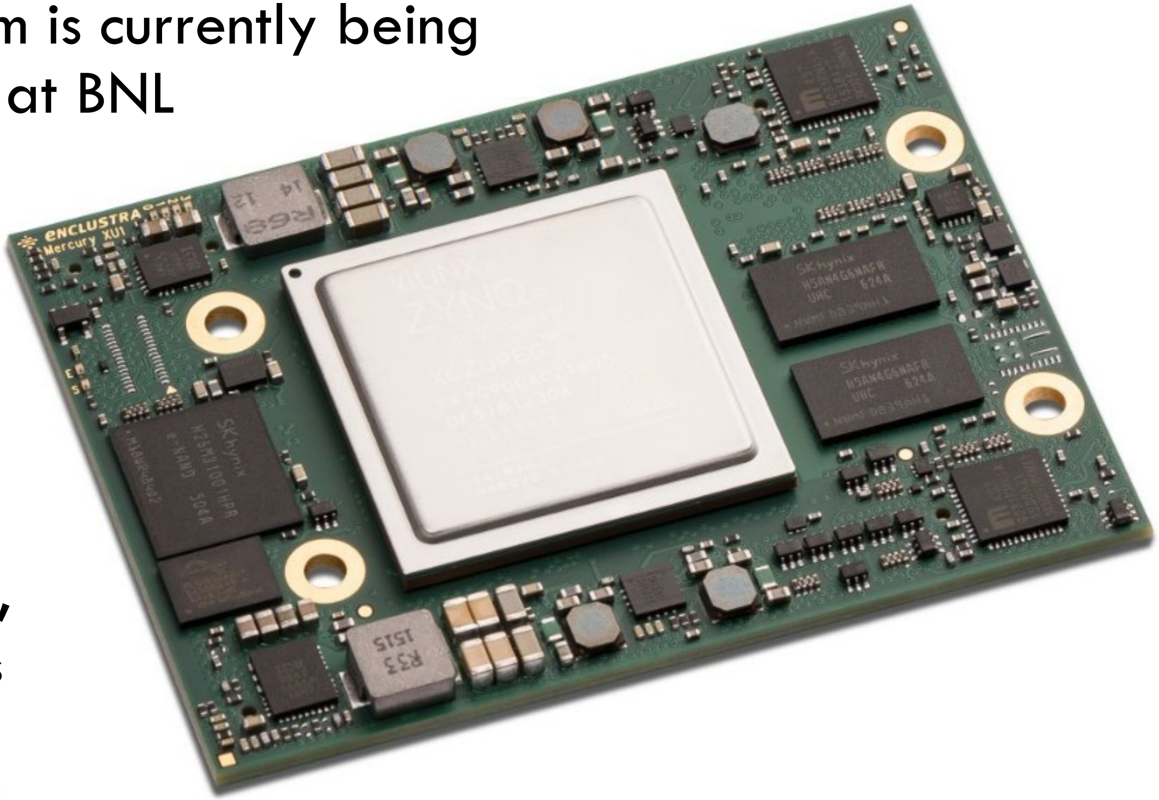
Run Number: 96 (next run)

Connections:

type	name	state	connection	message	information
LogCollector	log	CONF	tcp://128.141.235.207:34480	Configured	<_SERVER> tcp://36687
DataCollector	spidr_dc	CONF	tcp://128.141.235.207:34482	Configured	<EventN> 0 <MonitorEventN> 0.000000 <_SERVER> tcp://35967
DataCollector	ni_dc	CONF	tcp://128.141.235.207:34484	Configured	<EventN> 0 <MonitorEventN> 0.000000 <_SERVER> tcp://37601
DataCollector	caribou_dc	CONF	tcp://128.141.235.207:34486	Configured	<EventN> 0 <MonitorEventN> 0.000000 <_SERVER> tcp://33230
Producer	CLICTD	CONF	tcp://128.141.235.90:58168	Configured	<EventN> 0

Future plans

- The next generation of the Caribou platform is currently being design using Enclustra Mercury+ XU1 SOM at BNL
- Lower cost for users than current platform
  - From 3000€ to under 1500-2000€
- Increased IO performance, RAM capability
- Increased computing resources
  - 64bit CPU, Display and HDD support
- Multiple pin-compatible SoC modules exists,
  - Users can select one according to a project needs



Caribou summary

- Caribou is a versatile DAQ system for silicon pixel detectors
- Open source, Linux-based
- Standalone – no additional PC with a special software required
- Can run online data analysis locally
- Aimed for prototyping – laboratory and beam tests
- Focused on fast and simple implementation of a new detector
- New users and developers are welcome
- https://gitlab.cern.ch/Caribou