Planned LLRF upgrades

F. Ludwig / T. Jezynski
for the LLRF - Team


Outline

- Motivation
- Consequences from FLASH operation
- Transition to uTCA hardware platform
- Planned LLRF upgrades

FLASHs LLRF system at 2010

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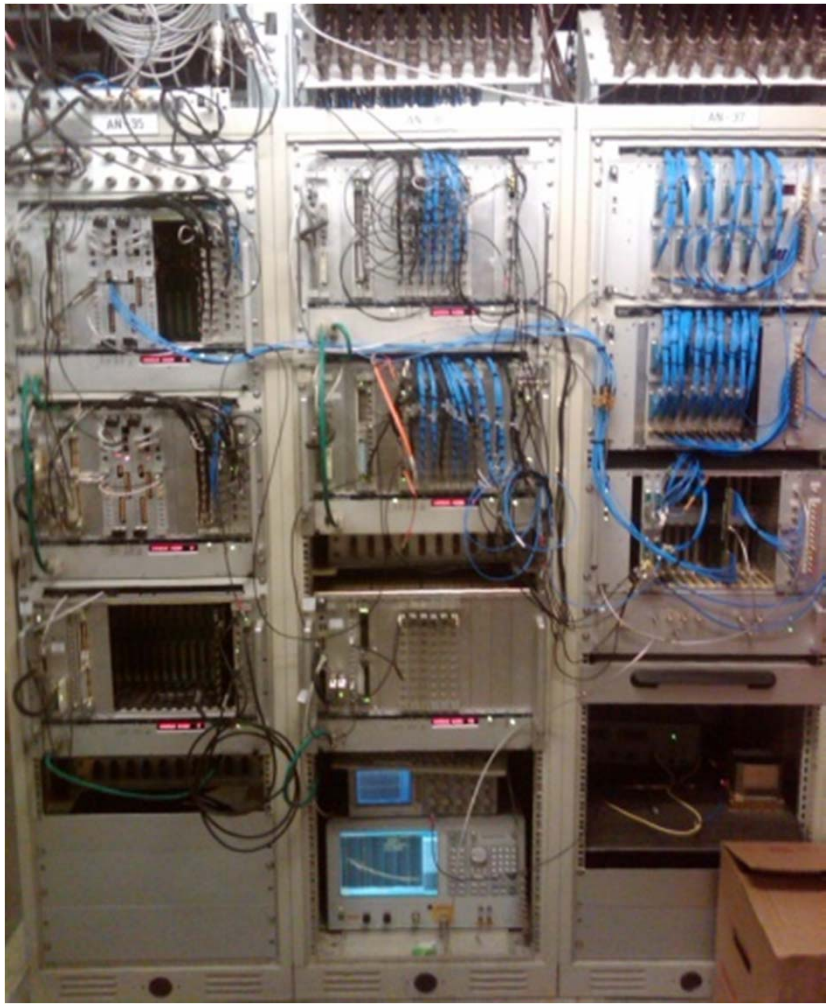
Upgrade of all injector RF stations

- Actuator and input power chain upgraded
- New cabling for RF-Gun, ACC1, ACC39
- Enclosed racks for better temperature stability
- Parallel cabling for development system
- Careful noise investigation, documentation

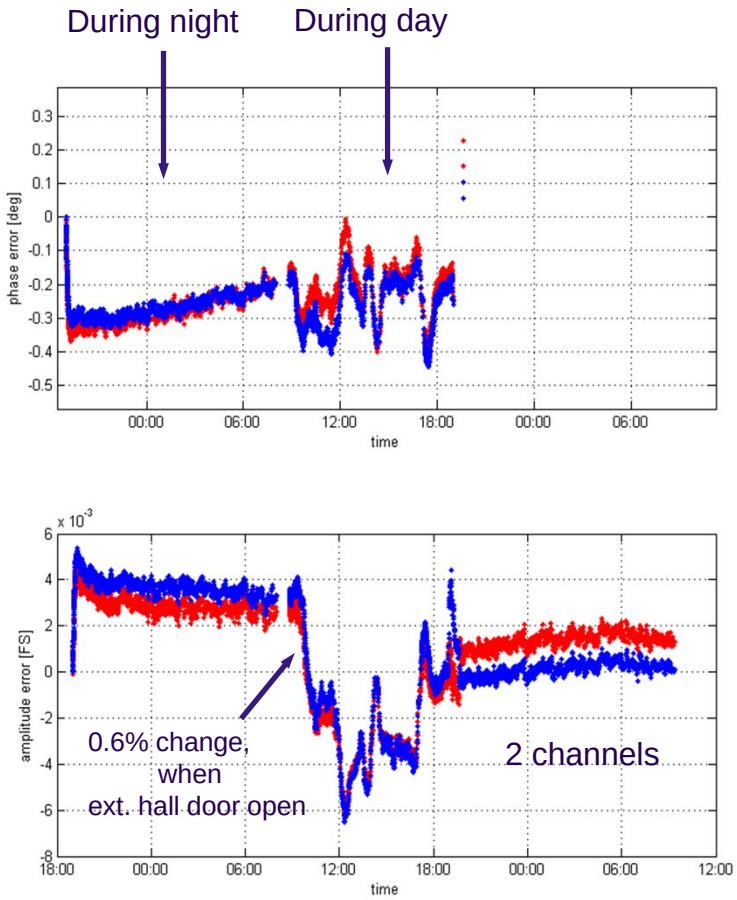
→ Energy stability improved by a factor of 3 to dE/E=0.5E-4.

We‘re done ? . . .

Motivation : Robust long-term operation



- **ACC456 Ext. Hall 3 :**



Motivation : Single cavity resolution

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LLRF performance :

Current system Testsystems

Status of the Performance Evaluation: [10min, 1MHz]	Switched-modulation (existing at FLASH)	CW modulation (non-IQ-sampling)	Direct-sampling
Self test using the reference in Laboratory (Single channel, 8 channels to be done)	**0.015% (11/2008) [3]**	**0.003% (2007)[1]**	to be done
Beam based in FLASH using SR-4BC2	0.016% (11/2008) [3]	0.022% (10/2007) [2]	to be done
2 DUT in FLASH using cavity probe splitting	**0.0065% (VS) [3]**	**?**	to be done
Self test using the reference in FLASH (Single channel, 8 channels to be done)	0.0068% (8 channels) [3]	0.016% (11/2007) [2]	0.022% (09/2008) [4]
Long-term operation at FLASH	YES	YES (ACC39)	No
Calibration scheme tested in laboratory / FLASH	YES (ACC1)	to be done	Reference tracking

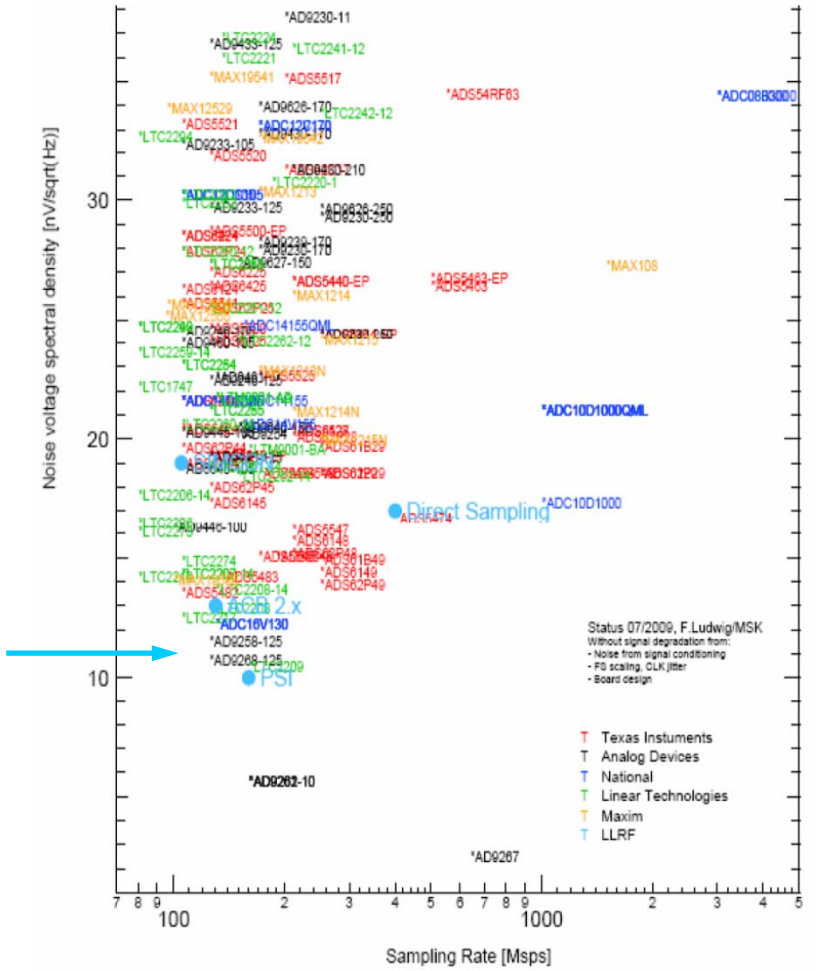
Confguration: **1:** Passive Receiver, 16-bit ADC ACB 2.1, **2:** Active Receiver, 14-bit ADC SIMCON 3.1
3: Active Receiver, 14-bit ADC SIMCON Boards, **4:** 12-bit ADC, 200Msps

- We benefit from cavity channel scaling in vector sum by about sqrt(8).
- ADC spectral density is (was) the limitation in the current SIMCON system
  14-bits (-135dBc/Hz) -> 16-bits (-147dBc/Hz)

Motivation : Single cavity resolution

- **AD9268 Eval Board with FLASH reference**

Actual ADC landscape:



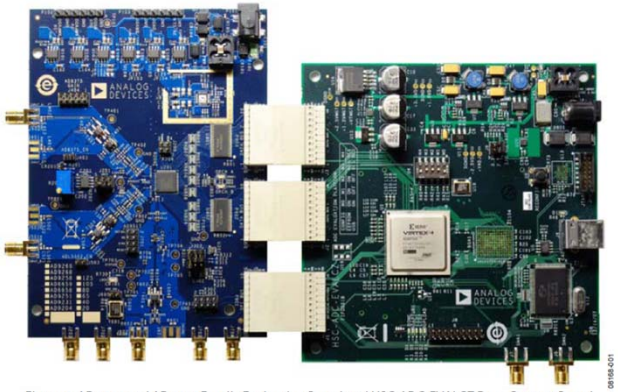
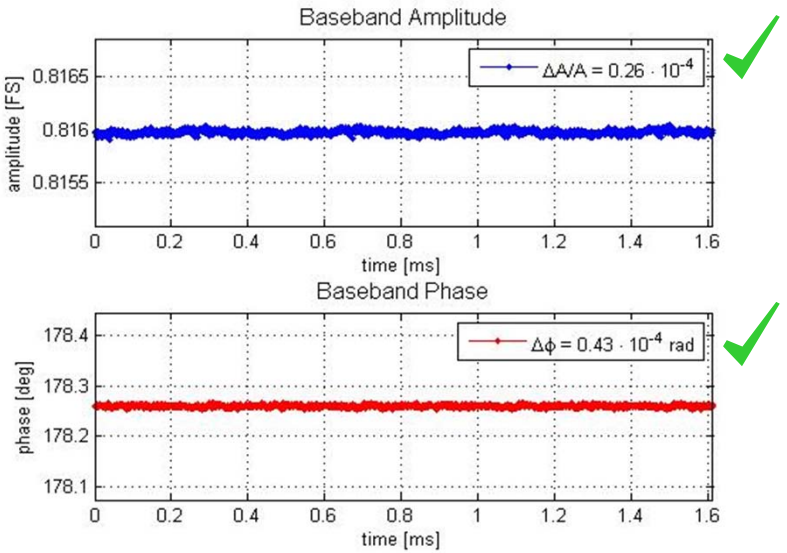


Figure 1. AD9268 and AD9269 Family Evaluation Board and HSC-ADC-EVALCZ Data Capture Board



Testconfguration:

- Multi-channel active receiver (KS Version)
- AD9268, dual, 16-bits, 125Msps, Evaluation Board
- FLASH Reference, Extension Hall
- LO-Generation Module (19“, FL, PM version)
- Offline Matlab non-iq analysis (N=2*65K)

Consequences from FLASH operation

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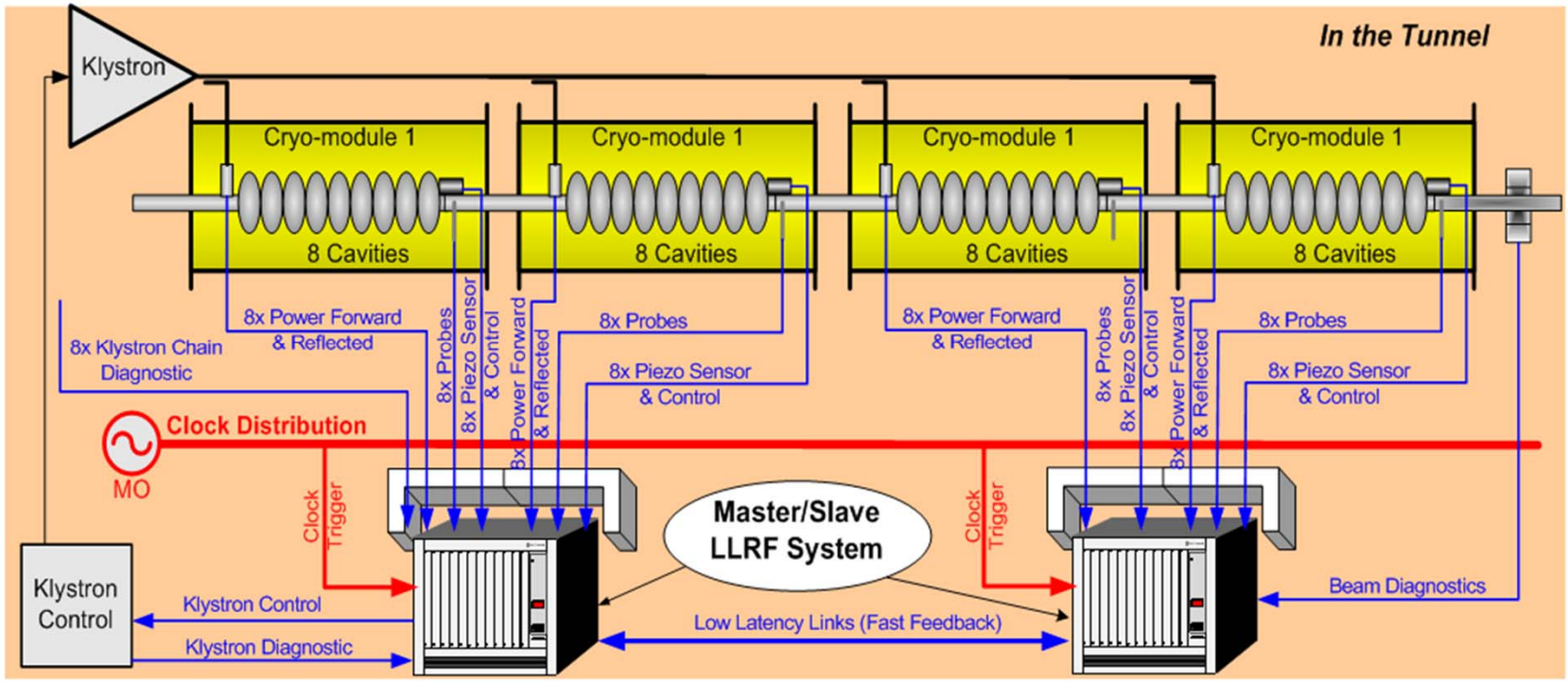
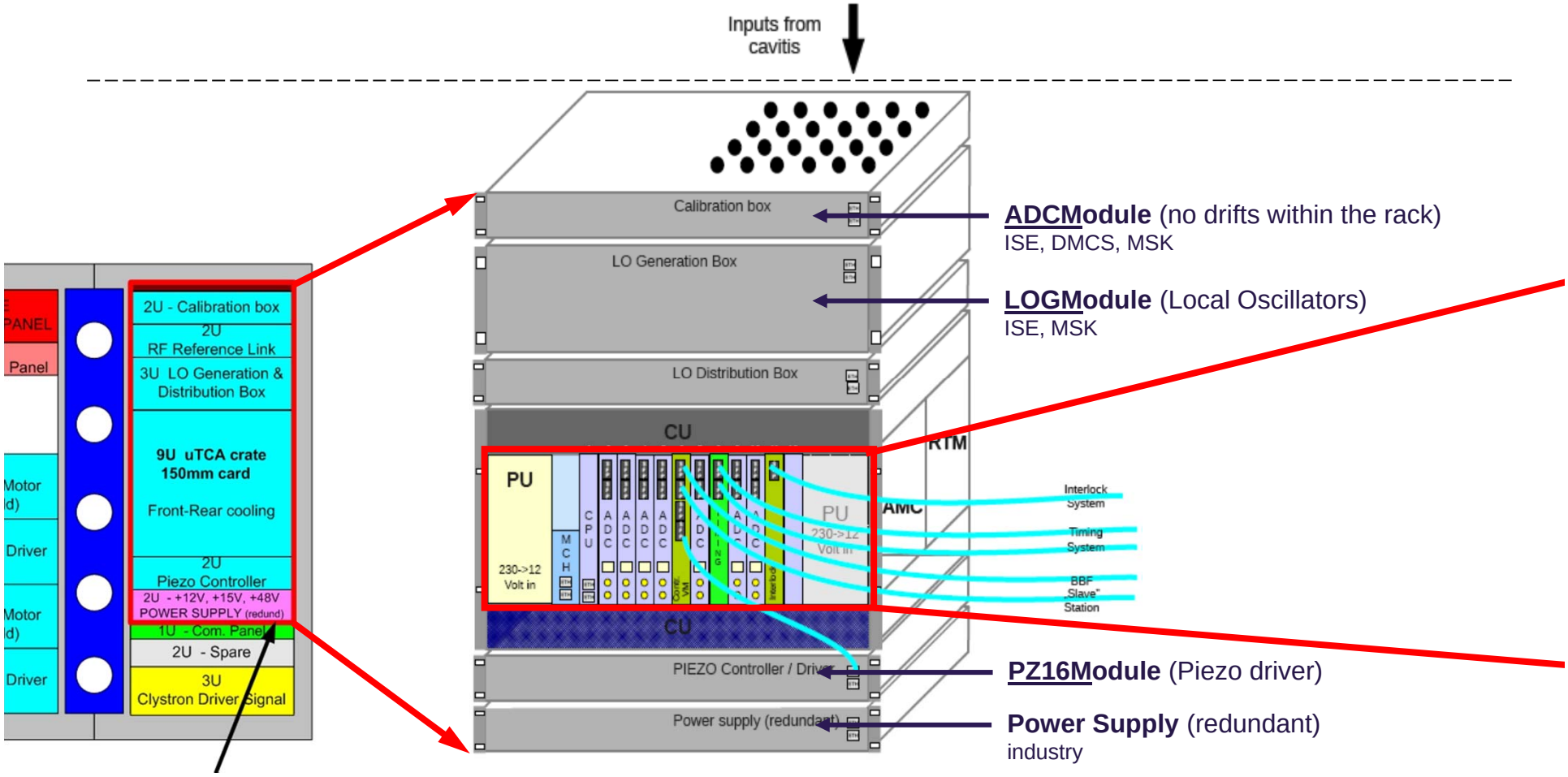
- **2 semi-distributed uTCA stations supply 4 cavity modules (J0,L1,L2,L3)**



Driving Argument → Short pickup cables for low drifts (10fs/m/K) and prevent crosstalk from high power cables

uTCA LLRF hardware platform

- **How will a LLRF System look like inside . . . 19“ modules . . .**

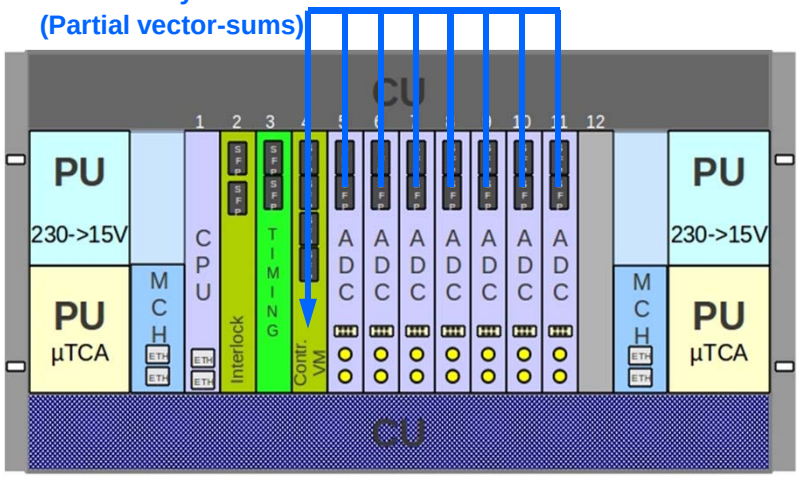


uTCA LLRF hardware platform

- **. . . and the crate . . .**

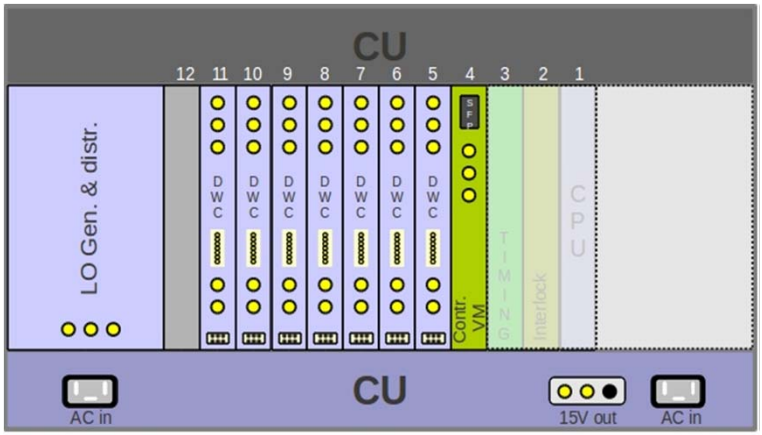
AMC front : (data pre-processing)

Low-latency links
(Partial vector-sums)



Slot #01: CPU	(Industry)
Slot #02: Interlock	(MCS)
Slot #03: Timing	(MCS)
Slot #04: **LLRF Controller**	**(uTLC / DMCS, MSK)**
Slot #05: ADC, Klystron Chain	(SIS8300 / Struck, MCS, MSK)
Slot #06: ADC, VS Reflected	(SIS8300 / Struck, MCS, MSK)
Slot #07: ADC, VS Reflected	(SIS8300 / Struck, MCS, MSK)
Slot #08: ADC, VS Forward	(SIS8300 / Struck, MCS, MSK)
Slot #09: ADC, VS Forward	(SIS8300 / Struck, MCS, MSK)
Slot #10: ADC, VS Probe	(SIS8300 / Struck, MCS, MSK)
Slot #11: ADC, VS Probe	(SIS8300 / Struck, MCS, MSK)
Slot #12: free	

RTM rear: (signal conditioning)



Slot #01: -	
Slot #02: -	
Slot #03: -	
Slot #04: **Klystron Driver**	**(uTLC VM / DMCS, ISE)**
Slot #05: **DWC, Klystron Chain**	**(DWC8300 / ISE, MSK)**
Slot #06: DWC, Reflected	(DWC8300 / ISE, MSK)
Slot #07: DWC, Reflected	(DWC8300 / ISE, MSK)
Slot #08: DWC, Forward	(DWC8300 / ISE, MSK)
Slot #09: DWC, Forward	(DWC8300 / ISE, MSK)
Slot #10: DWC, Probe	(DWC8300 / ISE, MSK)
Slot #11: DWC, Probe	(DWC8300 / ISE, MSK)
Slot #12: free	
Slot #15: Test **LO-Generation**	**(uLOG RF-Backplane Test)**

uTCA LLRF hardware platform

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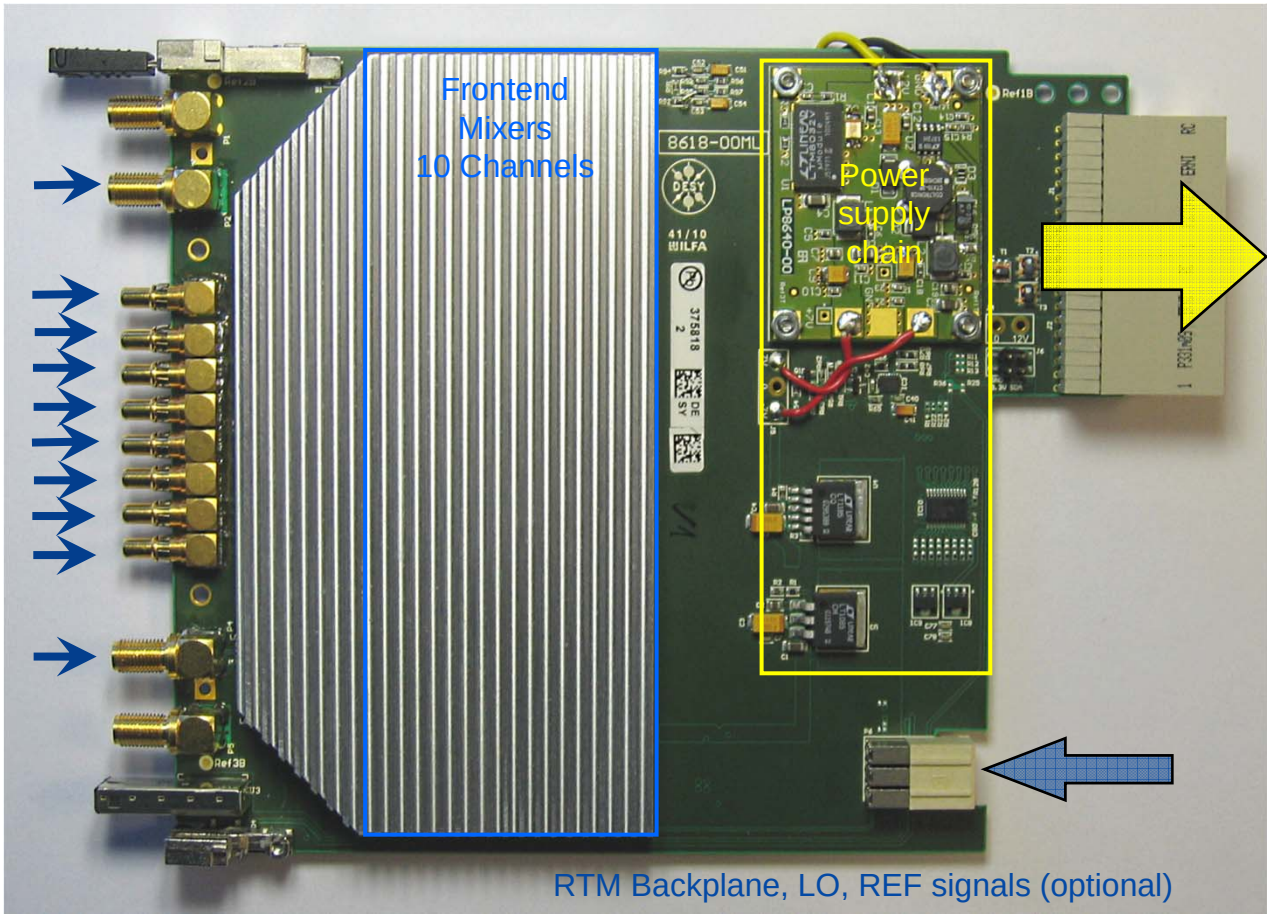
Multi-channel Down-Converter (DWC8300 R1.0)

- 10 channel field detection
  (1.3GHz … 3.9GHz version)
- Rear / Backplane RF access
- 8 Layer, Rogers (ZE)

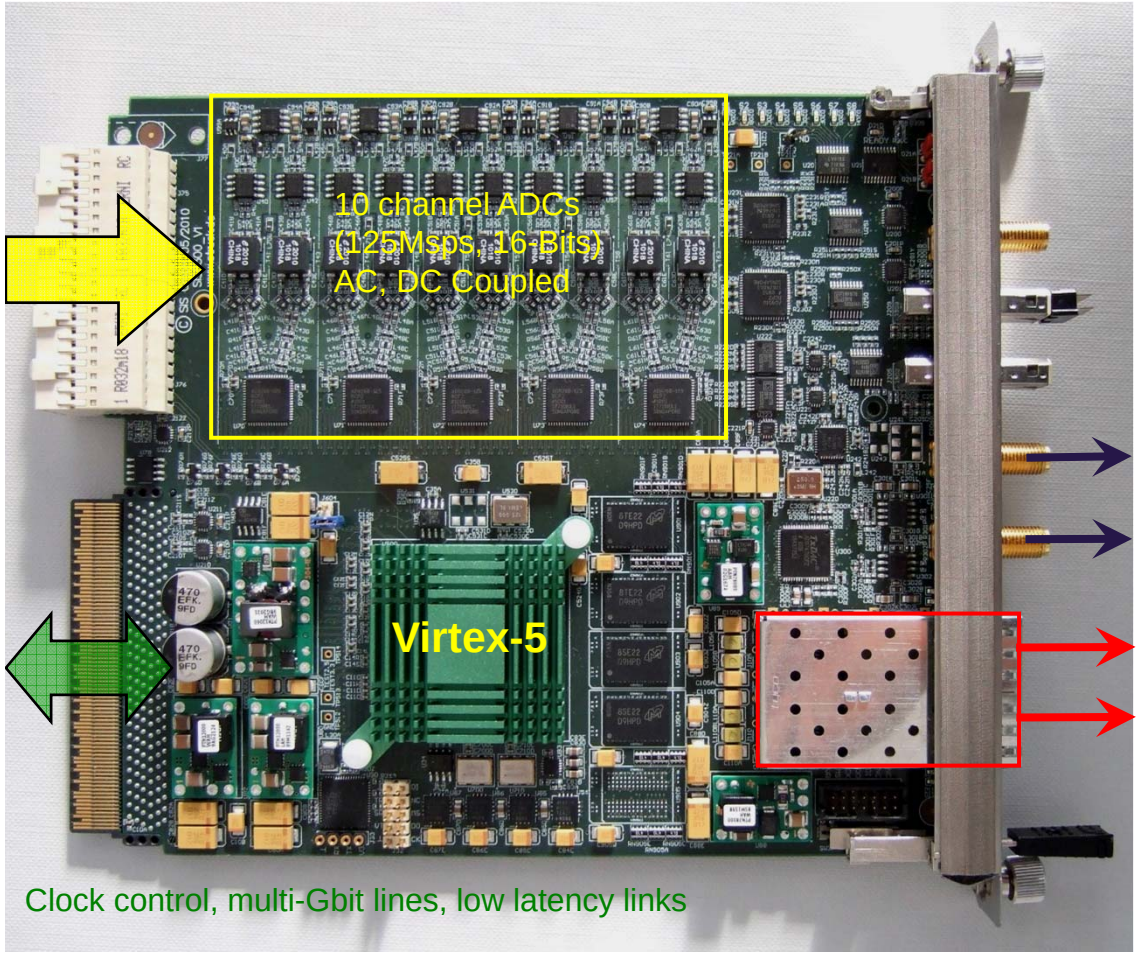


Courtesy:
J.Piekarski / ISE
M.Hoffmann, D.Kühn / DESY

uTCA LLRF hardware platform

Digitizer, Partial Vector Sum (SIS8300_V2)

struck innovative systeme



- 10 channel ADCs (125Msps, 16-Bits)
- FPGA partial cavity vector sum
- Low latency links via uTCA-backplane

2x DAC Outputs

SFP front I/O's
Fiber or cable

uTCA LLRF hardware platform

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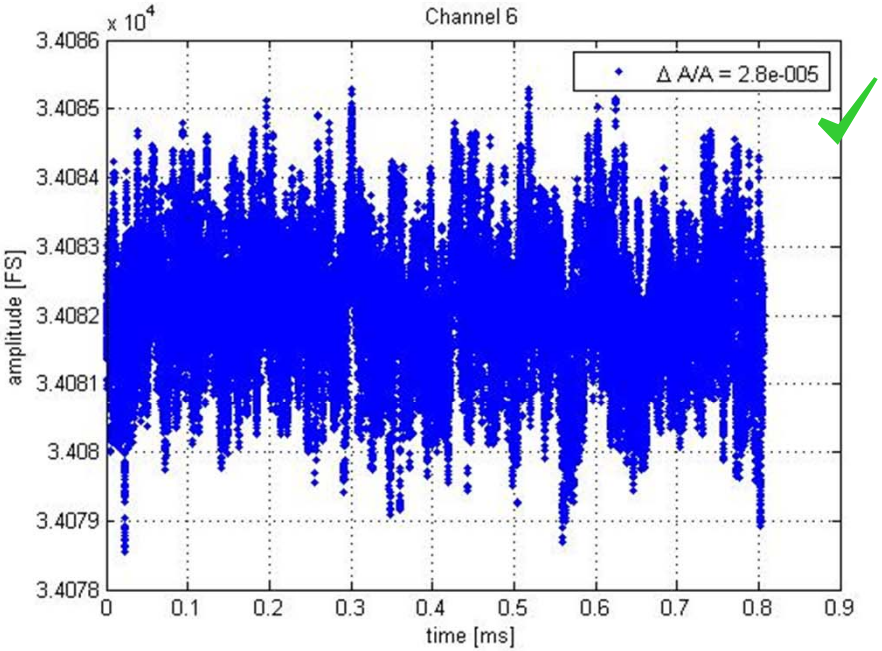
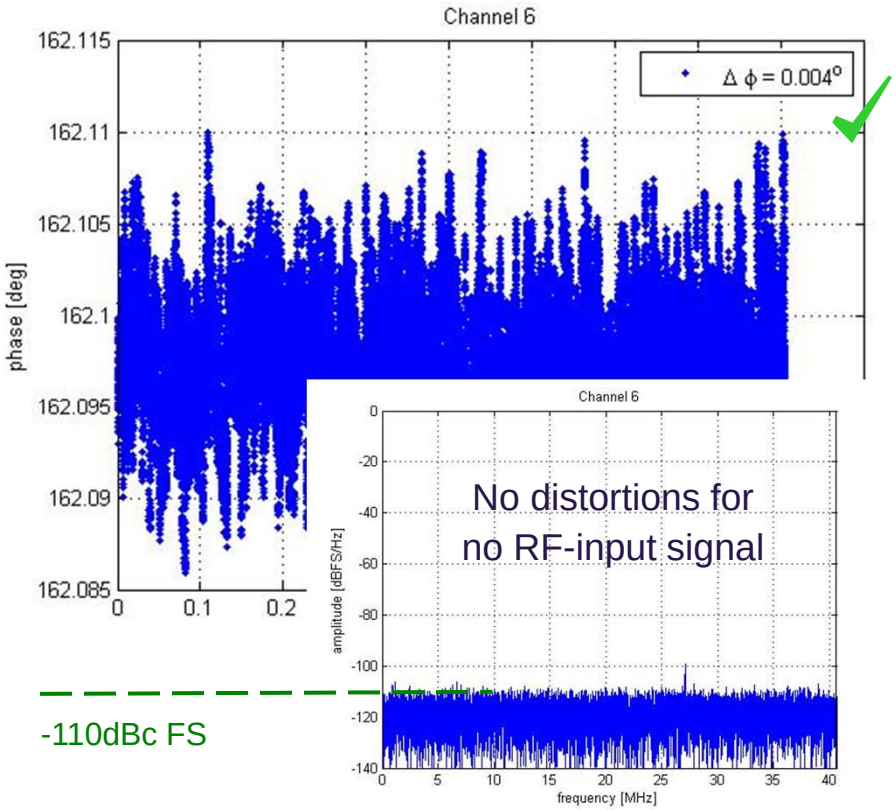
- **Signal-chain short-term stability in a uTCA crate (laboratory) :**





Testconfguration:

- DWC8300 R1.0, SIS8300_V2, MCH, CPU, uTCA crate
- DRO 1.3GHz (PSI), 1354 MHz LO, 54MHz IF, 81MHz SR
- LO-Generation Module (19“, FL, PM version)
- Offline Matlab non-iq analysis (N=65K), 1MHz Bandwidth

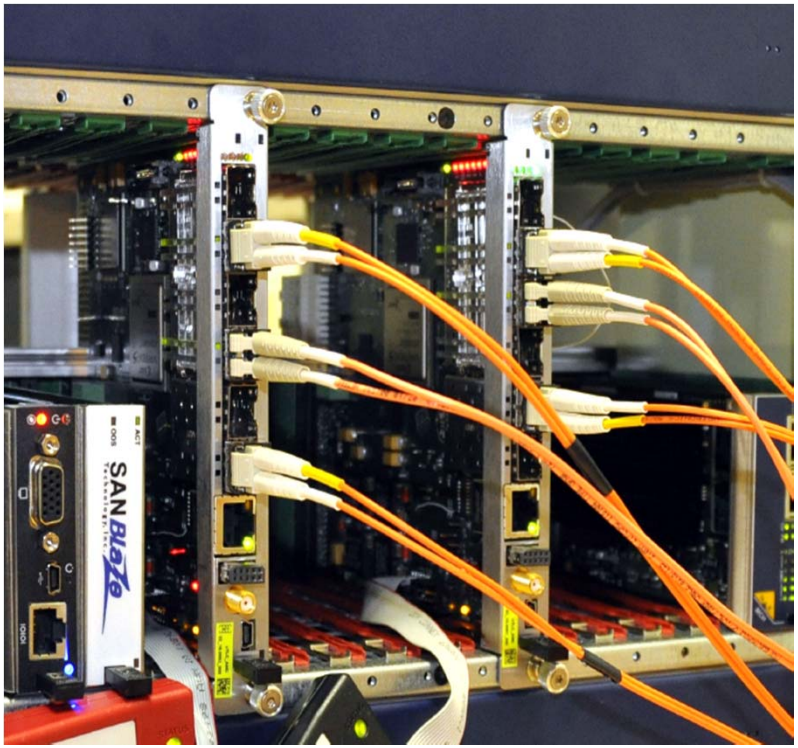
-110dBc FS

→ Single cavity resolution improved by a factor of 5 to dA/A=2.8E-5.

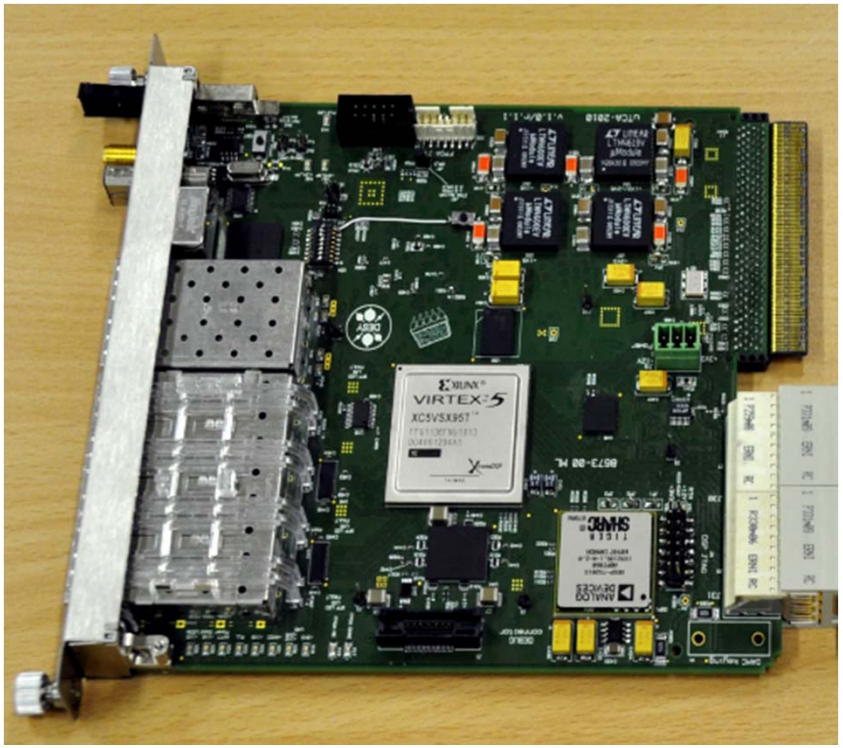
→ Signal integrity in uTCA crate achieved Eval board performance!

uTCA LLRF hardware platform

LLRF Controller (uTLC)



. . . during debugging . . .

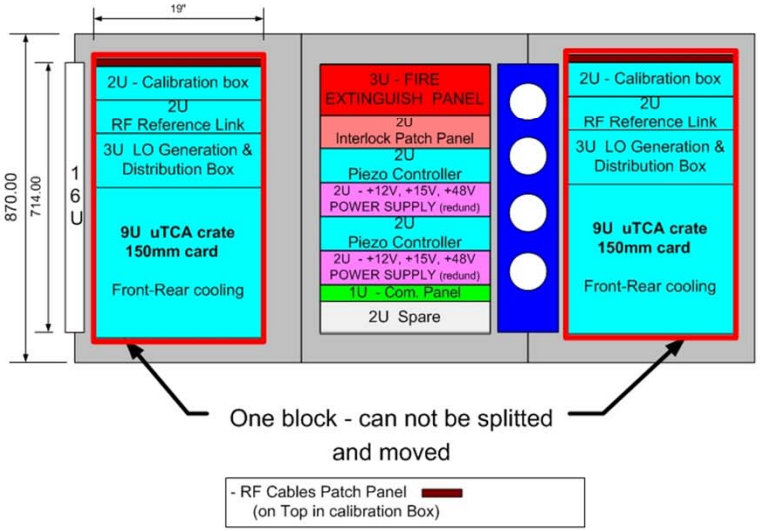


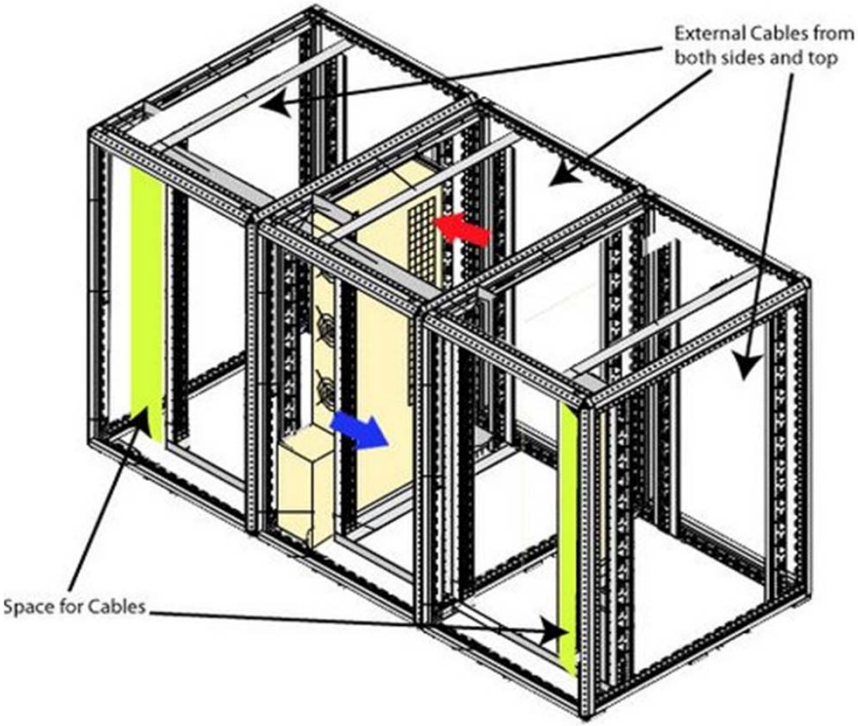
- LLRF Controller, 6 Fiber Ports, 2 GB-Links
- FPGA, DSP

Courtesy: D. Makowski / DMCS

uTCA LLRF hardware platform

- **Coarse inner rack temperature stability (<0.5°$_{pp}$)**



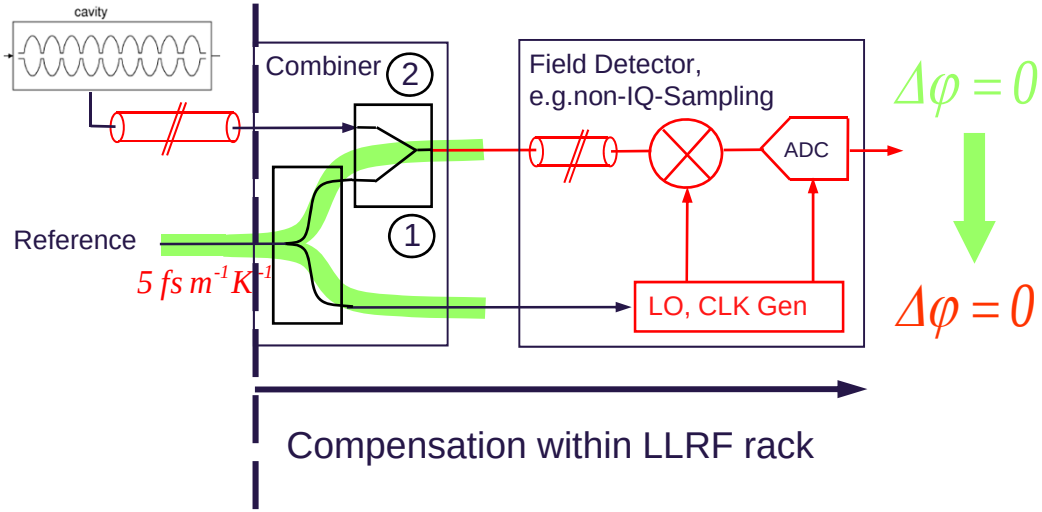


Courtesy:
W. Wierba / IFJ

uTCA LLRF hardware platform

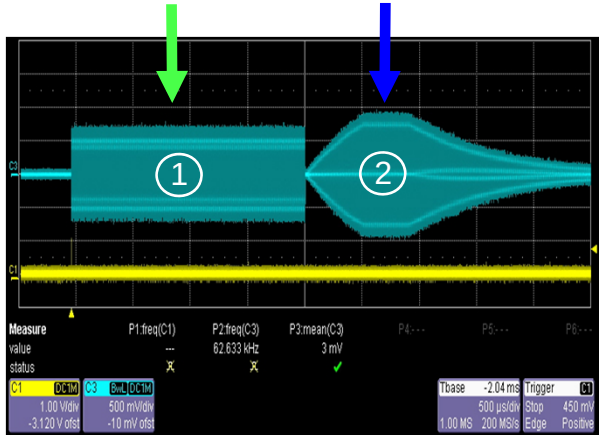
Reference injection calibration (simplified):

Relative Phase Calibration :



Injected reference and calibration

Cavity signal Measurement



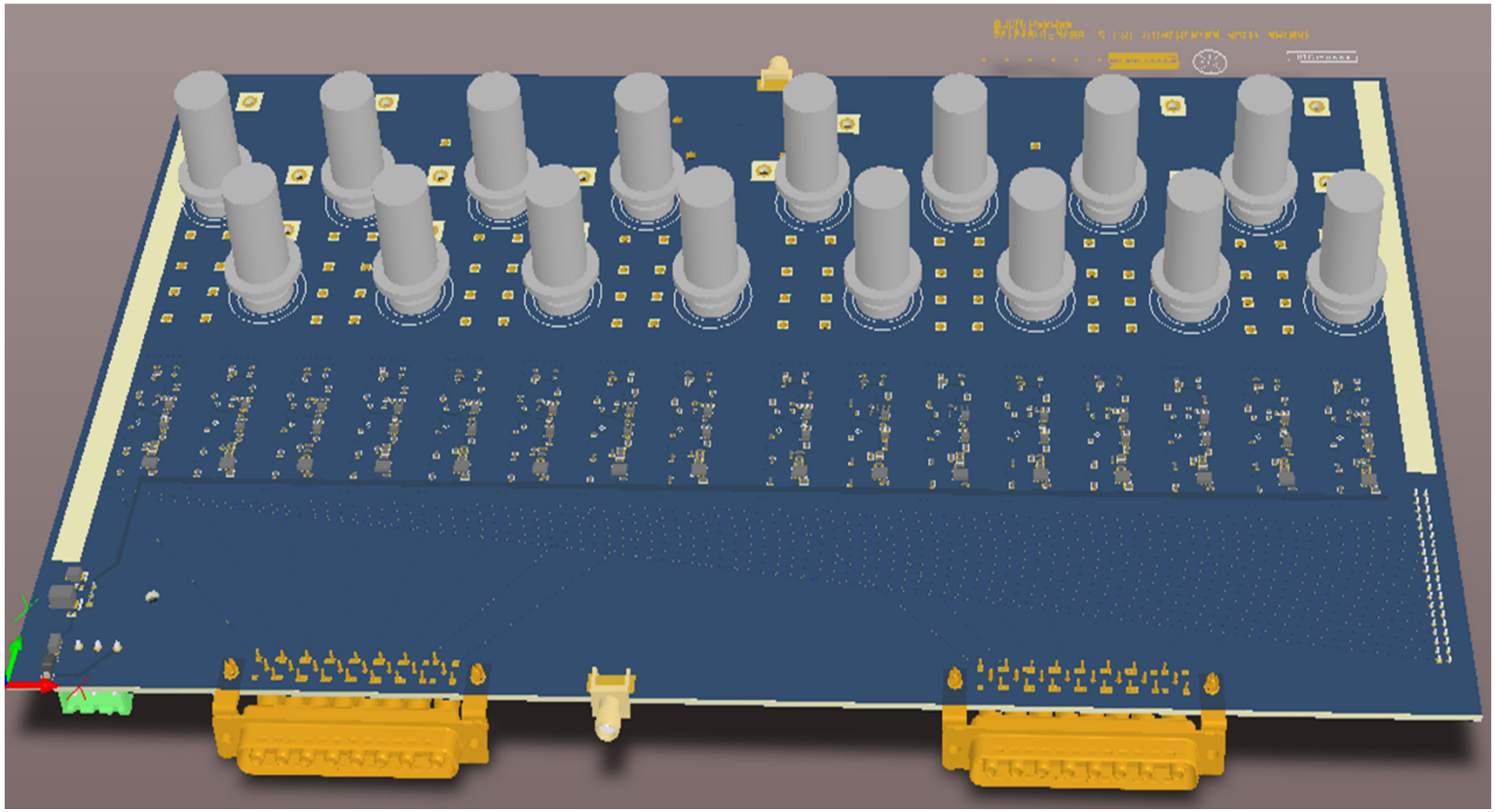
*** Uncompensated Heliax Pickup-cables:**

- Covered by Beam-based Feedback
- Heliax optimal operating point [32 deg] by heating
- 201x cavity-pickup reflectometer upgrade

- ➔ Long-term stability improvements by a factor of 100 from the ps-range to about 20fs (pp). ✓
- ➔ Demands on rack temp-conditioning will be relaxed.

uTCA LLRF hardware platform

- **Automated Drift Calibration Module (ADCM)** (design stage)



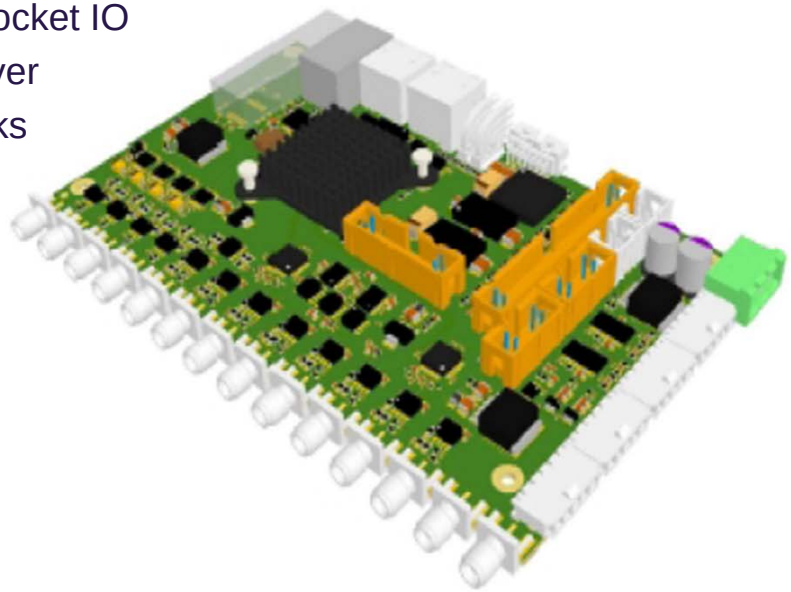
Courtesy: J. Piekarski / ISE

uTCA LLRF hardware platform

Temperature Control & Monitoring Board (TMCB)

- Control module for all 19“ modules
- Common hardware, software and firmware
- Variant assembly

- ADC, DAC data-acquisition (16-, 24-bit)
- Peltier temperature control
- I2C, GPIO, Rocket IO
- Timing Receiver
- GP LVDS Links
- Ethernet



Instrumentation Technologies

Instrumentation Technologies d.d.
Velika pot 22
5250 Solkan
Slovenia
Tel: +386 5 3352600
Fax: +386 5 3352601

Production folder for:

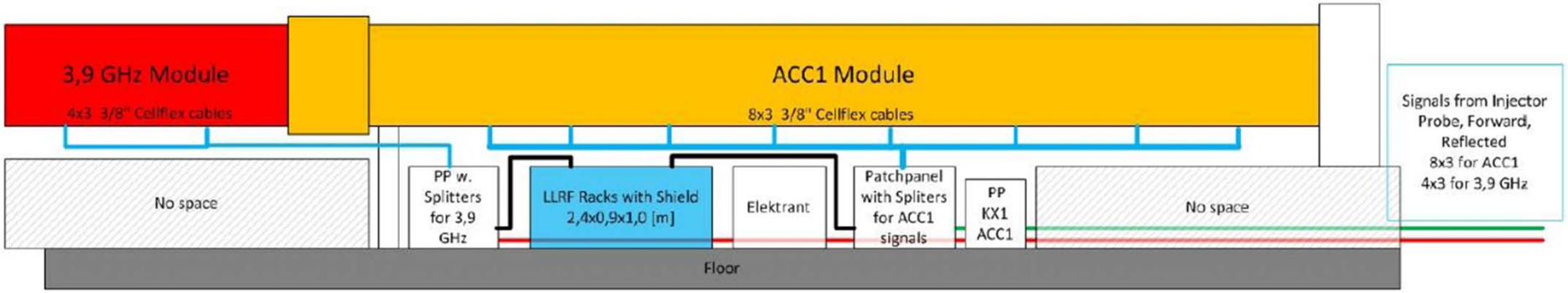
name: ***TMCB1***
version: *A*
variant: *Master*
I-Tech Code: *4205*

Planned LLRF upgrades at FLASH

FIL

2011

• REGAE	(May-July)	1 Crate (8)	
• FLASH ACC1	(July-Sep)	1 Crate (24)	Test & Software
• PITZ TDS	(Aug-Sep)	1 Crate (8)	
• CMTB	(Sep)	1 Crate (24)	
• Racks ACC67	(Sep-Dec)		Ext. Hall 3
• Racks ACC1/ACC39	(Sep-Dec)		Tunnel (preparation)
• Racks ACC23	(Sep-Dec)		Tunnel (preparation)



2012

• FLASH ACC23	(Spring)	1 Crate (48)
• FLASH ACC67	(Spring)	1 Crate (48)

Planned LLRF upgrades at FLASH

- **Test of long-term and short-term stability at FLASH.**
- **Investigate possible improvements on the beam and SASE.**

Thanks for your attention!