

# Bunch Arrival-Time Monitor Electronics & Software Developments

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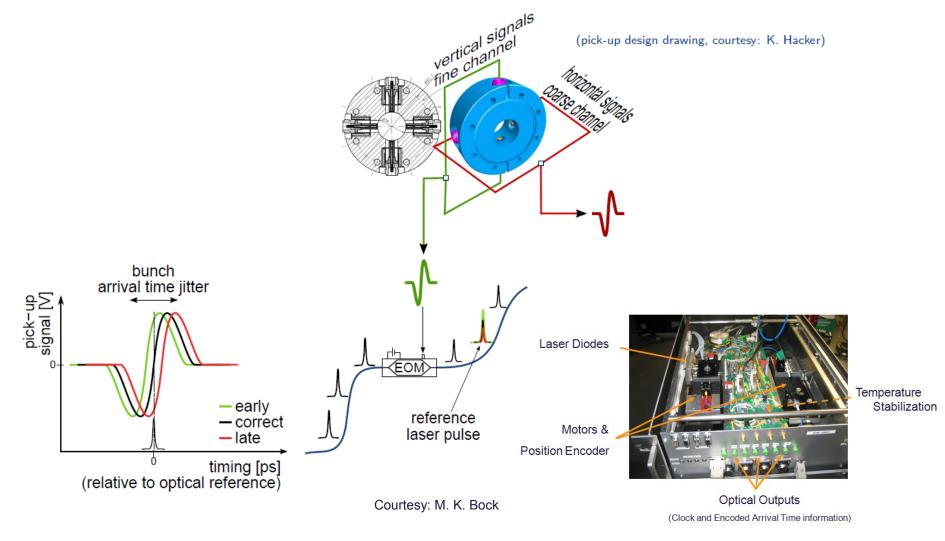
- From Bunch to Arrival-Time Feedback
- Current implementation
  - Hardware
  - Firmware
  - Software
- Functions to be added
- Next Generation developments





#### From Bunch to Arrival-Time Feedback (I)

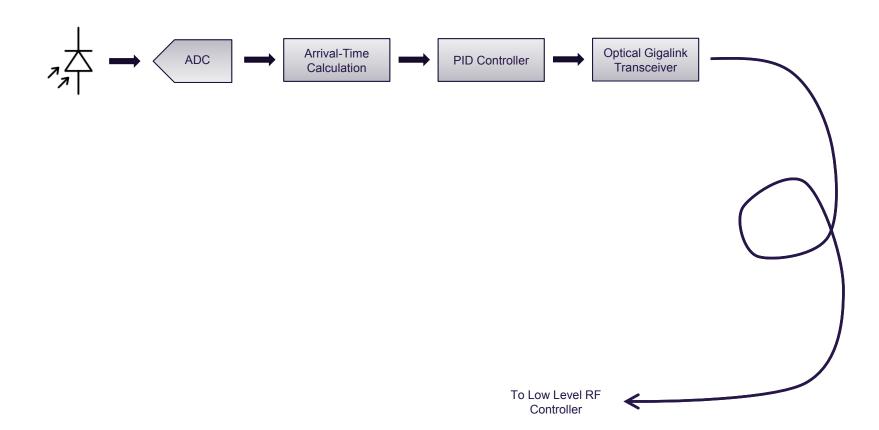






#### From Bunch to Arrival-Time Feedback (II)

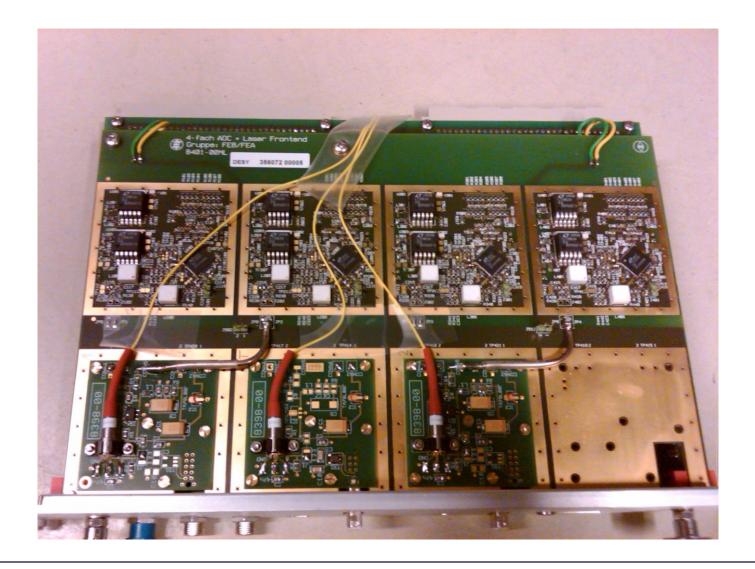






## XFEL Current Hardware: ADC Board with Front-end



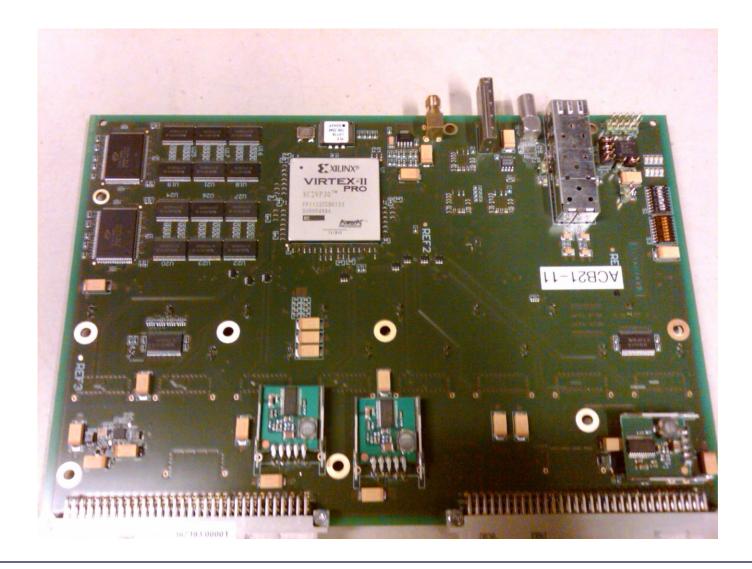






# XFEL Digital VME Advanced Carrier Board (ACB2.1)

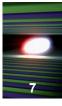








#### **\_ Tasks of the BAM Readout Hardware** ■



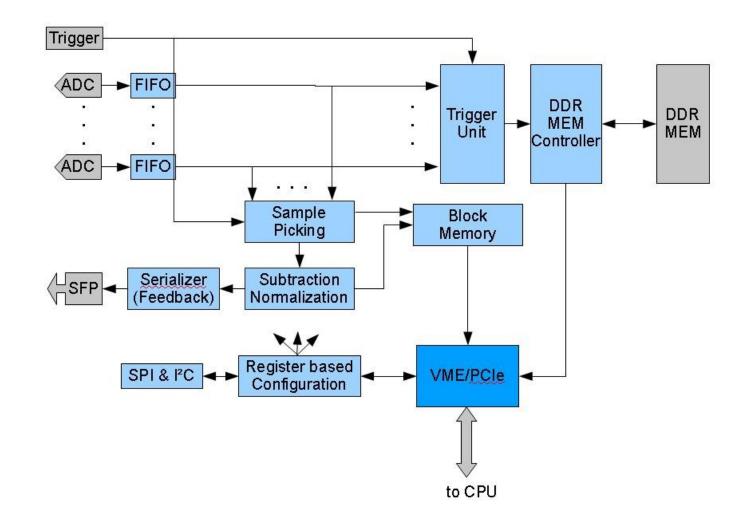
- Convert optical pulses to electrical ones
- "Generate" a stable clock
- Sample the signals
- Calculate bunch arrival-times (at least values proportional to them)
- Implement PID controller and high-speed serial link for Fast Feedback
- Offers high speed/ DMA Transfer to CPU





#### Simplified block diagram of Firmware



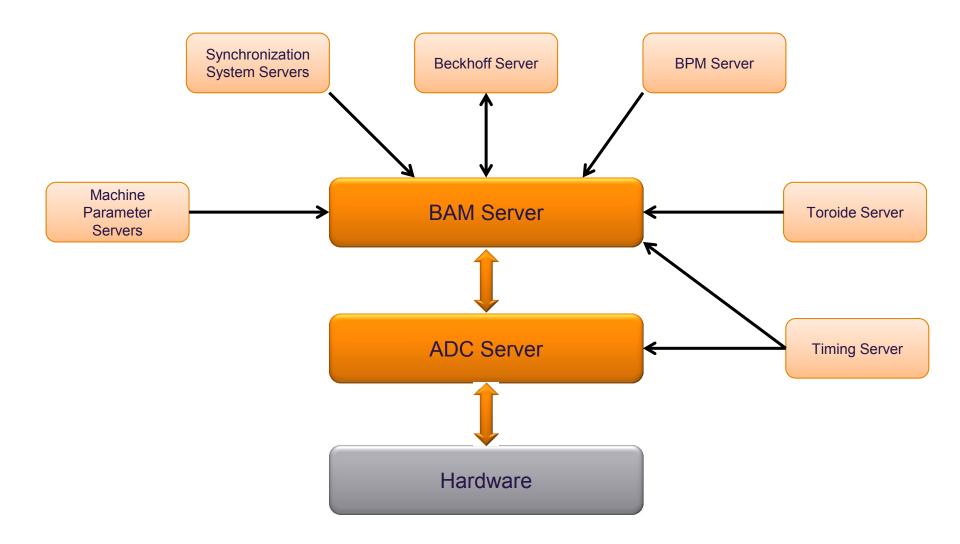






## XFEL Software Structure





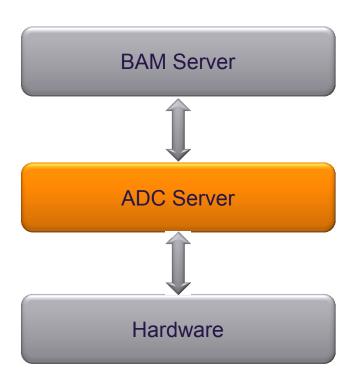




#### FEL Tasks of the ADC Server



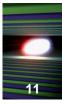
- Fast read out of data from hardware
- Synchronization of event number and data
- Configuration of hardware
- Sending data to DAQ



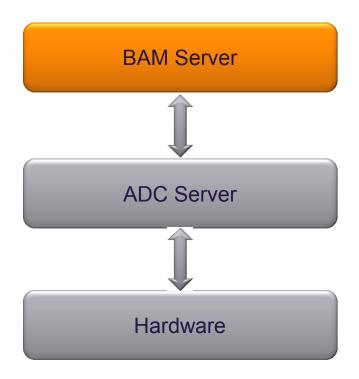




#### FEL Tasks of the BAM Server



- Calculate
  - Bunch Arrival-Times
  - Jitter
  - Resoluion
- Calibration
- Adjustment of delay stages
- Requires data from
  - ADC/ACB Server
  - Toroids
  - BPM
  - Position encoder in frontend
  - Machine parameters







#### Functions to be added



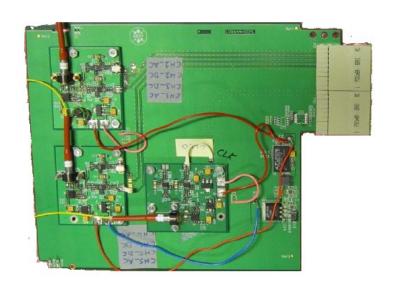
- Readout of motor position encoder in FPGA
  - Real time correction of motor movements
  - Calculation of absolute arrival-time in FPGA
- Control loop to optimize polarization → optical power
  - Optimize signal-to-noise ration at ADCs
- Remove reading / processing of duplicated data





#### XFEL Next generation developments







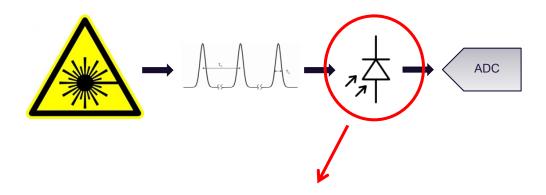
- Based on 10 CH, 125MSPS, 16Bit ADC Board from Struck (SIS8300)
- Includes powerful FPGA, high-speed serial ports
- Signal conversion, amplification and splitting on Rear Transition Module (RTM)

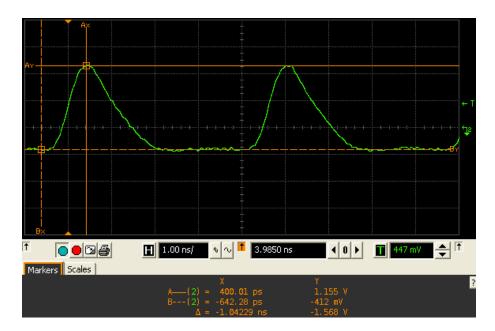




#### Critical aspect: Signal conversion and splitting



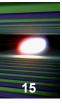








#### \_ Alternative Development



- 2 CH, 500MSPS ADCs
- > 1GHz analog input bandwidth
- Combined with signal conversion and clock generation on one PCB
- Implemented as
  - Double size FPGA Mezzanine Card (FMC)
  - or Rear Transition Module
- Connecting to a digital Advanced Mezzanine Card





#### FEL Next Steps



- Implementation and tests of the "Functions to be added"
- Performance measurements of the 125MSPS board with RTM solution and further developments towards complete RTM
- Test at FLASH with beam based feedback

