

PCIe Gen4/5 and 100G-Ethernet on mTCA platform



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mTCA applications / mTCA-NG working group motivation

Industry



Telecommunication



Medicine



Physics



The most of these applications have one thing in common:
need for higher data rates

Defence



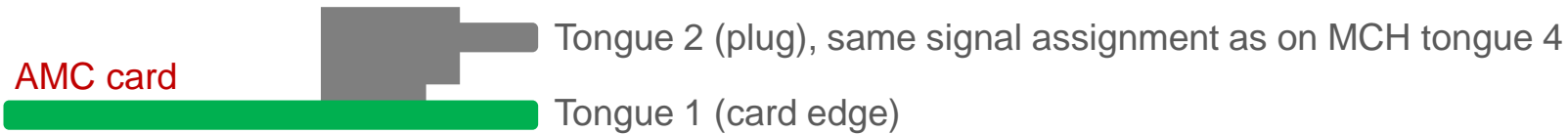
**SI goal of the PICMG mTCA-NG working group:
implementation of the latest bus generations PCIe Gen4/5 and 100Gbps ethernet**

mTCA, new connectors

SI improved connectors from Yamaichi and Amphenol (backplane and MCH-plug tongue 2)



AMC-card second tongue (more power and wider data planes for AMC)



New HUB connector, **ExaMAX** from Amphenol and Samtec

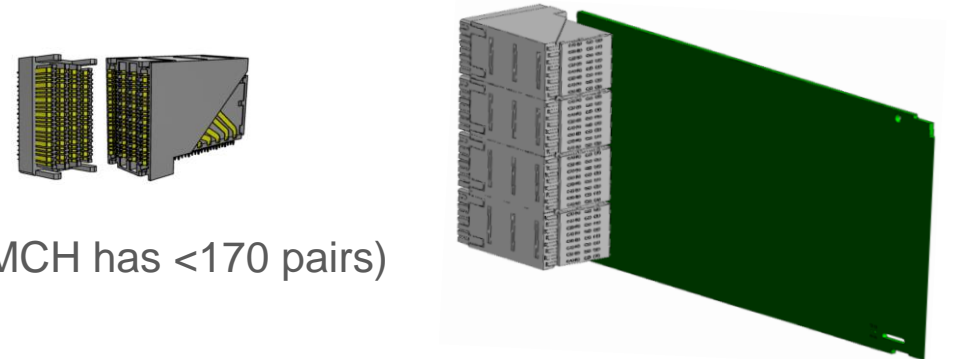
PCIe Gen4/5 and 100Gbps Ethernet capable

with **4 connectors** up to **192 pin pairs** on MCH realizable (current MCH has <170 pairs)

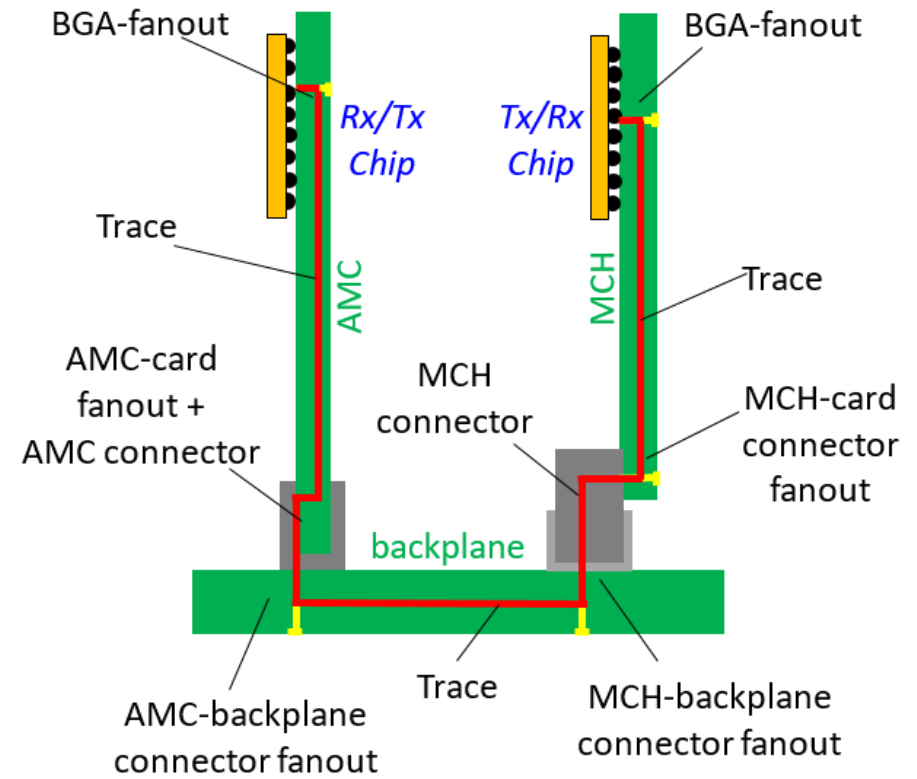
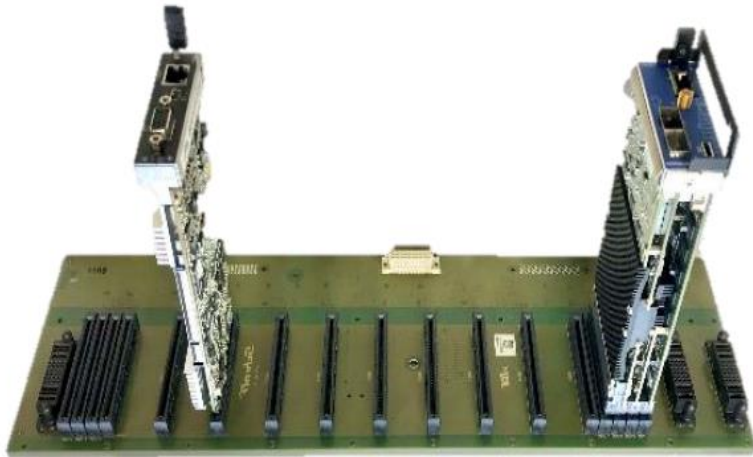
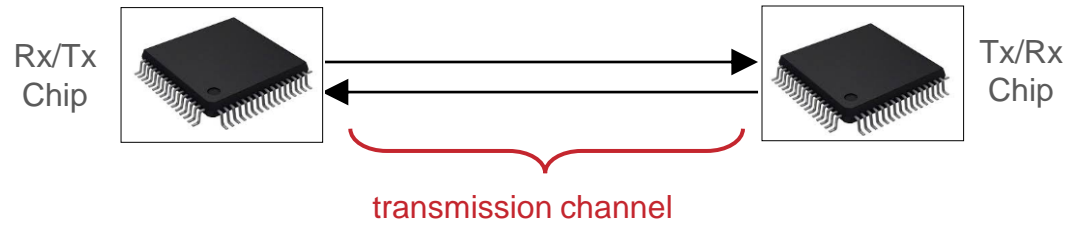
new, x-talk optimized signal assignment (Rx/Tx allocation)

MCH-card pn: **not finally decided** (e.g. Samtec EBTF-6-08-2.0-S-RA-1 or Amphenol 10131762-101LF)

Backplane pn: **not finally decided** (e.g. Samtec EBTM-6-08-2.0-S-VT-1 or Amphenol 10124752-101LF)



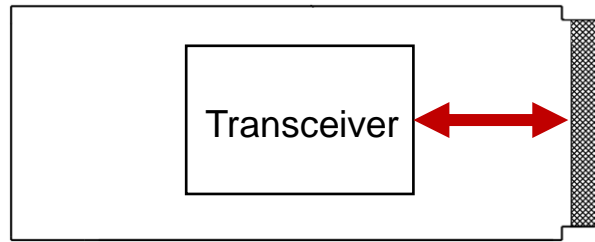
mTCA transmission channel (PCIe or Ethernet)



mTCA, 3D-model parameters

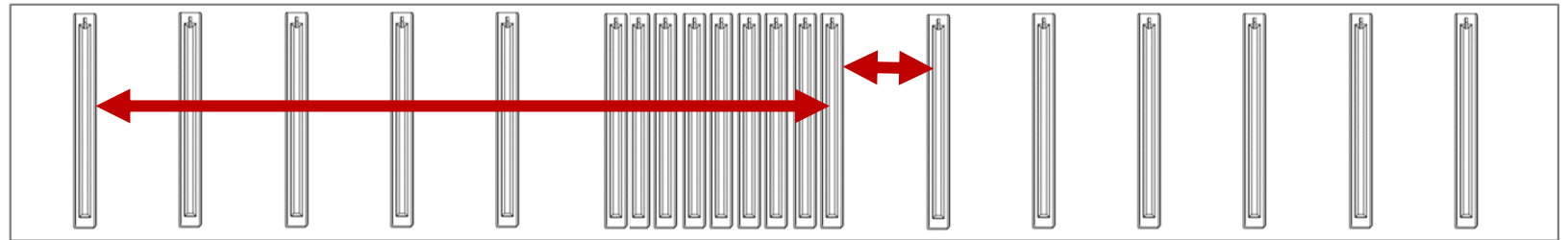
Min and max trace length:

AMC/MCH card



min trace length: 25mm (1 inch)
max trace length: 127mm (5 inch)

Backplane



min trace length: 50mm (2 inch)
max trace length: 250mm (9.8 inch)

PCB material:

For all cards: [Isola Tachyon100G](#) (typ. Dk 3.02 Df 0.0021 @10GHz)

For backplane: [Elite Material EM-891K](#) (typ. Dk 3.1 Df 0.0024 @10GHz)

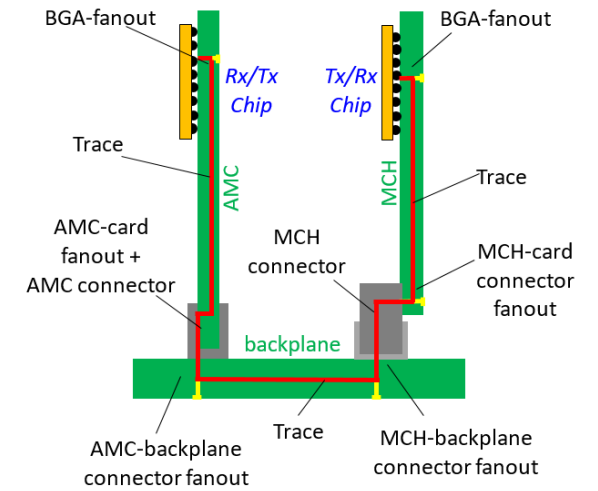
Diff pair impedance:

For PCIe and Ethernet busses: 90Ω

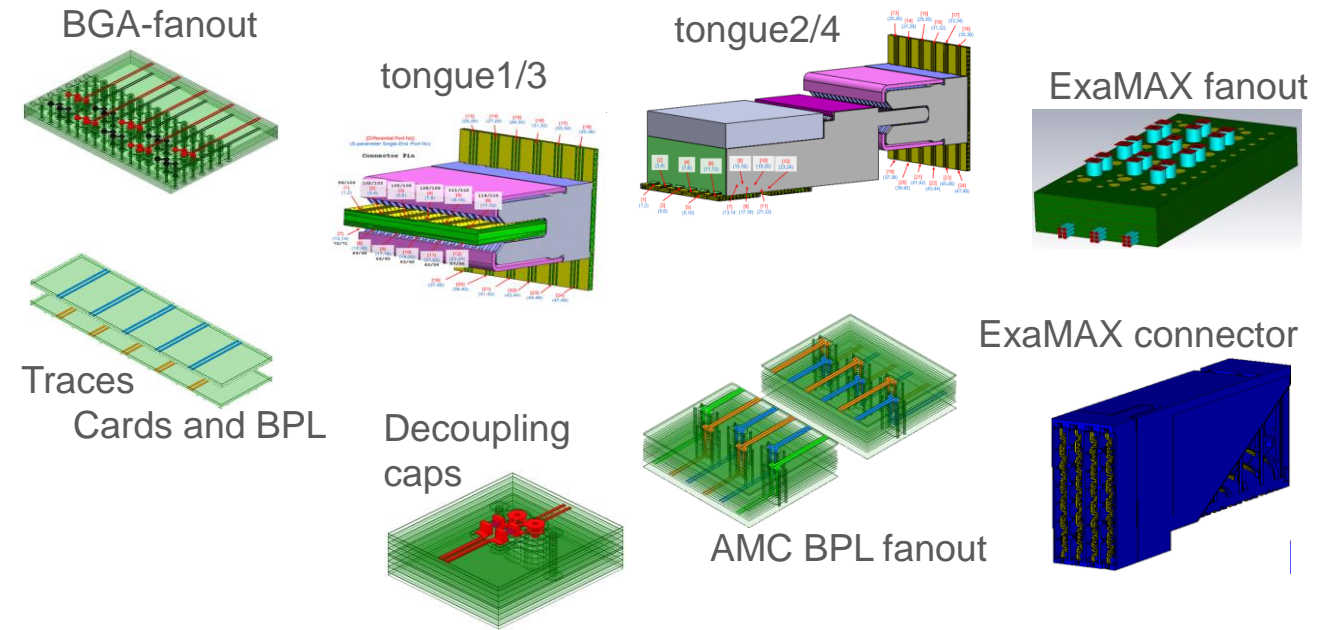
mTCA, 3D-model parameters

Channel segment parameters were defined in the group and based on realistic dimensions and routing strategies for AMC/MCH-cards and mTCA-backplanes:

- PCB stack-ups
- Routing layers
- differential trace dimensions
- BGA and connector fanouts
- Signal assignment/pinout
- Via, pad, anti-pad, backdrill ... geometries
- allocation of x-talk aggressors
- ...



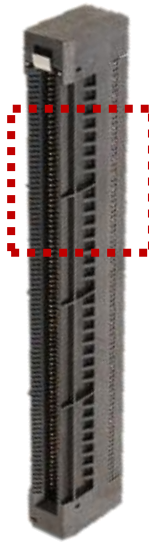
3D Models (simulated with CST and HFSS software):



mTCA, 3D-model parameters

Numbers of x-talk aggressors in the connector determines the 3D-model size

highest x-talk in the channel is caused by the connectors.



73	GND	GND	98
72		Rx10	99
71		F3	100
70	GND	GND	101
69	Rx7	Tx10	102
68	Rx7	Tx10	103
67	GND	GND	104
66	N2	Rx11	105
65	Tx7	Rx11	106
64	GND	GND	107
63	Rx6	Tx1	108
62	Rx6	Tx1	109
61	GND	GND	110
60	Tx6	Rx12	111
59	Tx6	Rx12	112
58	GND	GND	113
57		Tx12	114
56		Tx12	115
55	GND	GND	116

Model size
(number of diff pairs)

For example 10 diff pairs
for AMC tongue 1

3D Models (simulated with CST and HFSS software):

BGA-fanout

Traces
Cards and BPL

Decoupling caps

AMC BPL fanout

tongue1/3

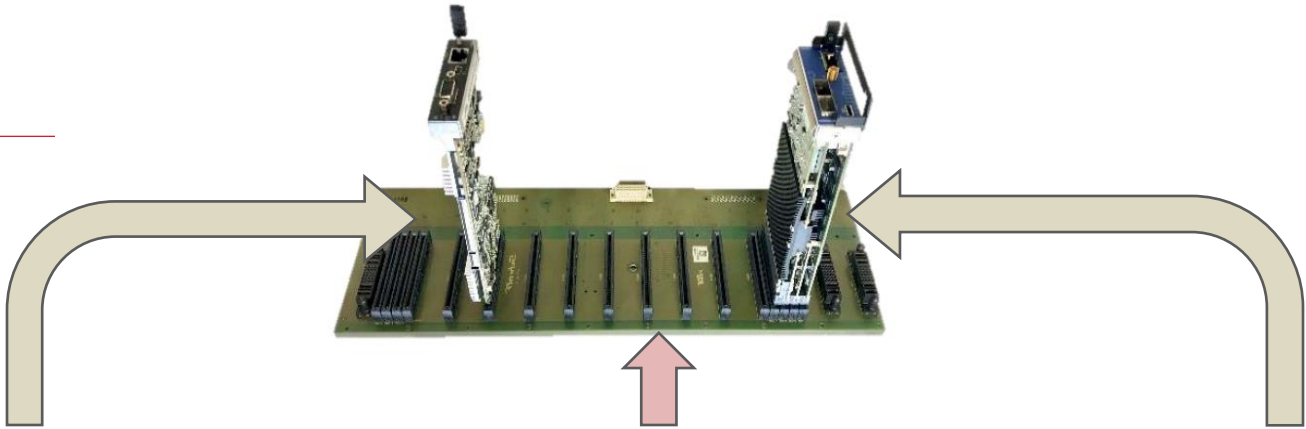
tongue2/4

ExaMAX fanout

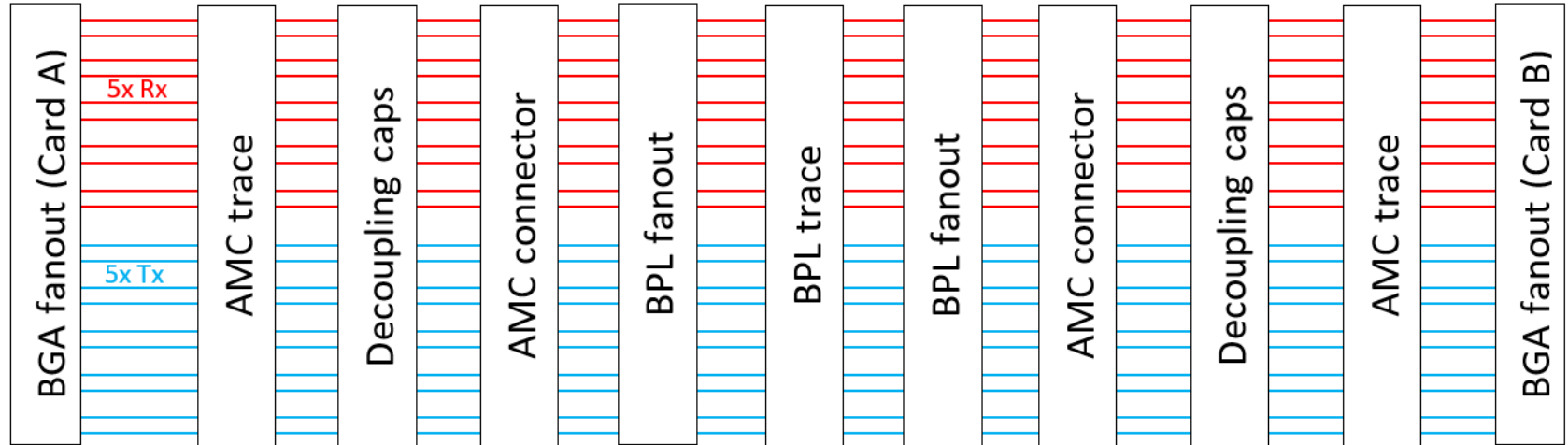
ExaMAX connector

Description and S-parameter of all 3D-models can be downloaded from PICMG mTCA-NG working group area

mTCA channel composition



AMC A card			AMC connector Tongue 1	Backplane			AMC connector Tongue 1	AMC B card		
BGA fanout <i>(start point)</i>	AMC trace	Decoupling caps		BPL fanout	BPL Trace	BPL fanout		Decoupling caps	AMC trace	BGA Fanout <i>(end point)</i>



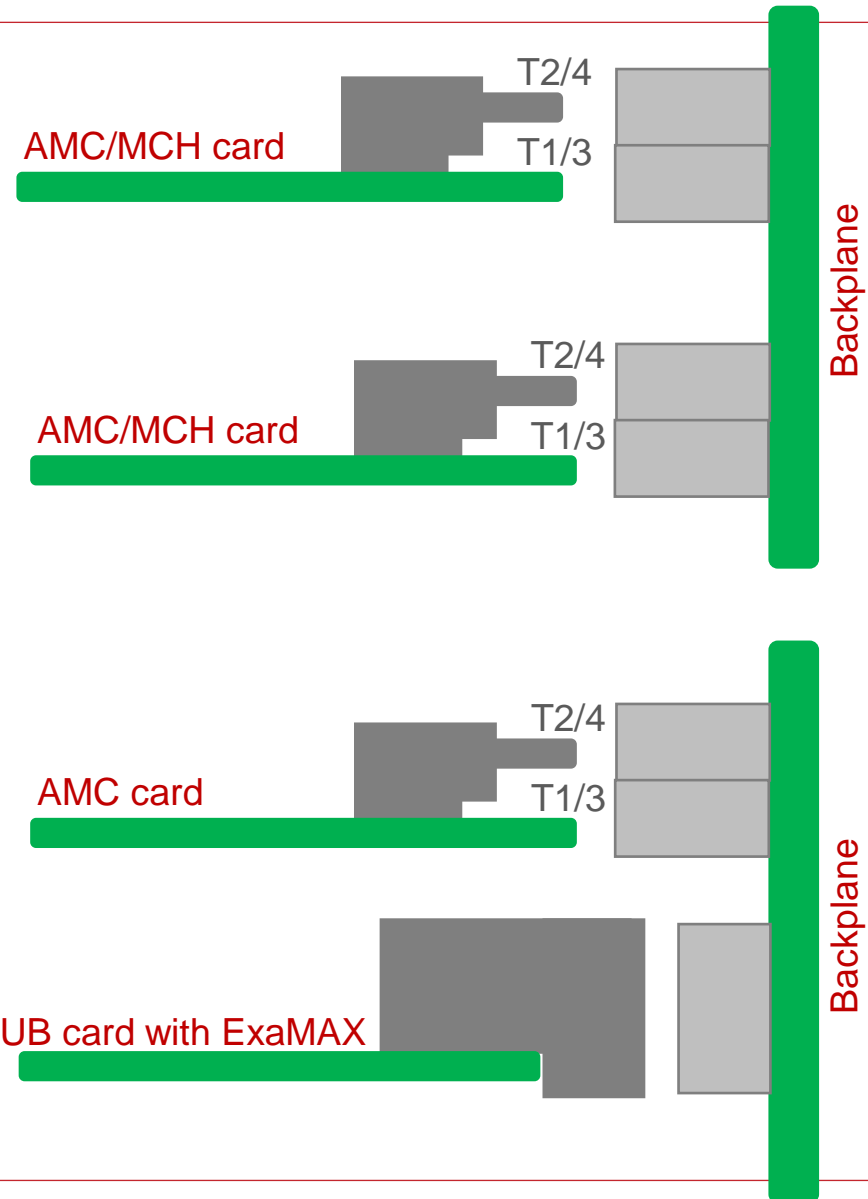
mTCA, simulation cases

Interconnection groups with existing connectors:

1. AMC_T1 to AMC_T1
2. AMC_T1 to AMC_T2 (AMC_T1 to MCH_T4)
3. AMC_T2 to AMC_T2 (MCH_T4 to MCH_T4)

Interconnection groups with ExaMAX connector:

4. AMC_T1 to HUB
5. AMC_T2 to HUB



mTCA, simulation cases

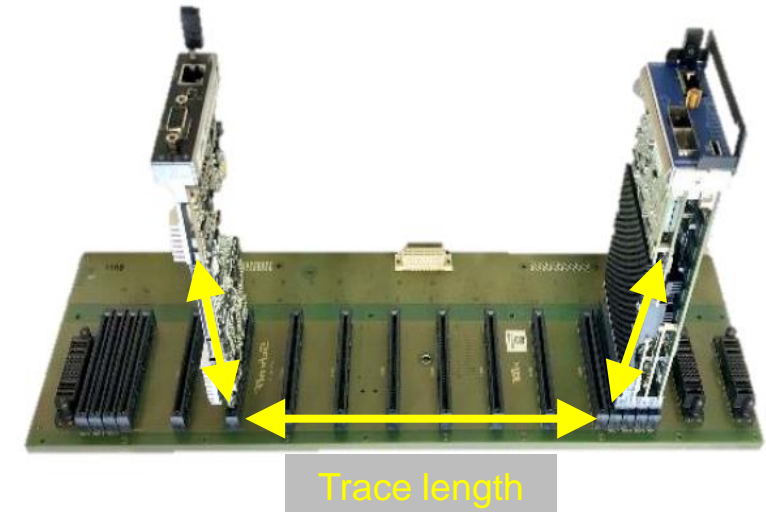
Corner cases (channels with the most critical parameters)

min trace length -> maximal Re-Reflections

max trace length -> worst case ICR (Insertion loss to Cross talk Ratio)

Cases for **AMC_T1 to AMC_T1** interconnection group:

Case	card A (trace length / impedance)	Tongue 1 connector	BPL (trace length / impedance)	Tongue 1 connector	card B (trace length / impedance)
AMC_T1_AMC_T1_Case 1	25mm / 90Ω	Yamaichi	50mm / 90Ω	Yamaichi	25mm / 90Ω
AMC_T1_AMC_T1_Case 2	25mm / 90Ω	Yamaichi	50mm / 90Ω	Yamaichi	127mm / 90Ω
AMC_T1_AMC_T1_Case 3	25mm / 90Ω	Yamaichi	250mm / 90Ω	Yamaichi	25mm / 90Ω
AMC_T1_AMC_T1_Case 4	25mm / 90Ω	Yamaichi	250mm / 90Ω	Yamaichi	127mm / 90Ω
AMC_T1_AMC_T1_Case 5	127mm / 90Ω	Yamaichi	50mm / 90Ω	Yamaichi	25mm / 90Ω
AMC_T1_AMC_T1_Case 6	127mm / 90Ω	Yamaichi	50mm / 90Ω	Yamaichi	127mm / 90Ω
AMC_T1_AMC_T1_Case 7	127mm / 90Ω	Yamaichi	250mm / 90Ω	Yamaichi	25mm / 90Ω
AMC_T1_AMC_T1_Case 8	127mm / 90Ω	Yamaichi	250mm / 90Ω	Yamaichi	127mm / 90Ω



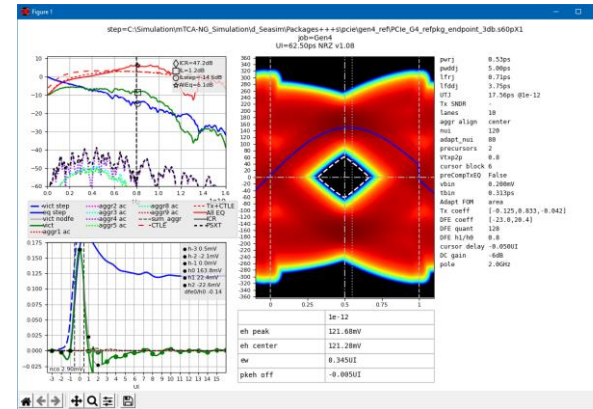
In total 88 channel cases for all 5 interconnection groups
(AMC connector vendors: Yamaichi and Amphenol)

mTCA, channel verification

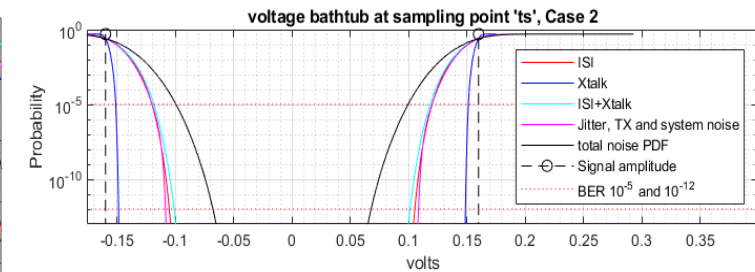
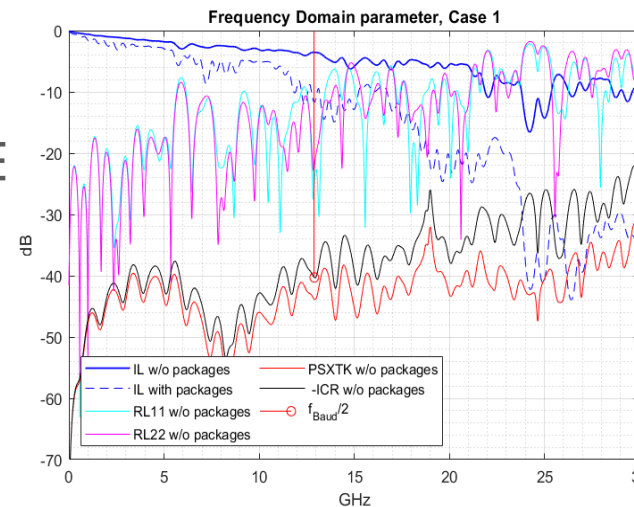
In all 88 channel cases it was checked whether their parameter were complied with specification requirements:

For PCIe Gen4/5, the Seasim tool from PCI-SIG was used ([seasim-release 1.08](#))

(transceiver reference packages from PCI-SIG were used for eye simulation)



For 100GBASE-KR4, MATLAB tool from IEEE was used ([ran_com 3bj 3bm 01 1114](#))



Transmitter and Receiver equalizer settings, Case 2	
FFE taps:	[-0.12, 0.86, -0.02]
CTLR gain:	0 dB
DFE taps [1:7]:	[0.3187, 0.1072, 0.0560, 0.0254, 0.0183, 0.0224, 0.0153]
DFE taps [8:14]:	[0.0161, 0.0046, -0.0282, 0.0474, 0.0193, 0.0246, 0.0046]

Channel Operating Margin (COM) @ DER0=1e-05, Case 2 [dB]: **8.17**

mTCA, simulation results

Trace length were updated:

AMC/MCH card:

min trace length: ~~25mm~~ 35mm

max trace length: 127mm

Backplane:

min trace length: ~~50mm~~ 60mm (100mm for HUB channels)

max trace length: 250mm

All 88 channel cases fulfils PCIe Gen4/5 and 100GBASE-KR4 requirements

- Worst case PCIe Gen4/5 eye opening: $\geq 20.7\text{mV}$ / $\geq 0.301\text{UI}$ (Pass criteria: 15mV / 0.3UI)
- Worst case 100GBASE-KR4 COM Value: $\geq 3.47\text{dB}$ (Pass criteria: 3dB)

Conclusion:

- PCIe Gen4/5 and 100GBASE-KR4, are realizable on mTCA platform
- 100% backward compatibility can be insured with the improved AMC connectors from Yamaichi and Amphenol
- All Channels with the ExaMAX connector meet the requirements

Evaluation concept

(compliance testing)

mTCA, evaluation

current situation:

- SI-parameter/limits and test procedures for AMC/MCH cards and mTCA backplane are defined for 10/40Gbps Ethernet only (MTCA.0 R2.0 Annex B)
- For PCIe Gen3 no limits and test procedures are defined -> interoperability problems

=> the goal is to insure the interoperability between different card and backplane vendors

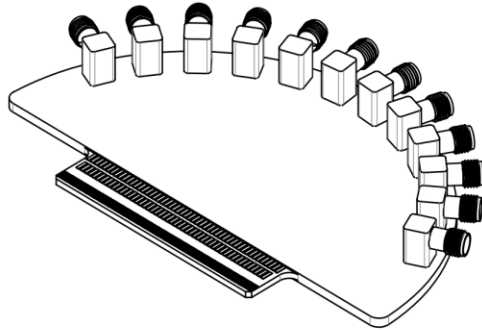
mTCA, evaluation

test adapters for measurements

- test cards replicates worst case cards (with longest and shortest traces)
- test backplane replicates worst case backplanes (with longest and shortest traces)

test cards

(with parameters of AMC/MCH cards with min and max trace length)



test backplanes

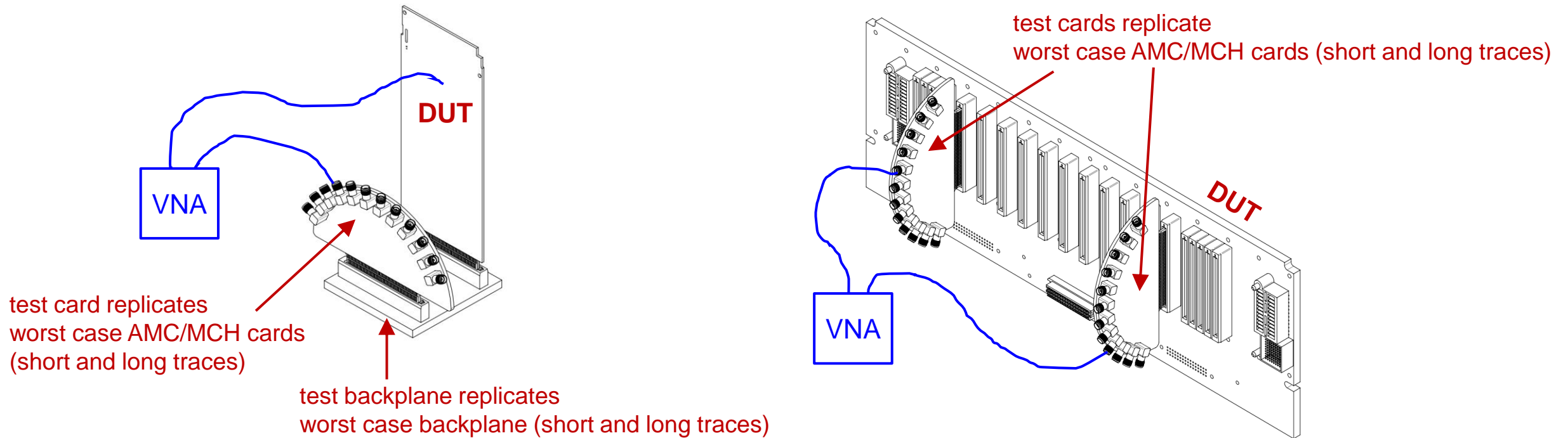
(with parameters of backplanes with min and max trace length)



mTCA, evaluation

100GBASE-KR4 evaluation:

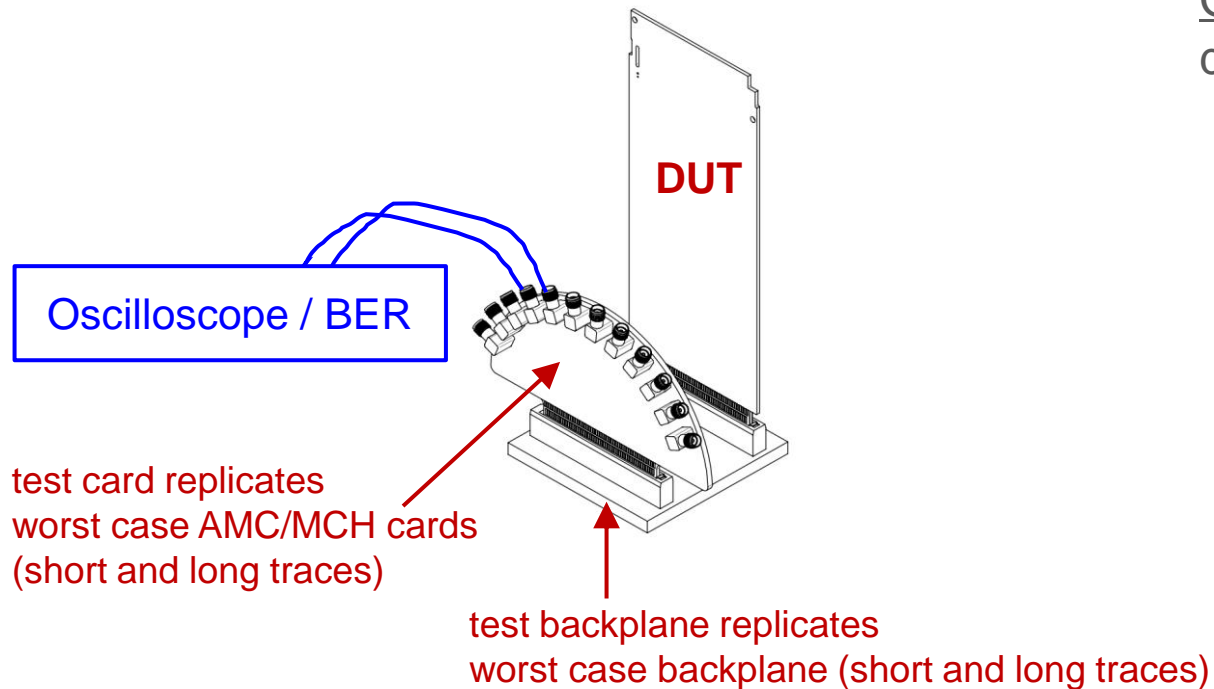
- same approach as defined in PICMG ATCA specification (PICMG 3.1 R3.0)
- measurement of DUT parameters in frequency domain in combination with worst case paddle cards and test backplanes
- calculation of COM value (Channel Operating Margin), shall be $>3\text{dB}$



mTCA, evaluation

PCIe Gen4/5 evaluation:

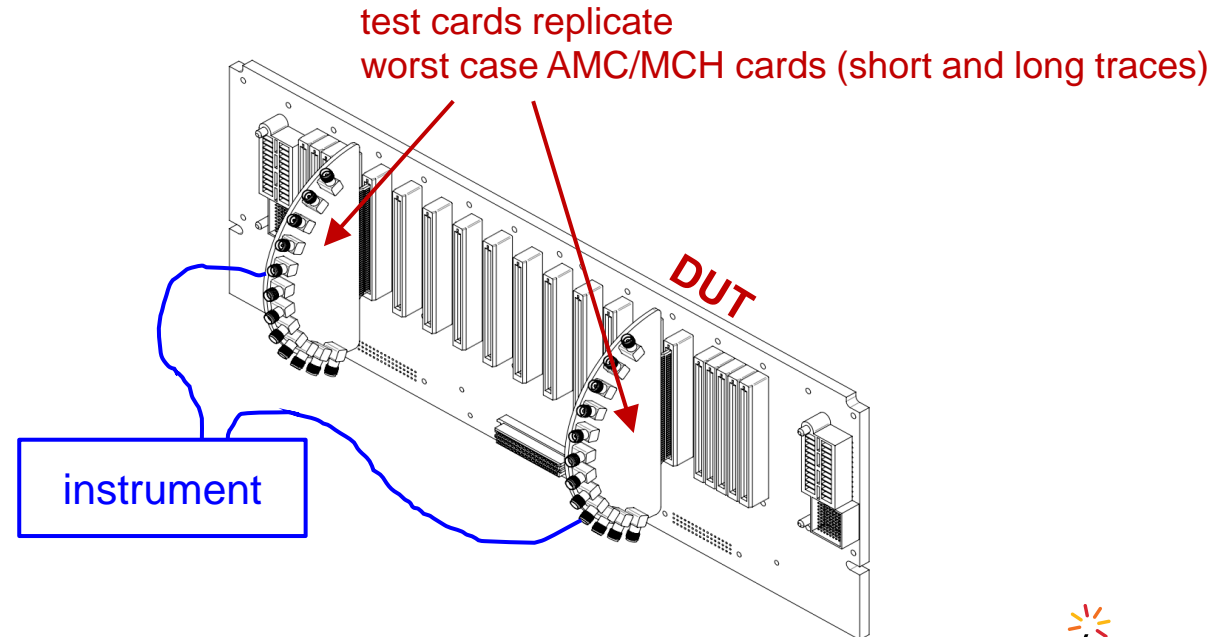
- Approach as defined in PCIe specification
- **For cards:**
measurement of eye opening in combination with worst case paddle cards and test backplanes



- **For backplane (TBD):**

Option 1: measurement of eye opening in combination with worst case paddle cards by using BER + Oscilloscope

Option 2: measurement of DUT parameters in frequency domain and calculation of the eye opening (e.g. in Seasim)



Thank you