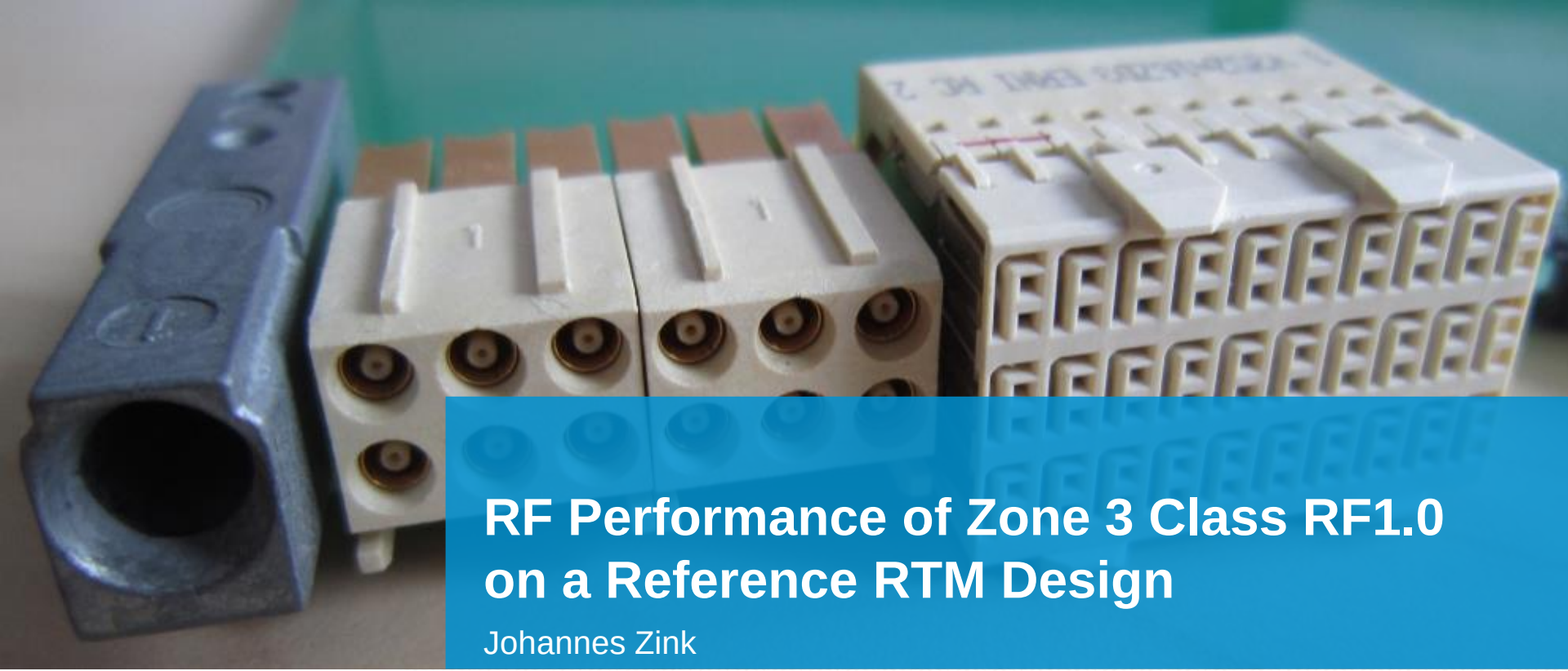


RF Performance of Zone 3 Class RF1.0 on a Reference RTM Design

Johannes Zink

MicroTCA TECHNOLOGY LAB

DESY.

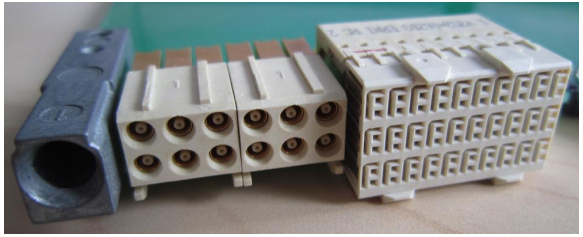
OUTLINE

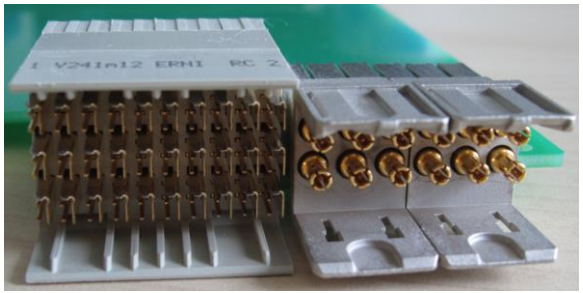
1. Zone 3 class RF1.0 for MTCA.4 – Coaxi Pack 2 connector
2. Coaxi Pack 2 isolation measurements for THT and SMD variants
3. first AMC – RTM combination + RF performance
4. conclusion and outlook

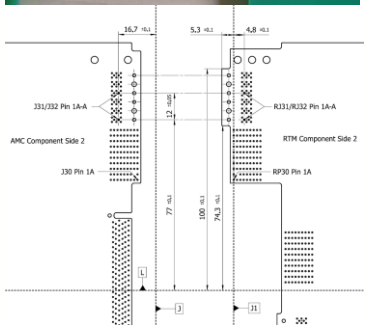
Zone 3 Class RF1.0 reminder

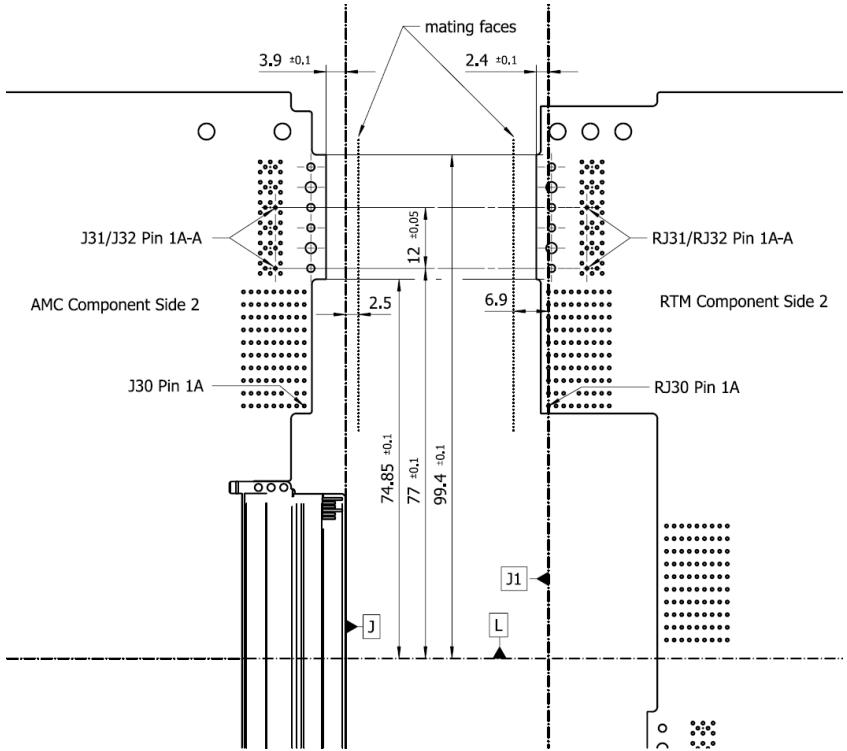
- single-ended coaxial connectors Radiall Coaxi Pack 2
- signals up to 3 GHz can be transmitted from / to RTM side

courtesy of Robert Wedel





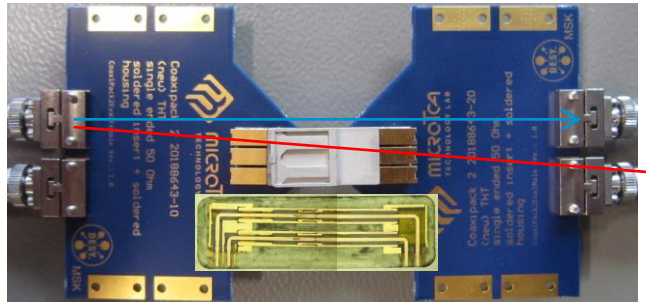


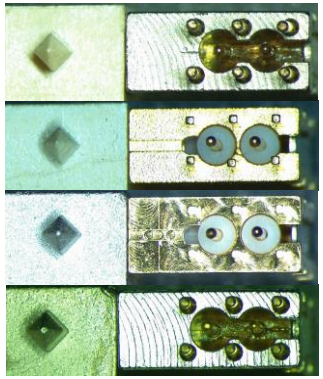


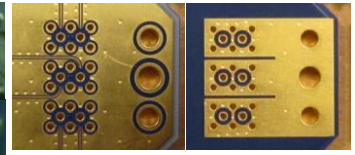
Coaxi Pack 2 THT Measurements (MTCAWS 2019)

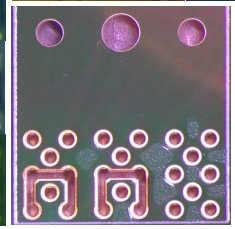
intra insert crosstalk

- near-end (NEXT)
- far-end (FEXT)



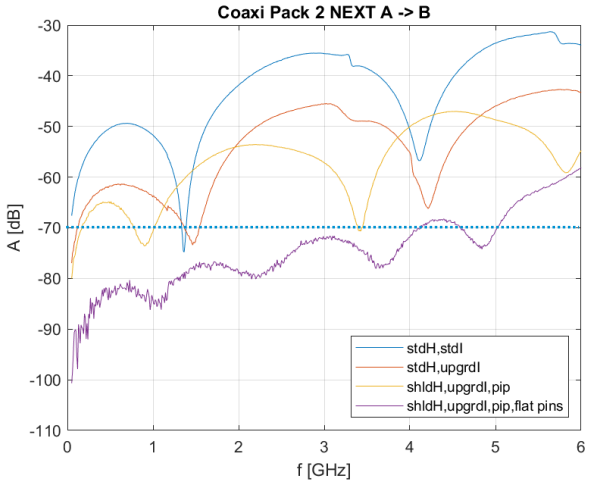




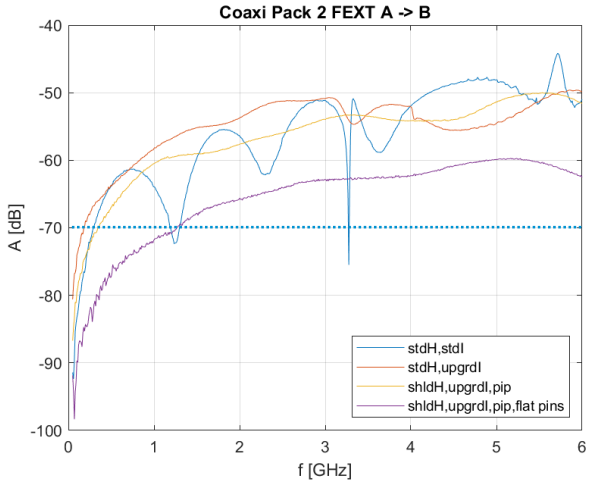


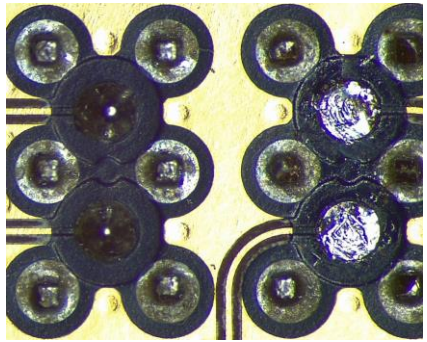
courtesy of Szymon Jablonski

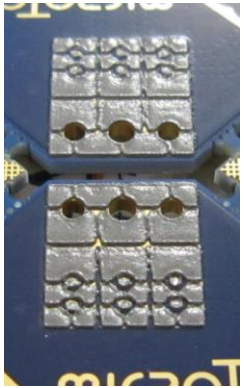
S_{21}



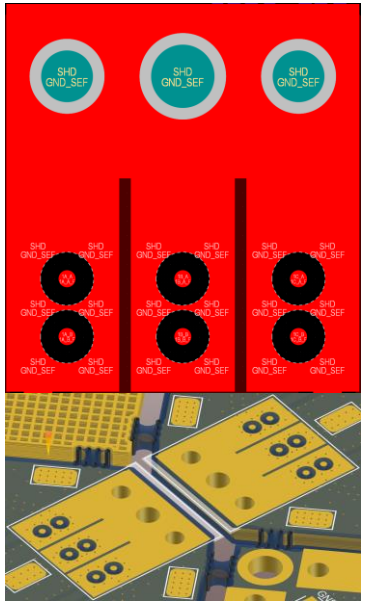
S_{31}

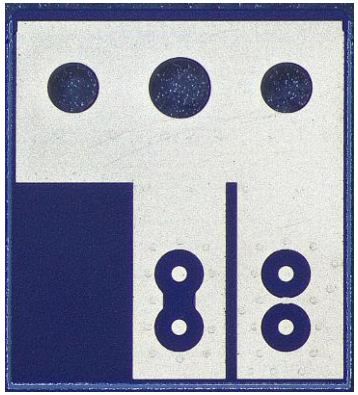


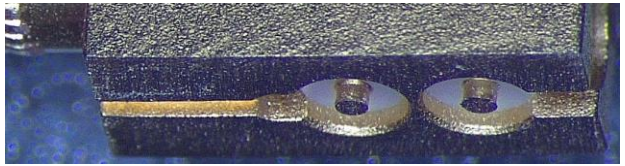




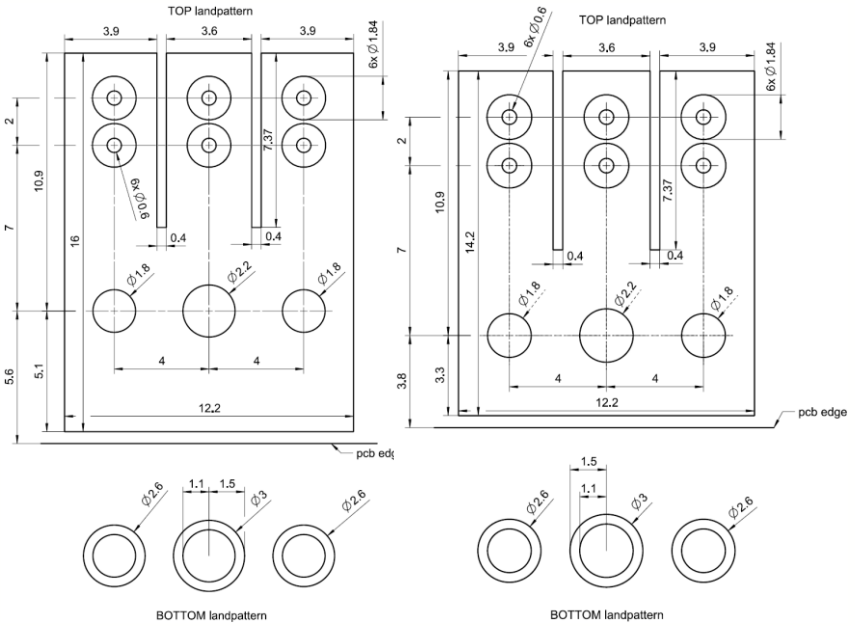
Coaxi Pack 2 SMD Footprint







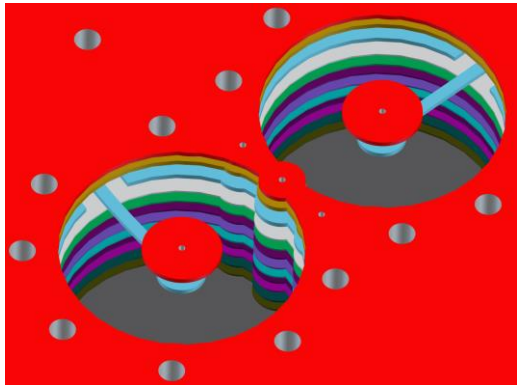
Radiall

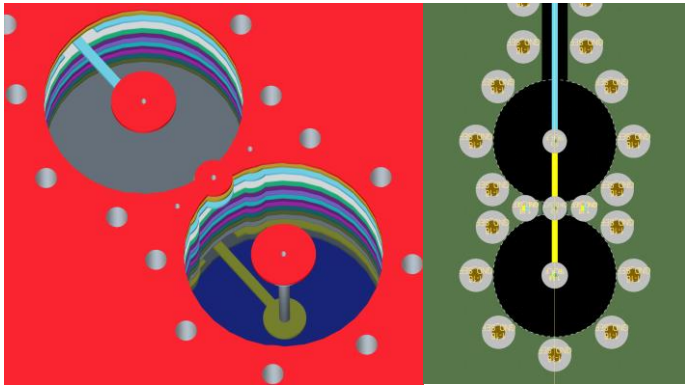


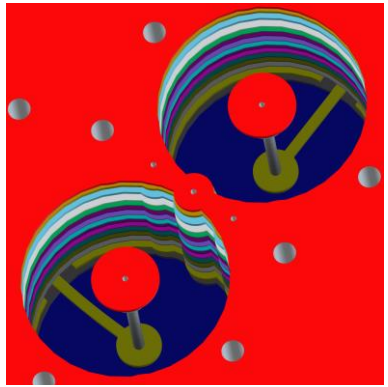
- based on the THT measurements an SMD footprint was created
- simply removed the pins from the insert and sanded them down
- created new evaluation modules with the SMD footprint

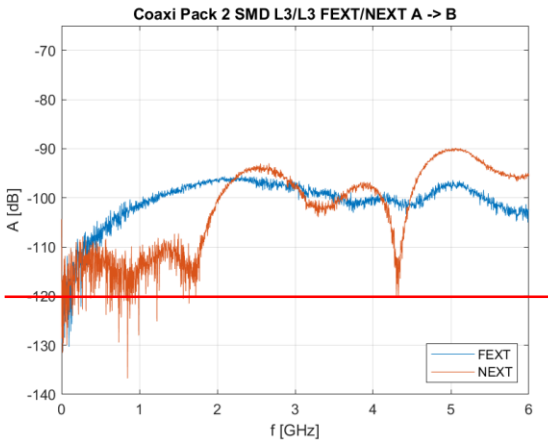
Coaxi Pack 2 SMD landpattern recommendation
(can be found in the Zone 3 class RF1.0 recommendation)

Coaxi Pack 2 SMD X-talk S_{21} / S_{31}

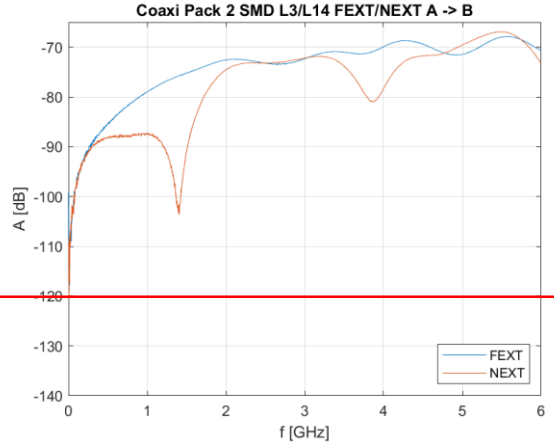


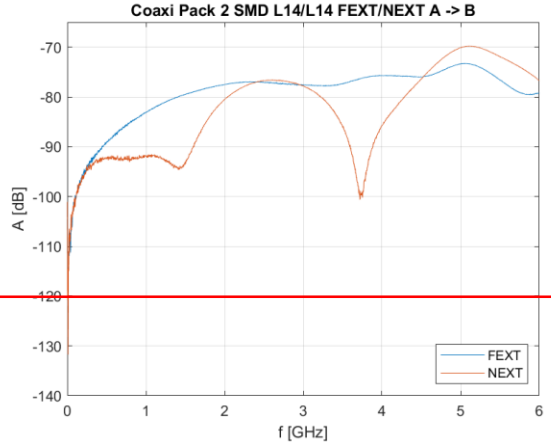




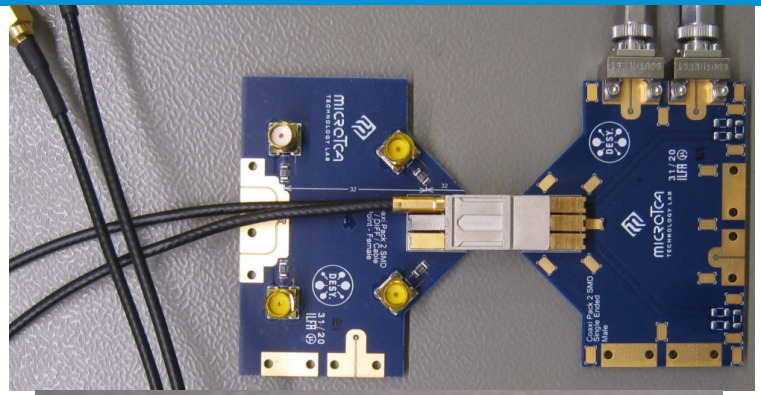


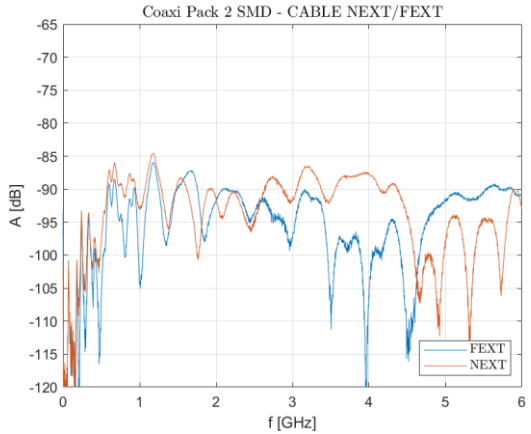
VNA noise floor

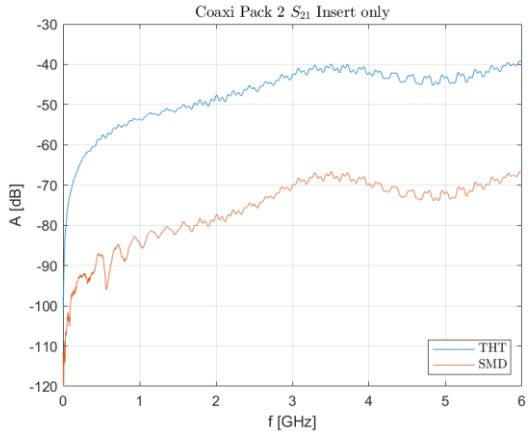




Coaxi Pack 2 SMD → Cable X-talk S_{21} / S_{31}







cable feed

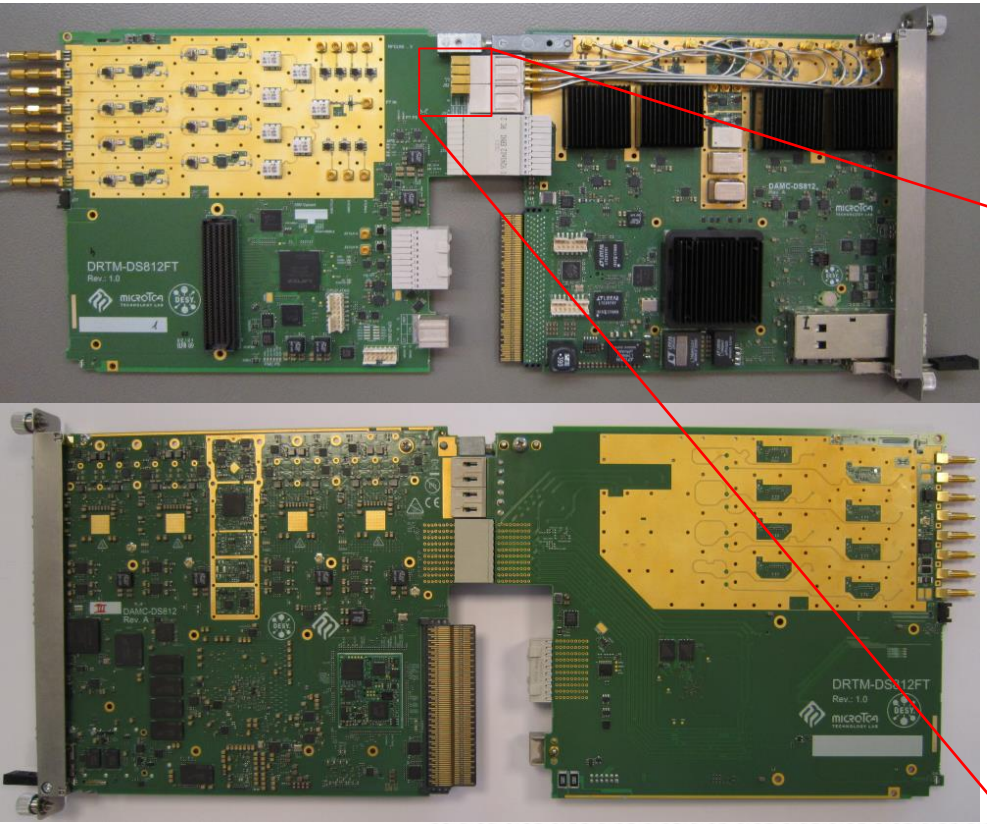
- isolation depends on the cables
- nearly same performance as SMD PCB mounting

insert only crosstalk

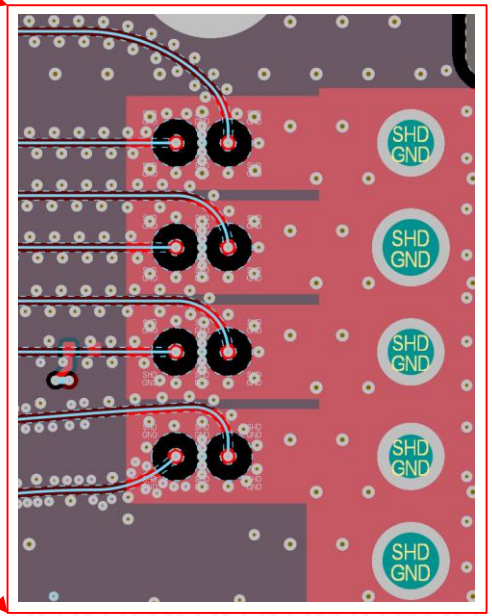
- strong coupling between THT pins
- SMD variant has significantly better isolation

Zone3 RF1.0 AMC – RTM Combination

DRTM-DS812FT DAMC-DS812ZUP



- SMD PCB connection on RTM side
- phase matched cable feed on AMC side
- cables made by elspec group GmbH



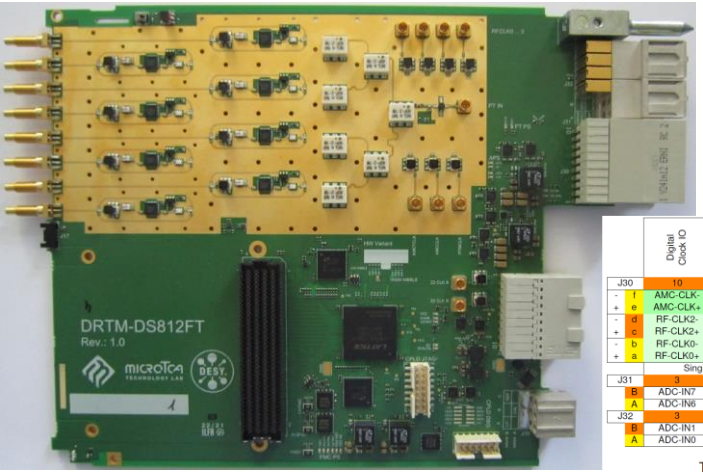
- 8 channel 12-bit ADC board
- 4 dual channel ADC chips
- cable connection from Zone 3 or front panel to ADC front-ends

- for more information about DAMC-DS812ZUP see:

Latest Hardware Developments in MicroTCA.4 by Michael Fenner

Thursday 12:35 – 12:50

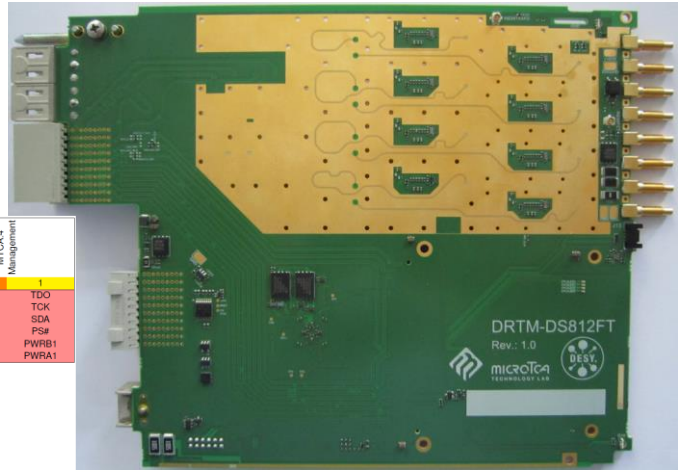
DRTM-DS812FT



		Digital Clock IO	Digital fixed IO	Digital Clock Input	Digital user IO		Standard Gbit-Links			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D7-	RF-CLK3-	D5-	D2-	GBT7-TX-	GBT4-TX-	GBT1-TX-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D7+	RF-CLK3+	D5+	D2+	GBT7-TX+	GBT4-TX+	GBT1-TX+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D6-	RF-CLK1-	D4-	D1-	GBT6-TX-	GBT3-TX-	GBT0-TX-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D6+	RF-CLK1+	D4+	D1+	GBT6-TX+	GBT3-TX+	GBT0-TX+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	D3-	D0-CC-	GBT5-TX-	GBT2-TX-	GBT0-RX-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	D3+	D0-CC+	GBT5-TX+	GBT2-TX+	GBT0-RX+	PWRA2	PWRA1

		Single Ended Analog Signals		
J31		3	2	1
	B	ADC-IN7	DAC-OUT1	DAC-OUT3
	A	ADC-IN6	DAC-OUT0	DAC-OUT2
J32		3	2	1
	B	ADC-IN1	ADC-IN3	ADC-IN5
	A	ADC-IN0	ADC-IN2	ADC-IN4

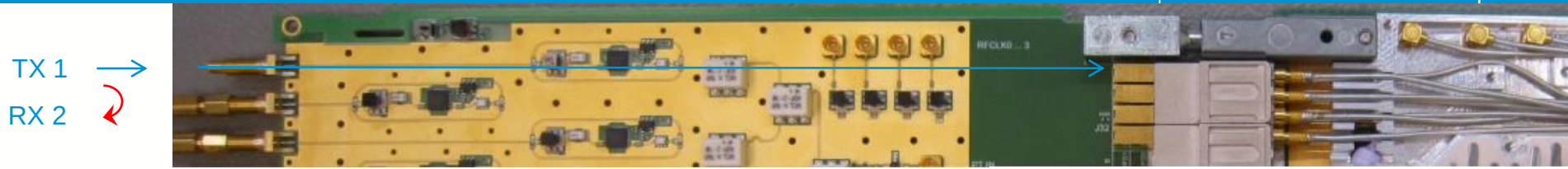
Table 1: Zone 3 - Class RF1.0 pin assignment J30, J31 and J32 connector, AMC side view

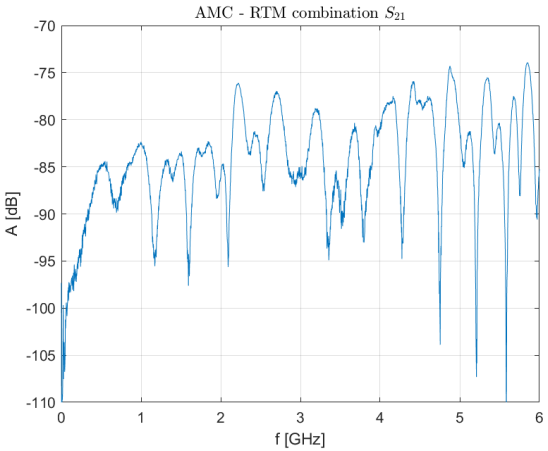


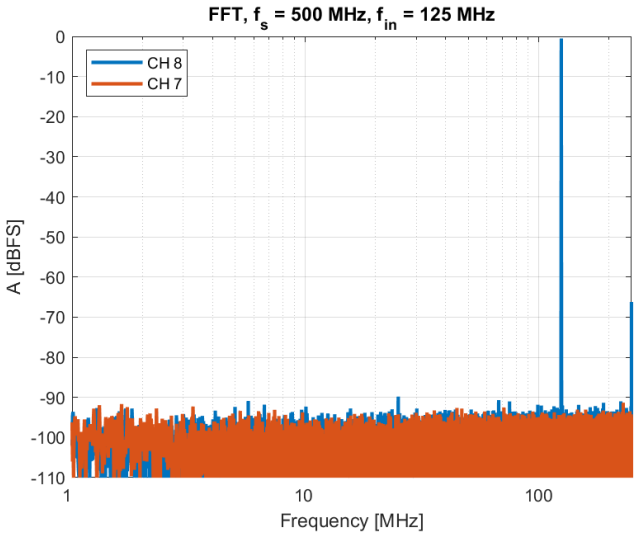
- 8x analog inputs routed directly to Zone 3 ADC-IN0 .. 7
- additional AC path with step attenuator and DC path with op amp
- 4x analog outputs open but can be connected via cables
- all clock in- and outputs can be connected via cables
- includes Zone 2, Zone 1 clocks and analog signals

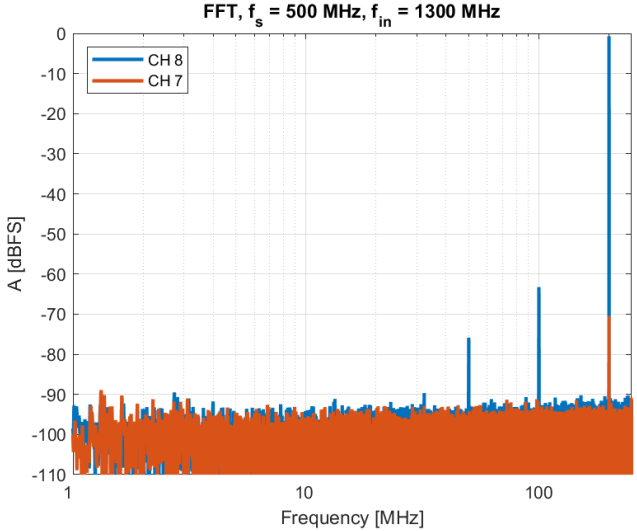
- pilot tone feed in and distribution
- all MGTs routed to FMC connector (JESD204B)
- digital LVDS signals are routed to a CPLD which is connected to the FMC connector (IO extender)
- full MTCA4.1 support for RF back plane and eRTM clock feed

Zone3 RF1.0 AMC – RTM Combination









- measured directly on the RTM ports
- ADCs and front-ends are running

- signal input at channel 8
- channel 7 is terminated with 50 Ohm

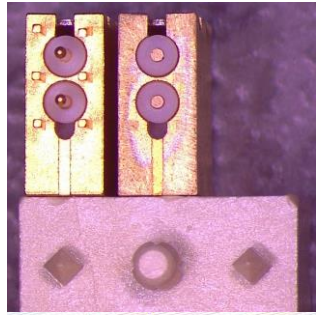
Conclusion and Outlook

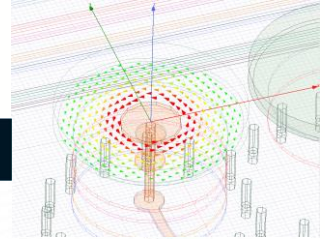
Conclusion

- Coaxi Pack 2 connector is a good choice for the new Zone 3 class
- SMD footprint has very good performance (X-talk)

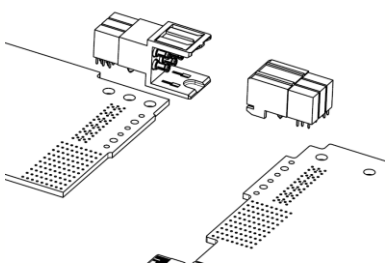
Outlook

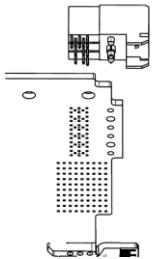
- finish Zone 3 Class RF1.0 recommendation and upload a new version (next days)
- test RF with running JESD204B interface
- test AC and DC path on the RTM

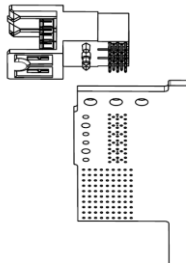


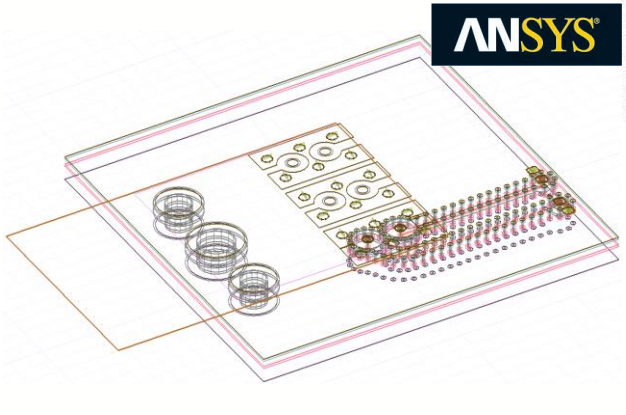


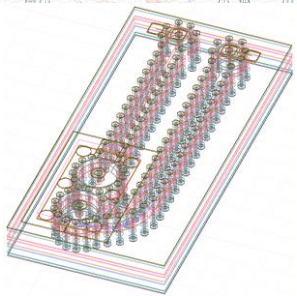
visit: ZONE 3 RECOMMENDATION Class RF1
to get the preliminary draft version of Zone3 Class RF1.0





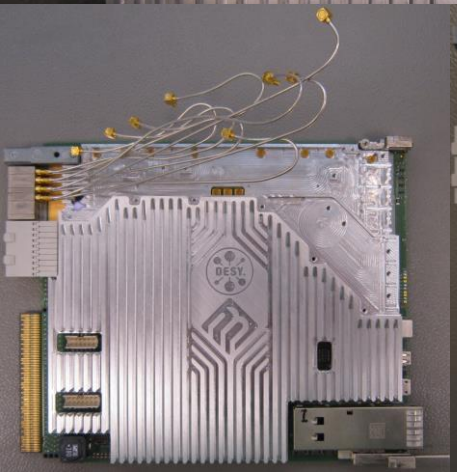


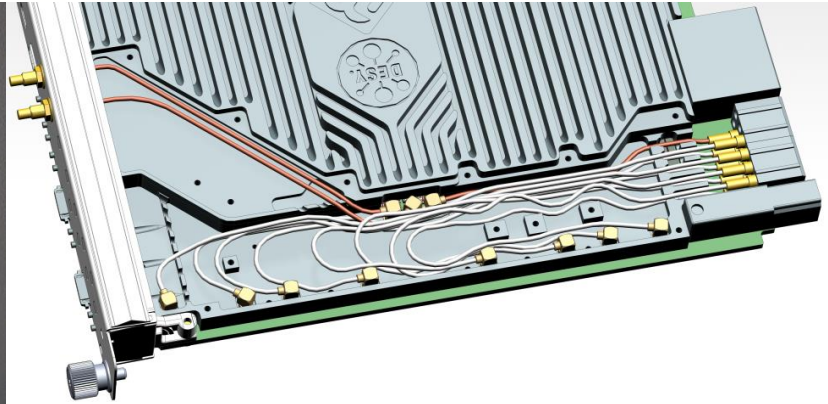




ACKNOWLEDGEMENTS

thanks to: P. Szatkowski, (DESY, ZE) for heatsink production,
M. Fenner, S. Jablonski, F. Ludwig, U.Mavric

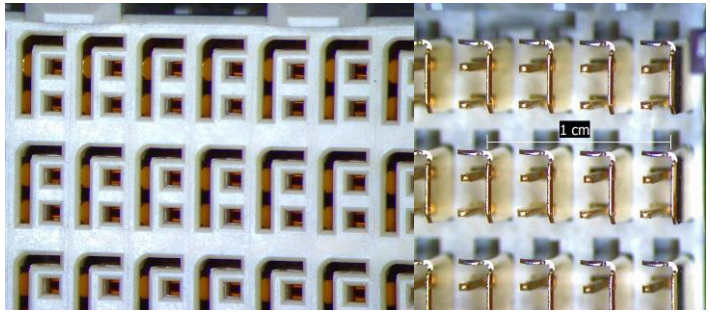




Thank you for your attention.

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

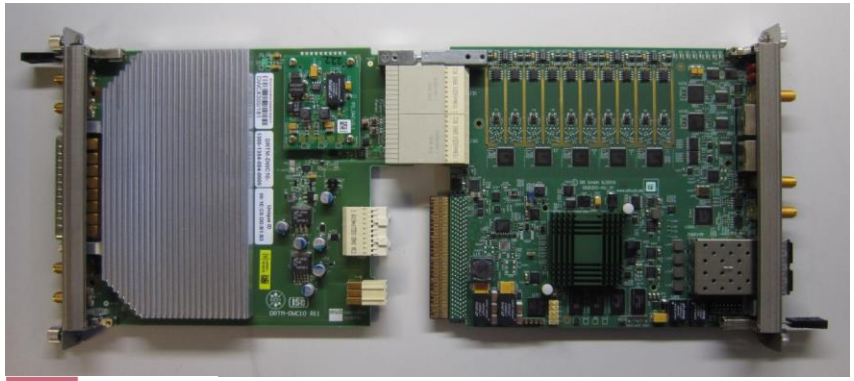
Zone3 RF1.0 AMC – RTM Combination



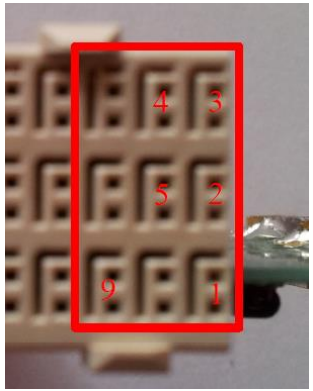
- differential pair connections between AMC and RTM board
- digital and analog Zone3 classes
- J30 contains power, management, clock and digital data signals
- J31 contains analog differential inputs and outputs (AMC view)

DISADVANTAGE:

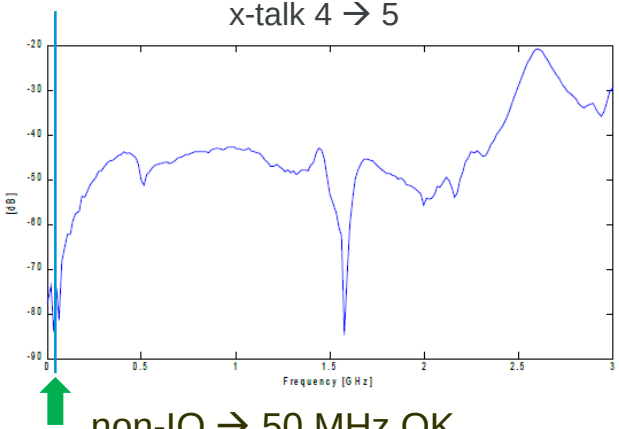
- cross talk between differential pairs



struck innovative systeme



x-talk 4 → 5

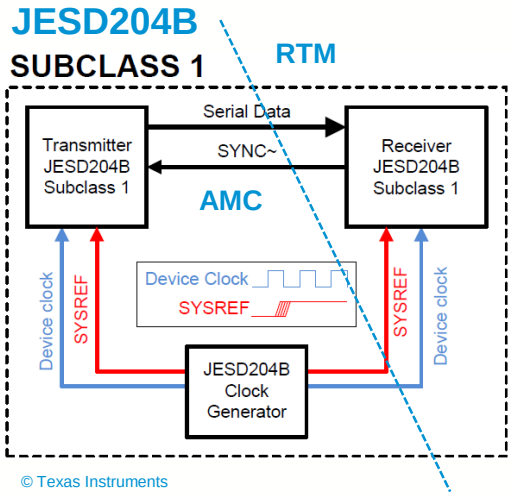


non-IQ → 50 MHz OK

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

New Zone3 Class RF1.0 - Preliminary

- new analog Zone3 class RF1.0
- RF1.0 ADCs on AMC side → DACs on RTM side (JESD204)
- different Zone3 RF sub-classes in the future



© Texas Instruments

LVDS interface

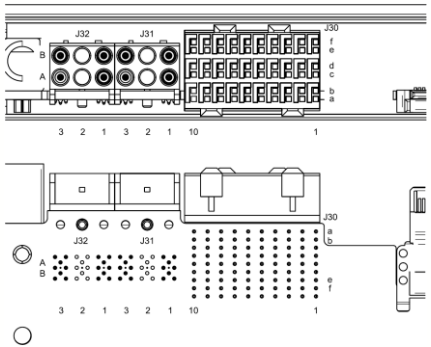
JESD204B interface (DAC)

		Digital Clock IO	Digital fixed IO	Digital Clock Input	Digital user IO		Standard Gbit-Links			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D7-	RF-CLK3-	D5-	D2-	GBT7-TX-	GBT4-TX-	GBT1-TX-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D7+	RF-CLK3+	D5+	D2+	GBT7-TX+	GBT4-TX+	GBT1-TX+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D6-	RF-CLK1-	D4-	D1-	GBT6-TX-	GBT3-TX-	GBT0-TX-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D6+	RF-CLK1+	D4+	D1+	GBT6-TX+	GBT3-TX+	GBT0-TX+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	D3-	D0-CC-	GBT5-TX-	GBT2-TX-	GBT0-RX-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	D3+	D0-CC+	GBT5-TX+	GBT2-TX+	GBT0-RX+	PWRA2	PWRA1

Single Ended Analog Signals

J31		3	2	1
	B	ADC-IN7	DAC-OUT1	DAC-OUT3
	A	ADC-IN6	DAC-OUT0	DAC-OUT2
J32		3	2	1
	B	ADC-IN1	ADC-IN3	ADC-IN5
	A	ADC-IN0	ADC-IN2	ADC-IN4

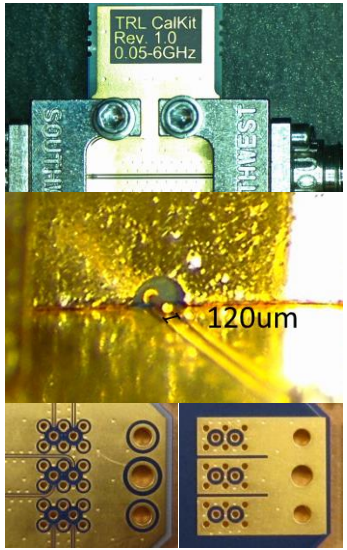
Table 1: Zone 3 - Class RF1.0 pin assignment J30, J31 and J32 connector, AMC side view

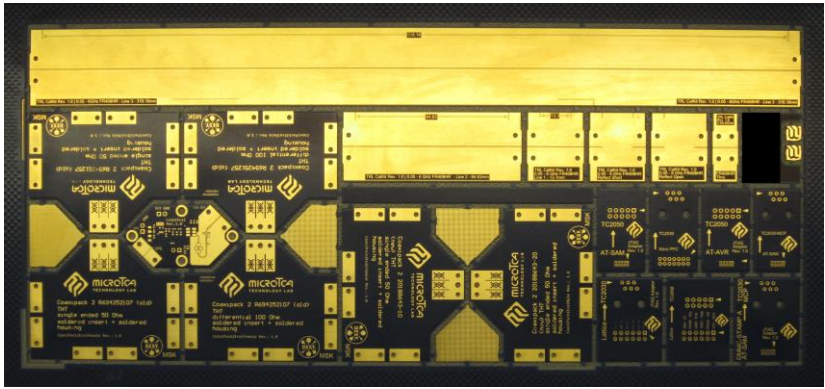


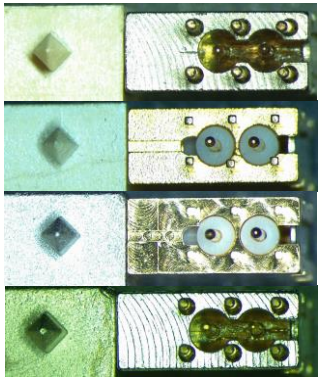
- AMC-CLK used as **device clock** for JESD204B subclass 1
- AMC-TCLK used as **SYSREF** for JESD204B subclass 1
- **SYNC** signal is not timing critical → user IO or fixed IO pair can be used for SYNC

Coaxi Pack 2 Evaluation Board

- TRL calibration kit for the VNA (R&S ZNB20)
- test boards for single-ended and differential transmission, FR408HR, 16 layers, 1.8mm
- **GOAL**: provide a simple and cheap THT footprint with good performance
- **CONS**: compromise between simplicity and performance
- measured connector combinations:





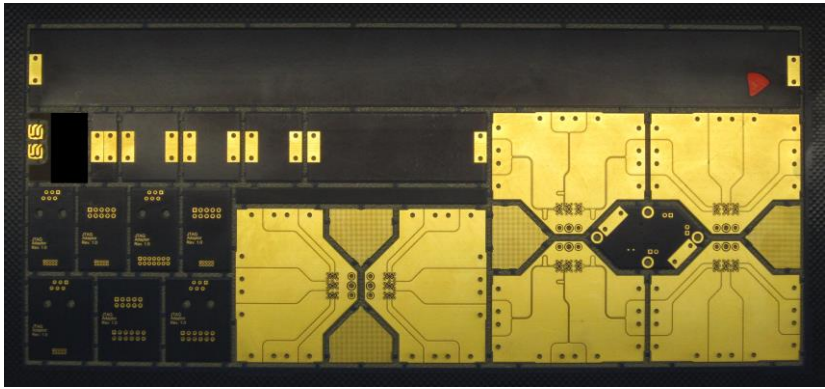


std. housing, std. insert

std. housing, upgrd. insert

shld. housing, upgrd. insert, pin-in-paste

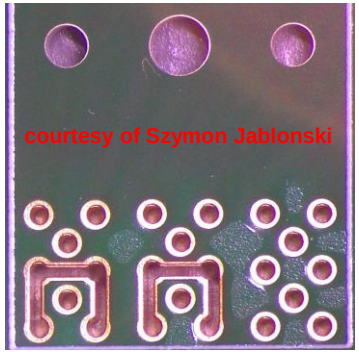
shld. housing, std. insert, pin-in-paste, differential

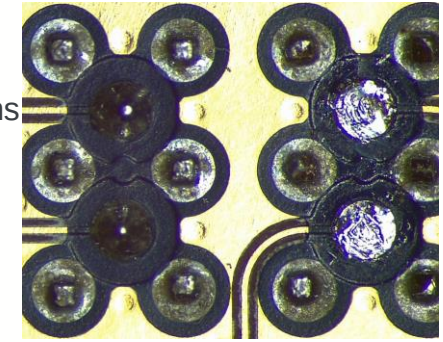


Coaxi Pack 2 Measurement Results

Intra Insert Crosstalk

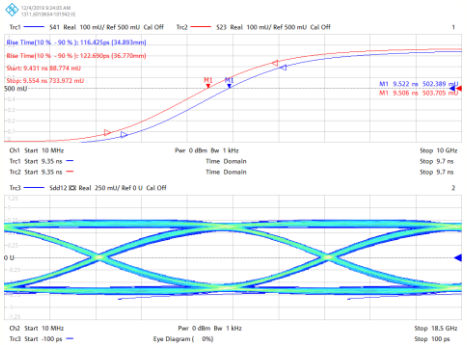
- near-end (NEXT)
- special footprint modifications

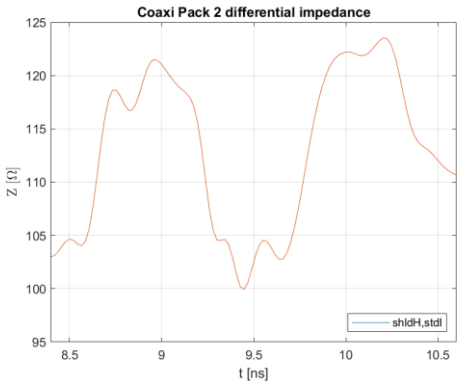




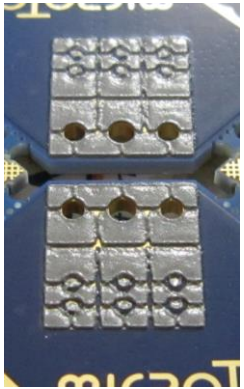
- pins cut to PCB surface

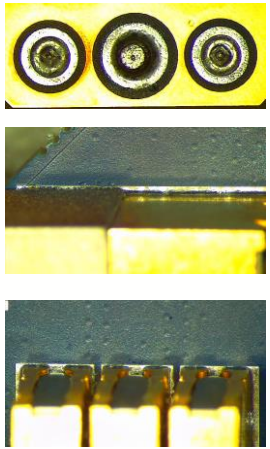
Differential Measurement





Pin-in-Paste





- intra pair skew: 16 ps
- EYE: 10 Gbit/s @ ±1V