Tomasz Włostowski
CERN BE-CEM | SY-RF

Use of MTCA.4 and White Rabbit in the CERN SPS Low Level RF system

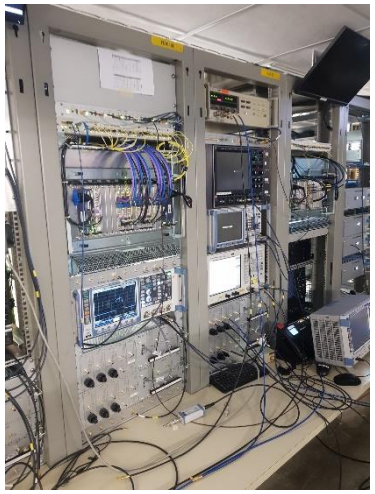
Zoom, 8 December 2021

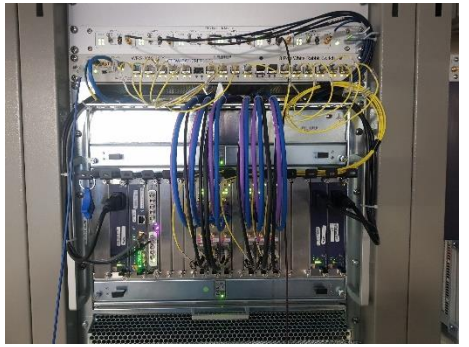
Background

- In 2015 decision was taken to renovate the Low Level Radio Frequency controls in the Super Proton Synchrotron[1] at CERN
- The new system relies on distribution of the reference clock and RF signals over White Rabbit. In order to be able deliver beams of requested quality, the RF required:
- **< 13 ps end-to-end precision (1 deg phase @ 200 MHz, reproducible every power cycle)**
- **-130 dBc/Hz PN at 1 kHz (223 MHz)**

The "old" analog LLRF system

WR-based LLRF

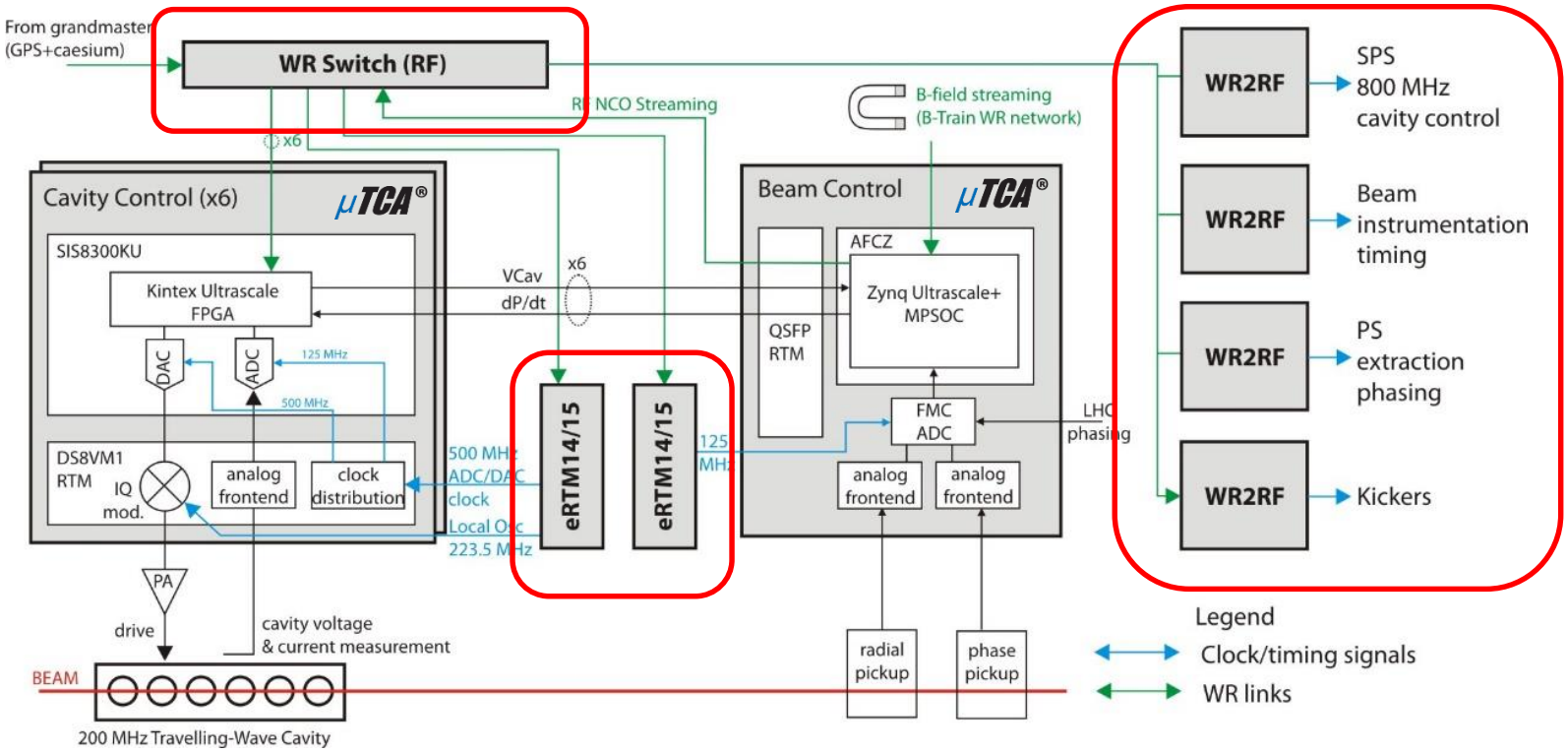




We had to deliver WR gear that can do that: **WRS-LJD, LPDC, eRTM, WR2RF**

[1] The second-largest accelerator at CERN (8 km circumference) and a direct injector to the LHC.

The LLRF System Overview



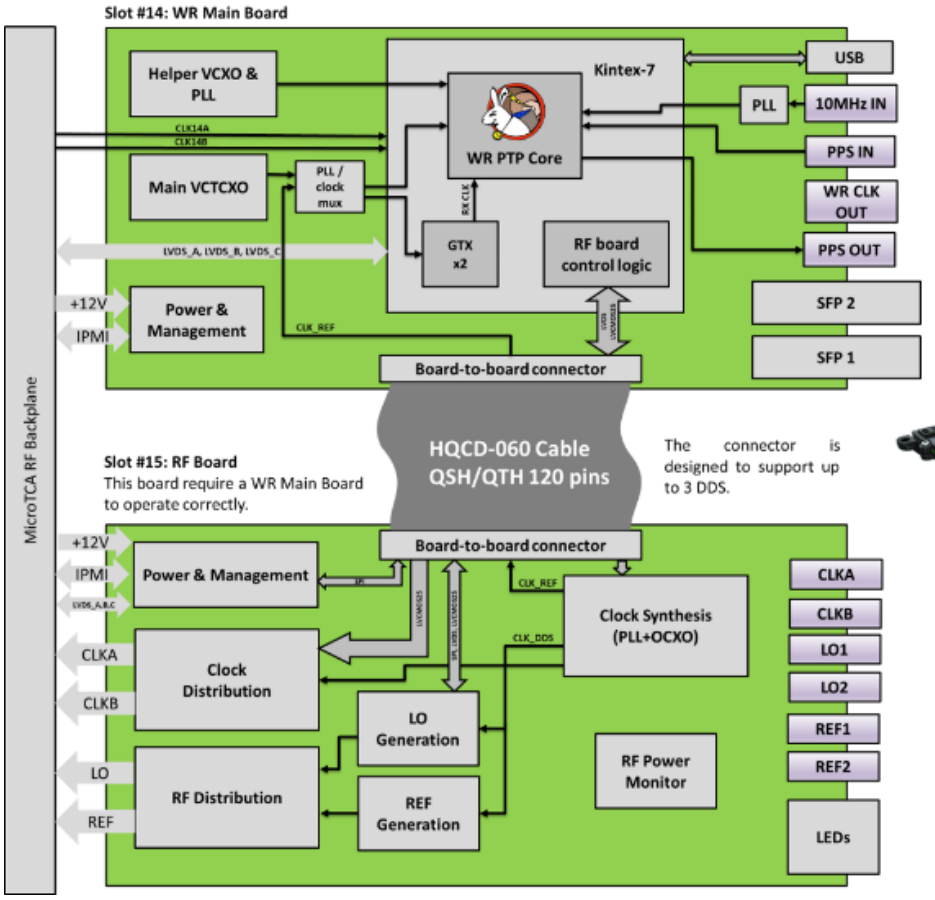
- **Cavity Controller** handles a single RF cavity (we have 6 in the SPS)
- **Beam Controller** calculates the RF frequency (called "RF-Train") and distributes it using WR Streamers
- The **CC** and **BC** reside in two **MTCA.4** crates, with the **LLRF backplane**

- The **eRTM** provides the Local Oscillator and ADC/DAC clocks for the CC/BC
- The **WR2RF** receives the RF-Train and can generate the actual cavity RF signals and RF-synchronous trigger pulses.
- **WRS-LJD** and **LPDC** allow for improved precision and PN

The eRTM14/15

MTCA.4 eRTM, slots 14-15 of RFBP:

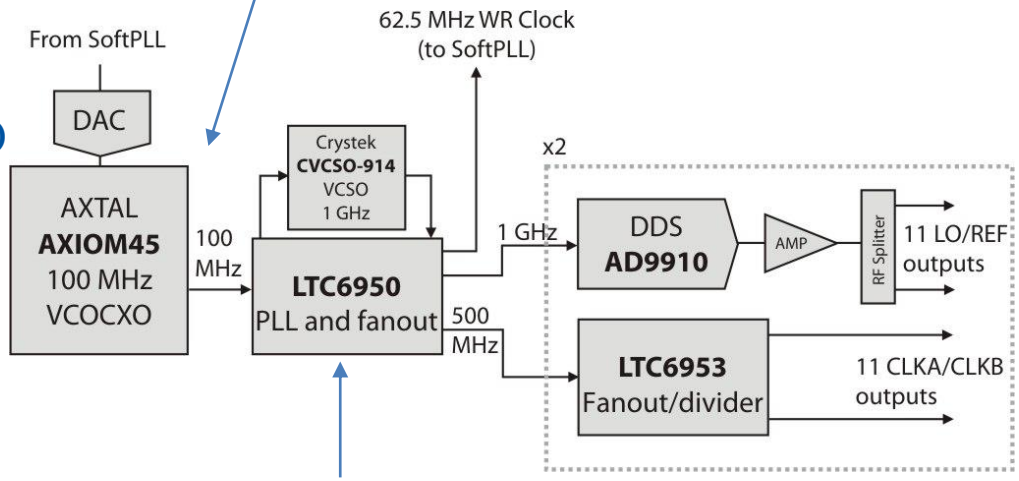
- "Sandwich" of two boards: digital with the FPGA and analog with the oscillators and clock distribution
- Kintex-7 7K70T FPGA
- Controlled by a heavily customized WR PTP Core
- Two DDS analog clocks LO and REF:
  - From 10 to 300 MHz, sine wave
  - Passive clock distribution with adjustable power (0-14 dBm)
  - 11 outputs for each (backplane + FP), on/off control + power monitoring
  - Network-wide phase alignment (WR trigger)
- Two digital clocks CLKA and CLKB:
  - 62.5, 125, 250 or 500 MHz
  - 10 outputs for each (backplane + FP), on/off control
- PPS and 10 MHz in/out
- Two WR uplink ports foreseen for network redundancy
- Software control over USB (we tried IPMI and failed...)
- Stand-alone (no MTCA crate) operation possible



The eRTM14/15 Clock Recovery and Distribution

- LO output must have PN better than -130 dBc/Hz at 1 kHz offset @ 223 MHz
- This is above WR PLL bandwidth and PN figure offered by FPGA PHYs
- Must provide enough PN headroom for the DDS
- **Solution:** AXIOM45ULN 100 MHz OCXO
- DDS and digital clocks require ~100 fs rms jitter and a master clock of 1 GHz
- **Solution:** multiply using PLL + discrete oscillator combo (CVCSO-914-1000)
- 2nd PLL bandwidth = ~10 kHz
- PN at offsets below 10 Hz not critical (not "seen" by the beam)
- LO/REF outputs used for driving RF mixers (low-distortion sinewave), using an analog network of RF amplifiers and passive splitters

-100	dBc/Hz	@ 10 Hz
-135	dBc/Hz	@ 100 Hz
-162	dBc/Hz	@ 1 kHz
-172	dBc/Hz	@ 10 kHz
-175	dBc/Hz	@ 100 kHz

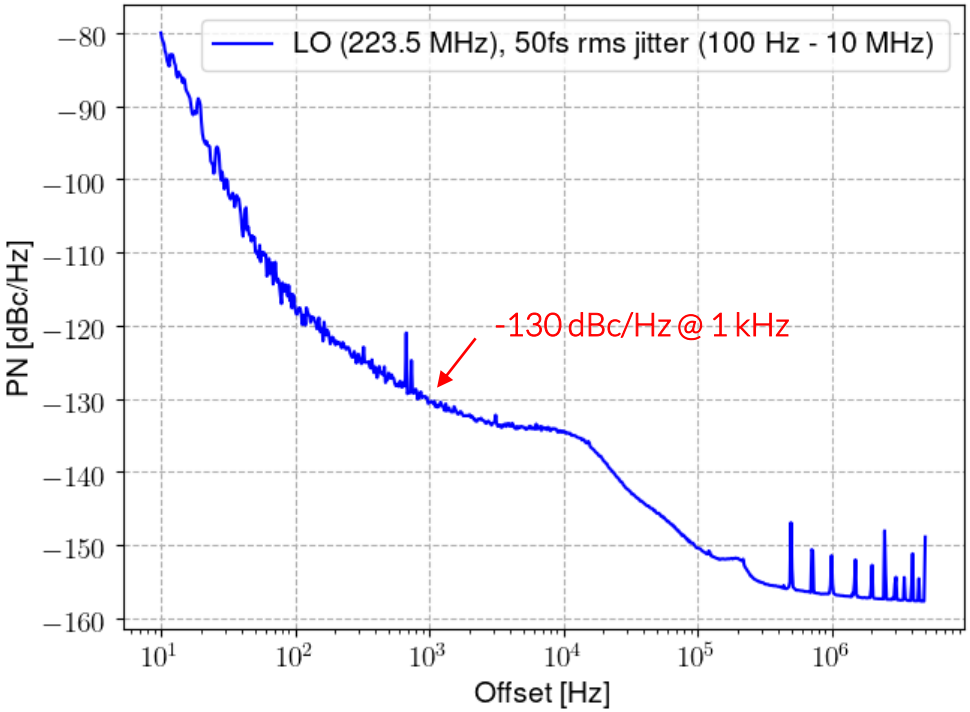


Phase Noise Typical: (free running)

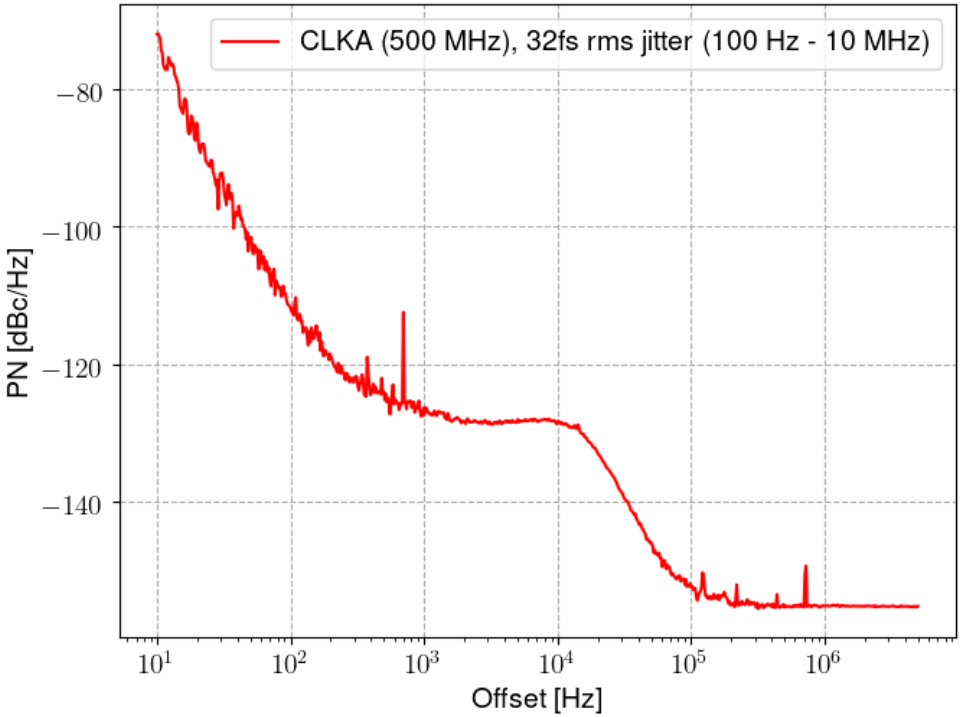
1kHz	**-110 dBc/Hz**
10kHz	**-139 dBc/Hz**
100kHz	**-160 dBc/Hz**
1MHz	**-170 dBc/Hz**
10MHz	**-174 dBc/Hz**

The eRTM14/15 PN measurements

LO (front panel) @ 223.5 MHz



CLKA (front panel) @ 500MHz



- DDS LO/REF PN of **-130.5 dBc/Hz** at 1 KHz (223.5 MHz), jitter **51 fs** (100 Hz – 10 MHz)
- CLKA PN of **-126 dBc/Hz** at 1 KHz (500 MHz), jitter **32 fs** (100 Hz – 10 MHz)
- Measured for front panel outputs of the eRTM14/15
- At these PN levels, even mechanical vibrations caused by cooling fans matter!

The eRTM14/15 Varia

Management capabilities:

- IPMI/MMC implemented on STM32F3 MCUs using LNLS's OpenMMC (our experience is very positive)
- Monitoring of onboard voltages, 10+ temperature sensors and OCXO health
- USB control provides access to all board features (frequencies, amplitudes, WR link control) and provides same monitoring capabilities as IPMI
- Grafana panels for interactive monitoring/alarms

```
ERTM14/15 command line interpreter - type 'help' for a list of commands
ertm> bs
DDS: ------------------------------------------------------------------------
LO ftw: 39374bc6 (223.500MHz)          | REF ftw: 39374bc6 (223.500MHz)
LO level adjust: 0.2578 ( 66/256)      | REF level adjust: 0.2578 ( 66/256)
LO pll_out power: 3.930 dBm            | REF pll_out power: 14.970 dBm
LO sync_state:  rdy                    | REF sync_state:  rdy
LO04:   pow: 11.490 dBm  st:monitor    | REF04: pow: 11.670 dBm  st:monitor
LO05:   pow: 11.850 dBm  st:monitor    | REF05: pow: 11.560 dBm  st:monitor
LO06:   pow: 11.890 dBm  st:monitor    | REF06: pow: 12.050 dBm  st:monitor
LO07:   pow: 11.780 dBm  st:monitor    | REF07: pow: 12.100 dBm  st:monitor
LO08:   pow: 11.670 dBm  st:monitor    | REF08: pow: 12.090 dBm  st:monitor
LO09:   pow: 11.850 dBm  st:monitor    | REF09: pow: 11.950 dBm  st:monitor
LO10:   pow: 11.860 dBm  st:monitor    | REF10: pow: 11.860 dBm  st:monitor
LO11:   pow: 11.720 dBm  st:monitor    | REF11: pow: 11.980 dBm  st:monitor
LO12:   pow: 11.700 dBm  st:monitor    | REF12: pow: 11.870 dBm  st:monitor
CLKAB: ---------------------------------------------------------------------
CLKA04: on   rdy  500.0 MHz     | CLKB04: on   rdy  125.0 MHz
CLKA05: on   rdy  500.0 MHz     | CLKB05: on   rdy  125.0 MHz
CLKA06: on   rdy  500.0 MHz     | CLKB06: on   rdy  125.0 MHz
CLKA07: on   rdy  500.0 MHz     | CLKB07: on   rdy  125.0 MHz
CLKA08: on   rdy  500.0 MHz     | CLKB08: on   rdy  125.0 MHz
CLKA09: on   rdy  500.0 MHz     | CLKB09: on   rdy  500.0 MHz
CLKA10: on   rdy  500.0 MHz     | CLKB10: on   rdy  125.0 MHz
CLKA11: on   rdy  500.0 MHz     | CLKB11: on   rdy  125.0 MHz
CLKA12: on   rdy  500.0 MHz     | CLKB12: on   rdy  125.0 MHz
CLKA13: on   rdy  500.0 MHz     | CLKB13: on   rdy  125.0 MHz
CLKA14: on   rdy  500.0 MHz     | CLKB14: on   rdy  125.0 MHz
CLKA15: on   rdy  500.0 MHz     | CLKB15: on   rdy  125.0 MHz
-------------------------------------------------------------------------
ertm>
```

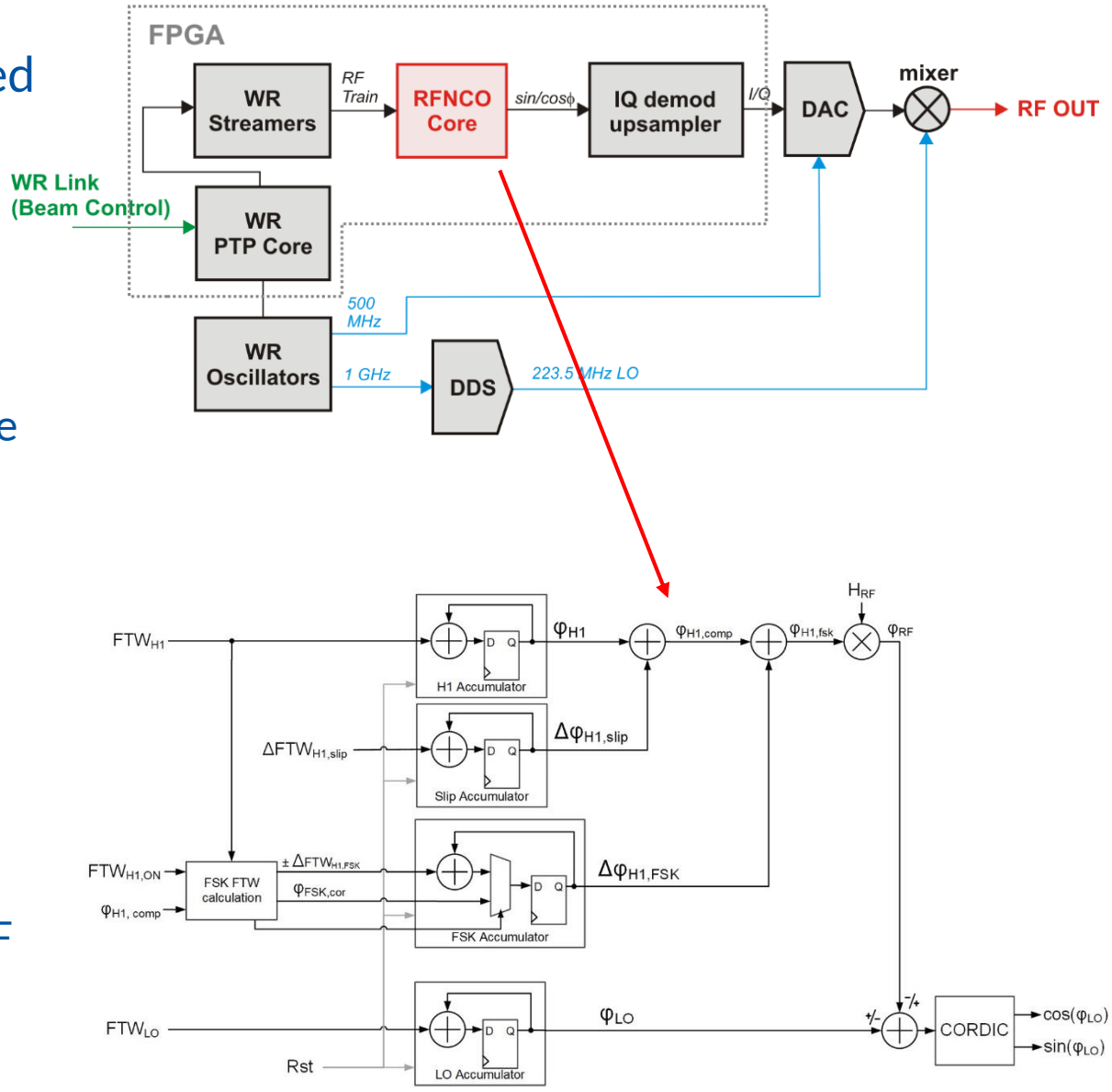
Future plans:

- CERN PS 200 MHz deployment
- Extend frequency range (applications: SPS 800 MHz system, LHC Crab Cavities, LHC LLRF 400 MHz). Upgrade DDS and clock distribution electronics
- Streamline calibration of the board (currently hand-done)

WR RF Distribution

Based on the RFNCO core provided by the LLRF team

- A bit more complex than the „DDS over WR" idea presented in the past...
- Inputs momentary RF parameters (machine-specific) broadcast by the Beam Controller using the WR Streamers
- The NCO core computes the momentary RF phase and outputs *sin/cos* for the DAC
- External DAC and mixer produce the ultimate RF output
- Performance very similar to eRTM (-132 dBc/Hz @ 1kHz/200 MHz RF out)

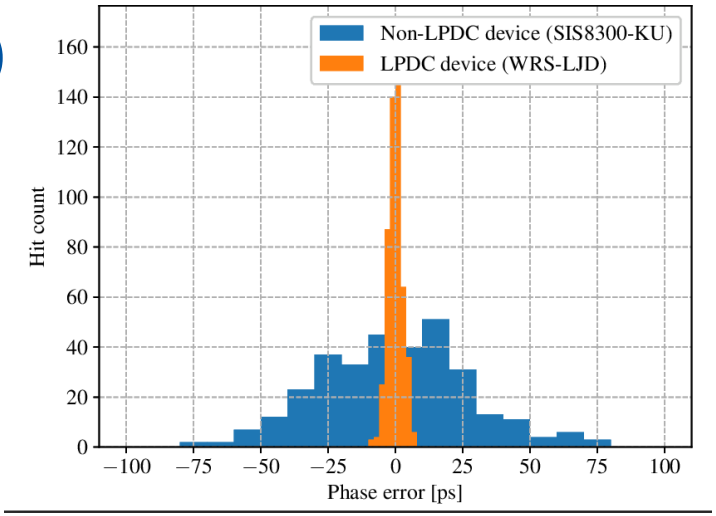


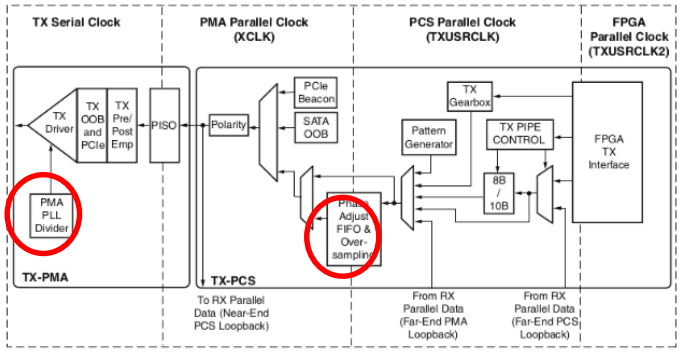
Drawings courtesy J. Gill, A. Spierer and G. Hagmann

Improving WR Precision

Goal: The RF system needs the phase reproducibility (power-cycle) better than 13 ps (1 degree at 200 MHz)

- "Standard" WR offers ~100 ps
- Most of this comes from the FPGA transceiver
- Two main sources of uncertainty:
  - Xilinx's TX/RX Phase Align logic
  - PMA bit clock -> PCS word clock dividers, where each 'tap' introduces slightly different phase offset
- Solution: **LPDC** (**L**ow **P**hase **D**rift **C**apable) ports:
  - Disable Phase Alignment
  - *Tom's Casino*[1] approach – keep resetting the TX/RX path measuring the phase of the clocks until it hits a predefined value (bypasses divider uncertainty)
- Currently available for GTXE1 (Virtex-6) and GTXE2 (Kintex 7 and Zynq-7000)
- Supported devices: WRS v6.0, eRTM, WR2RF-VME, SPEC7





[1] For more details/bibliography, see ICALEPCS 2021 THBR02 paper. Name by Peter Jansweijer/NIKHEF ☺

Our experience with MTCA.4

The SPS LLRF was also the first application of MTCA.4[1] in the CERN Accelerator Sector – and as such came with some issues:

- **Clock distribution and eRTM control issues**
- **Thermal design of the crate and fan units**
- Rear Power Module firmware issues with powering and communicating with the LLRF RTMs
- No standard data link between the CPU and eRTM slots 14-15
- Bugs in MCH firmware, such as non-functional configuration parameters
- CPU BIOS configuration (PCI Express) is very complex. Wrong settings can 'brick' the CPU module
- Difficult debugging of IPMI/MMC communication

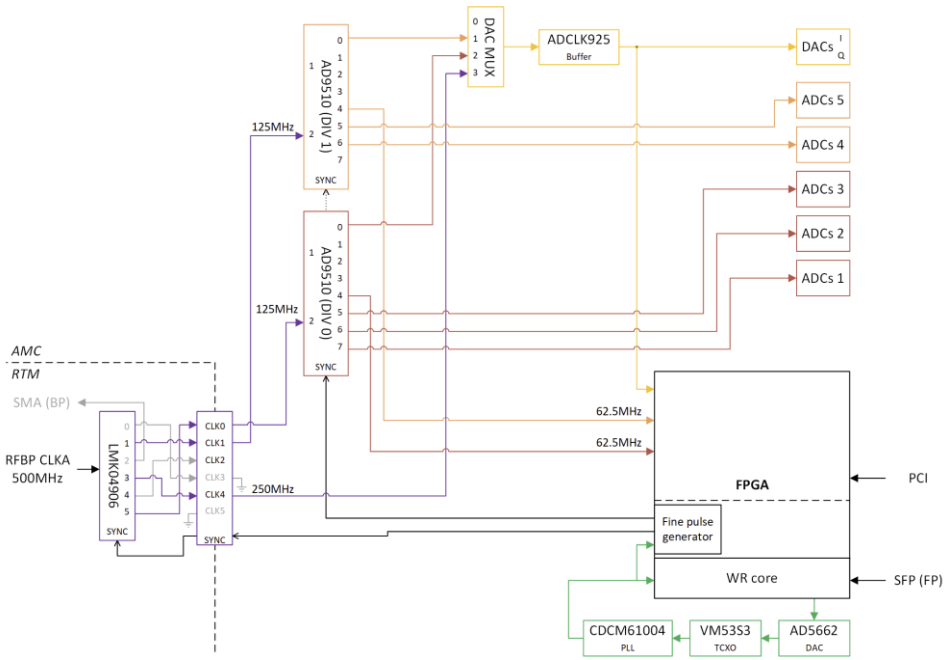
After 4 months of intense collaboration with the vendors – issues fixed

[1] Platform: Schroff/Nvent 11850-026 crate + LLRF backplane + NAT MCH/CPU/PMs

Our experience with MTCA.4

eRTM/DS8VM1 clock divider sync

- DS8VM1 board has only CLKA RFBP input
- Board is clocked by 500 MHz from the RFBP, but needs divided-down clocks (250/125/62.5 MHz) **aligned** to WR
- We had do develop a **Fine Pulse Generator** core on the SIS83K FPGA to generate the **SYNC pulses** for the clock dividers
- **Per-slot calibration** necessary (RFBP CLKAB lines are not length matched)
- Would have been much easier to use CLKB as the slow *sync clock*
- Easy to fix in hardware, but we could not do this ourselves
- Written collaboration agreement (NDA-like) required to obtain even the snippets of schematics from DESY
- Project **delayed** by several months



Our experience with MTCA.4

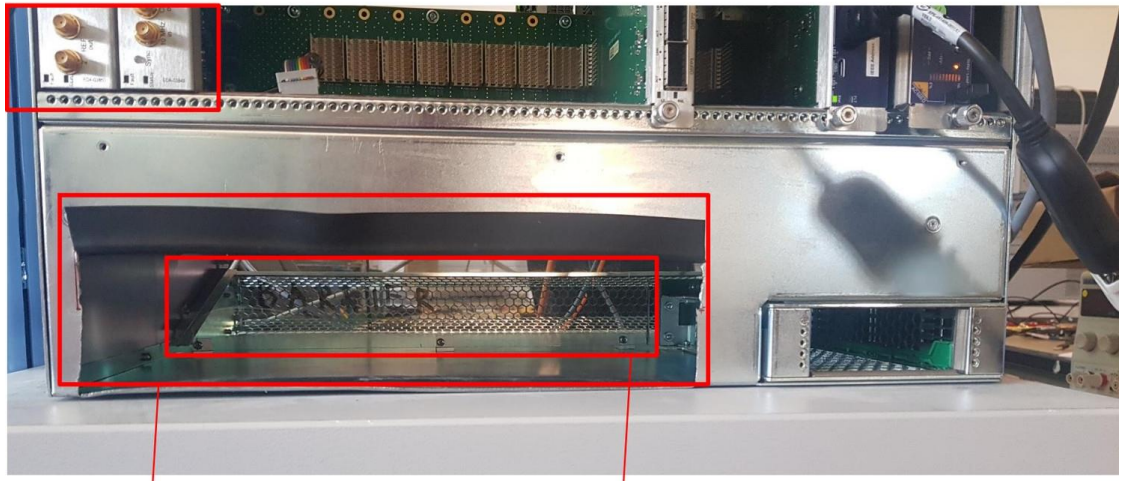
eRTM thermal issues

- eRTM14-15 slot cooling is very poor in the 9U nVent crate
- 84 W (7 A * 12 V) of total fan power, 36 W dissipated for slots 14-15, boards heating up to 100 deg Celsius!
- Suboptimal allocation of fan power (front fans 3x more powerful than the rear). Top fan tray not doing anything.
- Air inlet in front of the crate: front fans „steal” air for the rear part of the crate
- MCH not allowing to control front/back fans independently (bug in firmware)
- Similar overheating observed for the RPMs
- Firmware fixes and putting more powerful fans in the back provided a bit of improvement, but the fans are still at maximum speed and are **extremely loud**

5 $ fix for eRTM/RPM cooling

eRTM14/15 slot

No top fan tray needed (no impact on temperatures)



Cut a hole in the back of the crate

Installed a plexiglass air barrier separating front/back airflows

Conclusions

- Numerous new features for the White Rabbit ecosystem, enabling new areas of applications
- Vastly improved PN and phase reproducibility
- MTCA.4: suitable platform (after some bugfixing), but requires a lot of effort to set up correctly
- Fully digital LLRF system entirely relying on WR for synchronization and RF distribution, including driving the RF cavities in a large operational machine
- All components available for everyone as Open Source Software/Hardware on **ohwr.org**.

Acknowledgements:

- Grzegorz Daniluk, Maciej Lipiński, Javier Serrano, Adam Wujek | Core WR Team
- Mattia Rizzi | The Phase Noise Wizard
- John Gill, Tristan Gingold, David Cobas, Dimitrios Lampridis | eRTM/WR2RF Team
- Julian Palluel, Erik van der Bij, Michel Arruat | MTCA Platform Support Team
- Andrew Butterworth, Julien Egli, Gregoire Hagmann, Arthur Spierer, Maciej Sumiński, Karol Adrianek, Predrag Kuzmanovic, Philippe Baudrenghien, Saul Novel Gonzalez | LLRF Team

Backup slides

The WR2RF

VME64x card for interfacing the WR LLRF with the "analog" world

- Provides compatibility with VME systems
- Replaces expensive coaxial cabling with a single WR fiber
- WR Clock and DDS identical as in the eRTM board
- 2 independent RF outputs
- 250 MSPS 16-bit I/Q DAC followed by an upconverter
- Numerically Controlled Oscillator capable of reproducing the SPS cavities RF signal
- 2 low jitter Trigger Units per each RF output, generating pulse patterns synchronous with the RF (bunch clock, orbit clock or arbitrary pulses)
- A number of standard timing I/Os (PPS, 10 MHz, slow triggers)
- User API in C

Applications: driving systems that require beam-synchronous analog timing (instrumentation, kickers, synchronization with the Proton Synchrotron)