



Latest Hardware Developments in MicroTCA.4

Michael Fenner, Johannes Zink, Jan Marjanović, Nikola Radaković
Hamburg, 9. November 2021

Topics

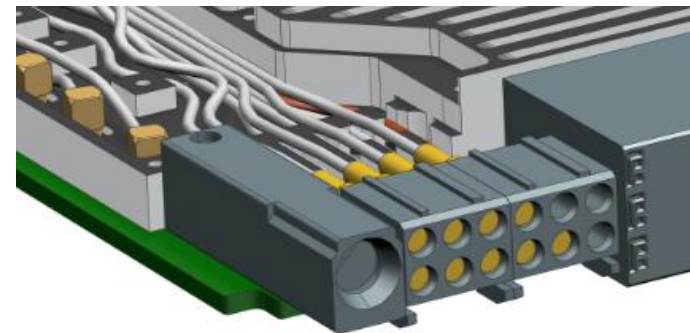
- **DAMC-DS812ZUP**
- **MicroTCA.4 Motion Controller**
- **DAMC-BPMZUP**
- **Support tools available to the community**

DAMC-DS812ZUP

DAMC-DS812ZUP – 8-Channel RF Low-Latency Digitizer



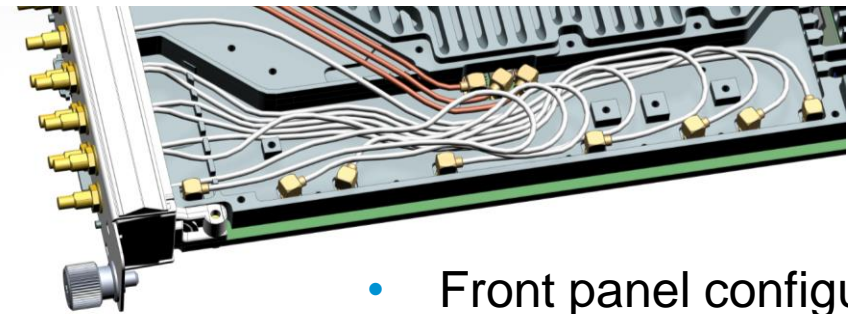
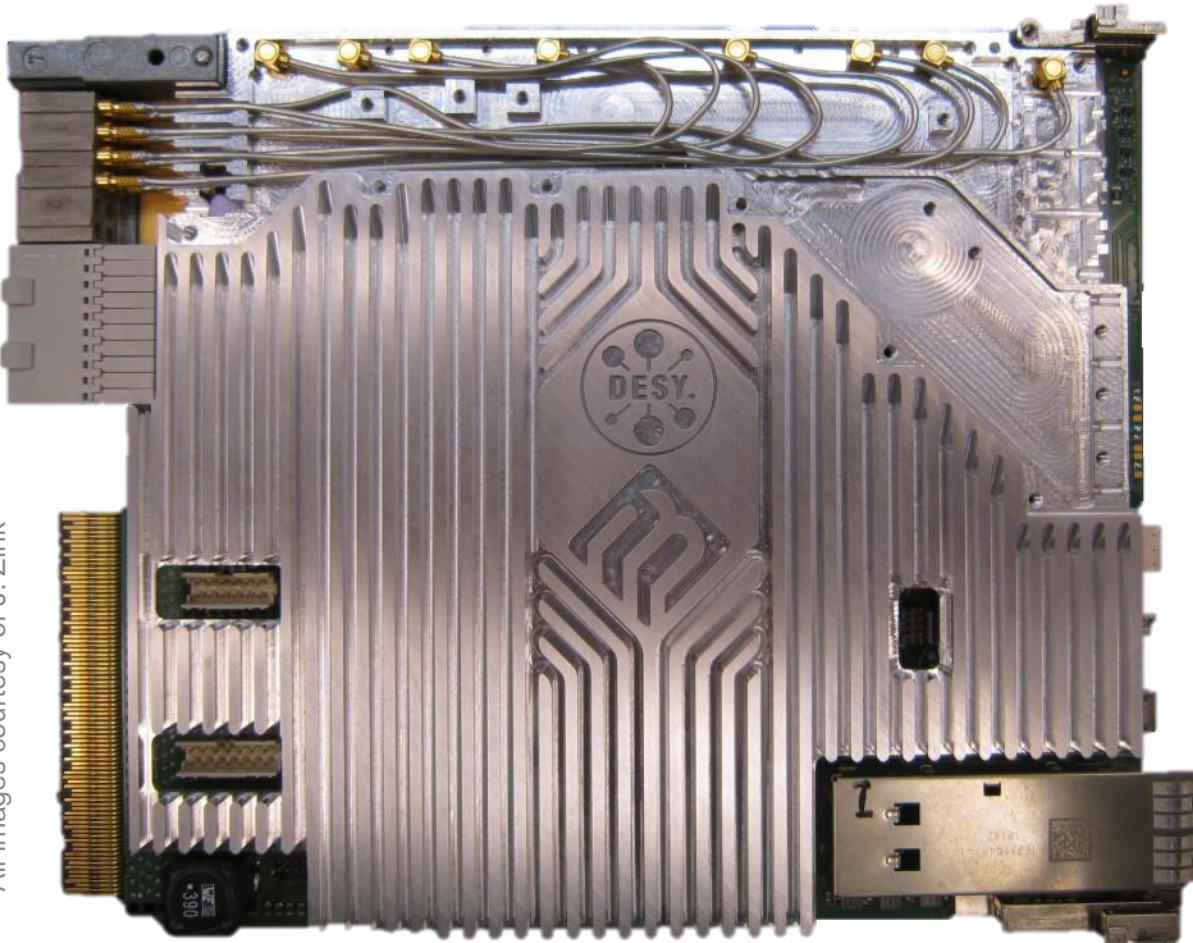
- **First Board that uses analog Zone 3 RF Class**
- 2.7GHz input BW, 12 bits, 8-channels
- Amplifier bandwidth: 4.8 GHz
- 50ns end-to-end latency
- **Uses coaxial semi-rigid cables for transmission**
- RF input from front panel or RTM
- 800 MSPS / 1600 MSPS
- On-board PLL: 14fs jitter
- PCIe Gen. 3 x4 or x8 connectivity
- QSFP+ support (4x10G)
- Stand-Alone Mode (with USB-C alternate mode)
- State-of-the-art high-level language support



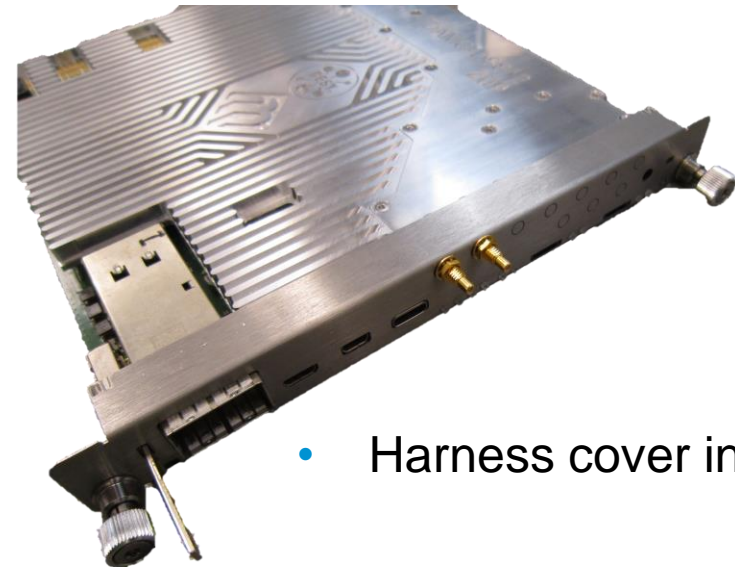
courtesy of J. Zink

DAMC-DS812ZUP – Coaxial Harness

- Coaxial cables offer excellent RF performance
- Usage of harness allows front input / rear input configuration
- Zone3 RF class specification (based on Radiall Coaxipak 2) is available to the community

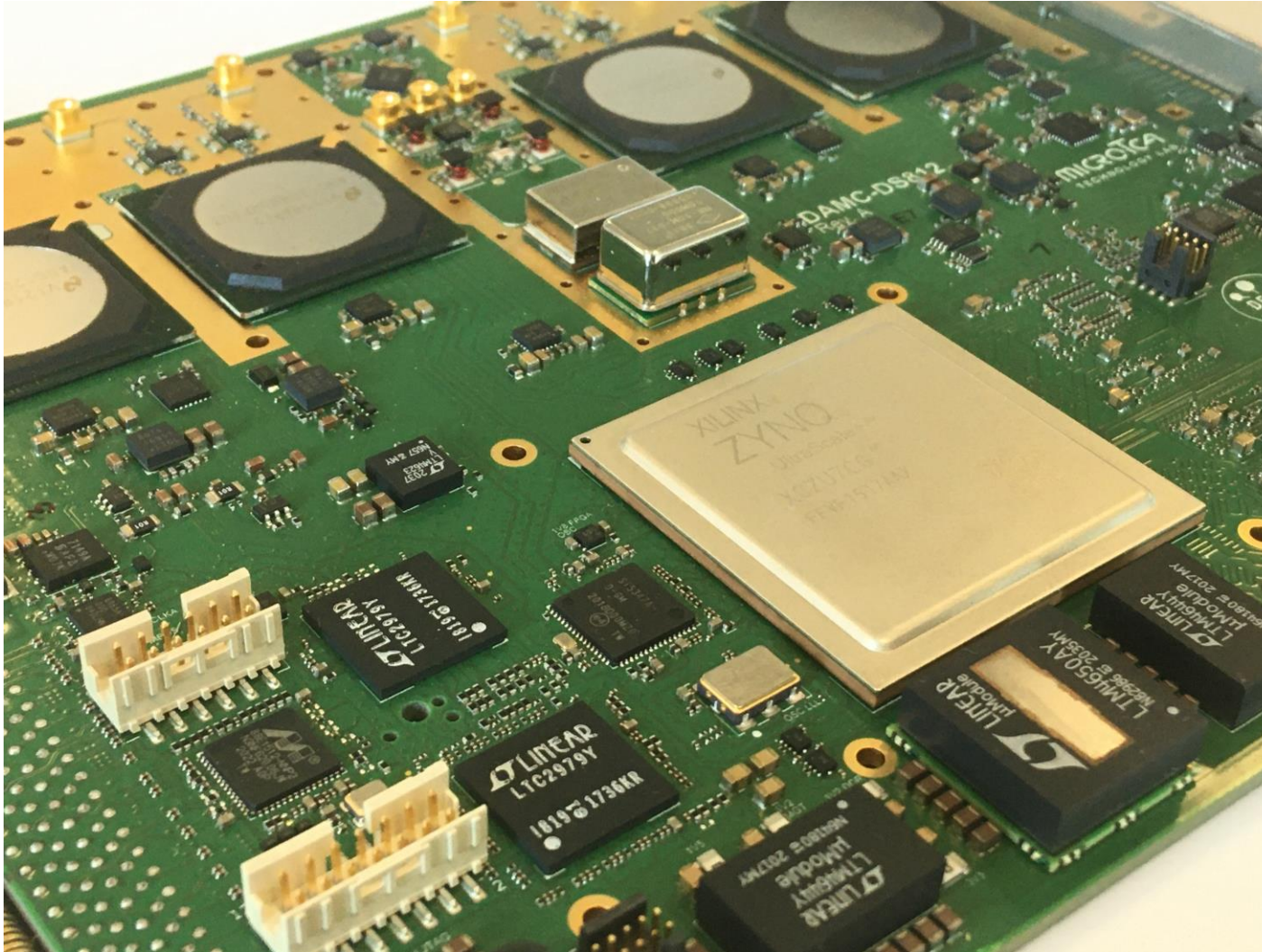


- Front panel configuration

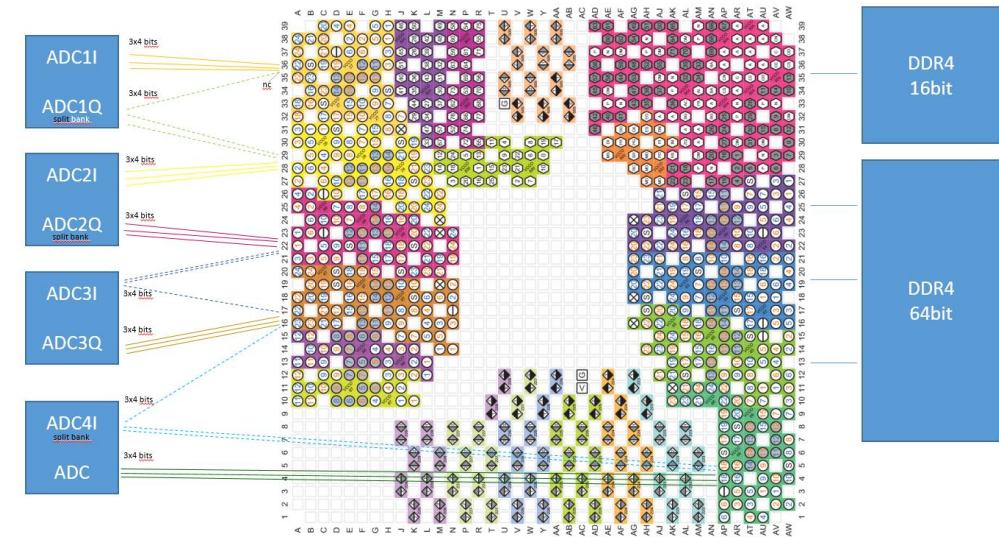


- Harness cover installed

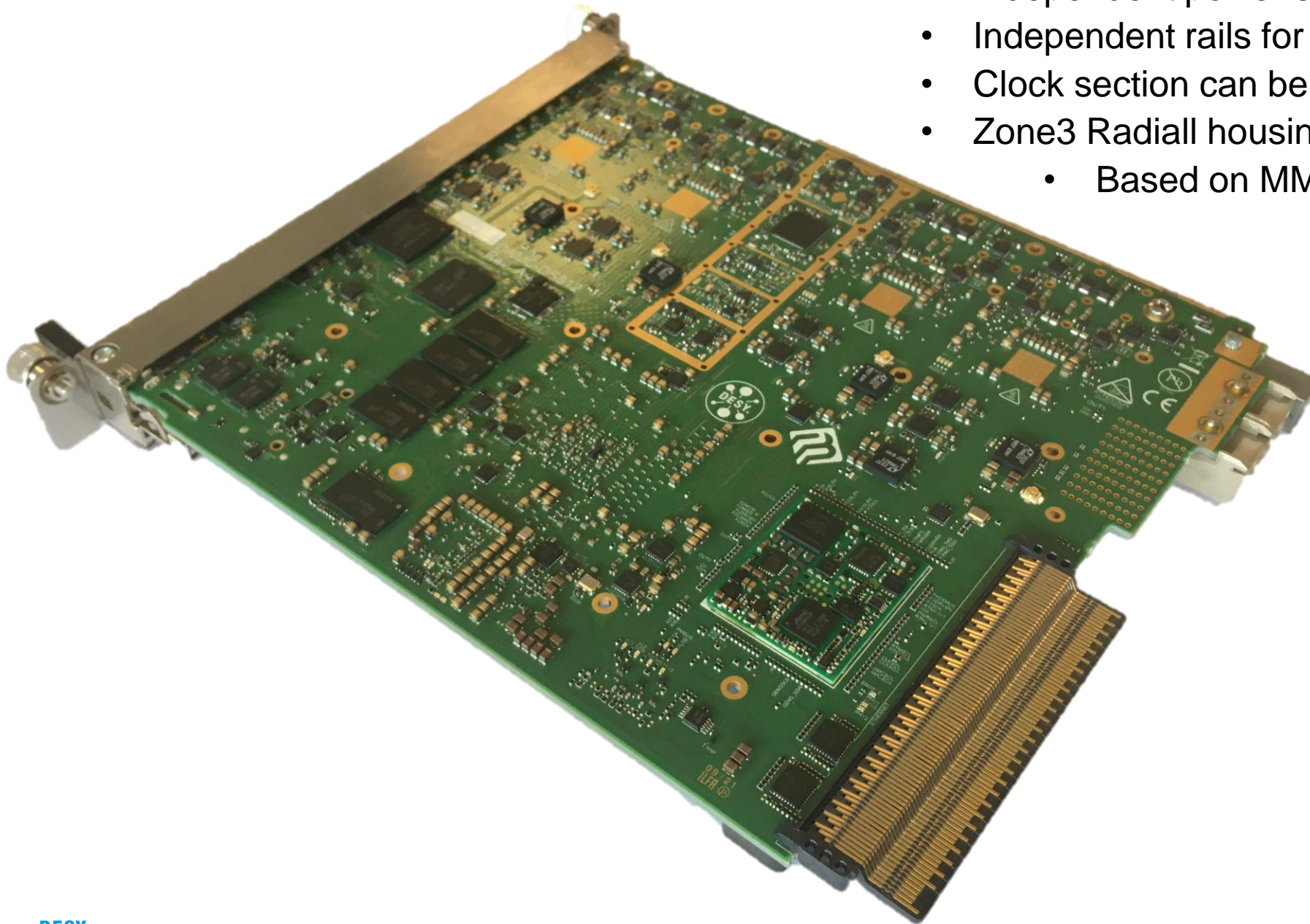
Based on Zynq Ultrascale+ MPSoC



- Most dense board developed in MSK group
- 4289 components down to 0201 size
- 16-Layer HDI stack-up
- Takes full advantage of the Ultrascale+ capabilities (bank assignment trick)

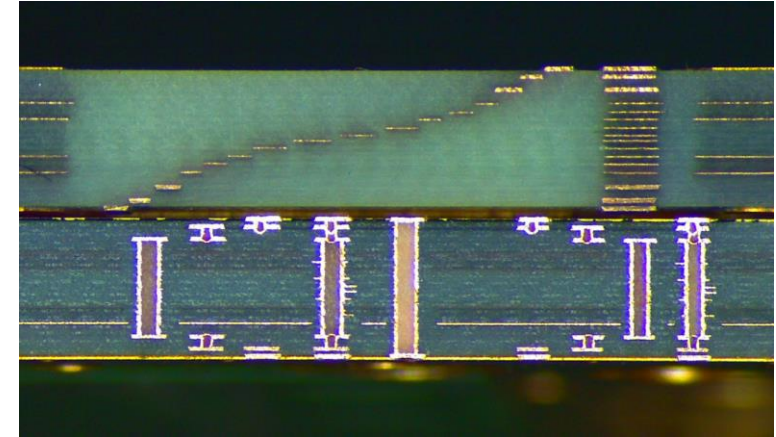
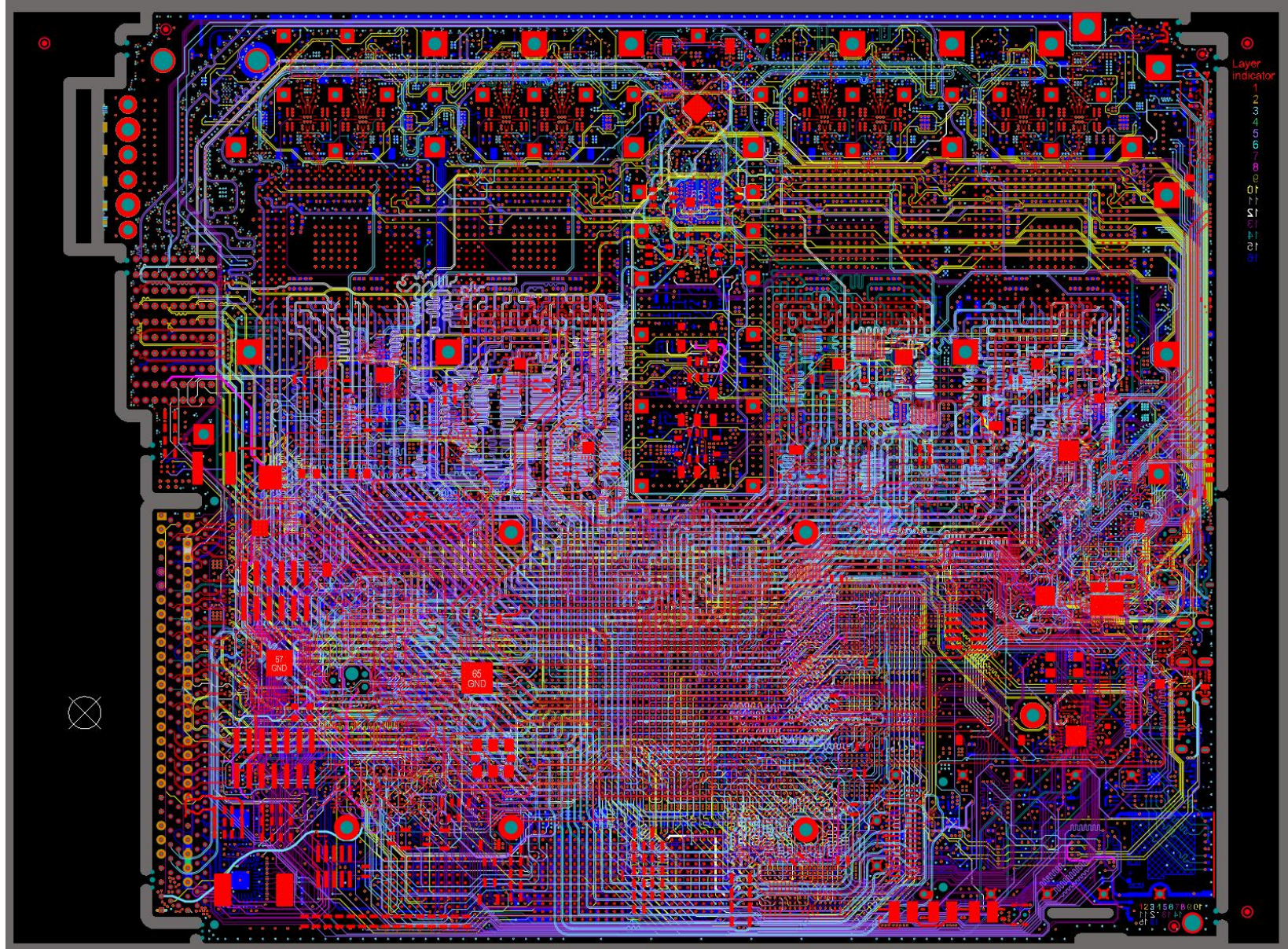


DAMC-DS812ZUP – bottom side

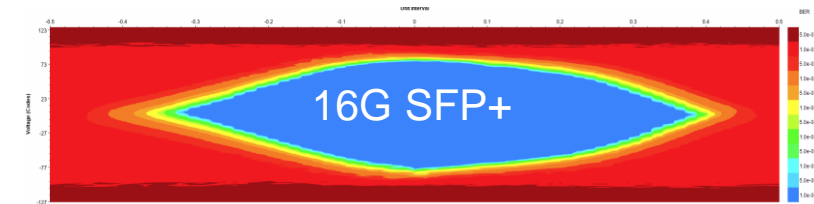


- Independent power supplies for digital/analog part
- Independent rails for each ADC channel
- Clock section can be fully shielded from both sides
- Zone3 Radial housing is metalized and soldered
 - Based on MMC Stamp

DAMC-DS812ZUP Layout details

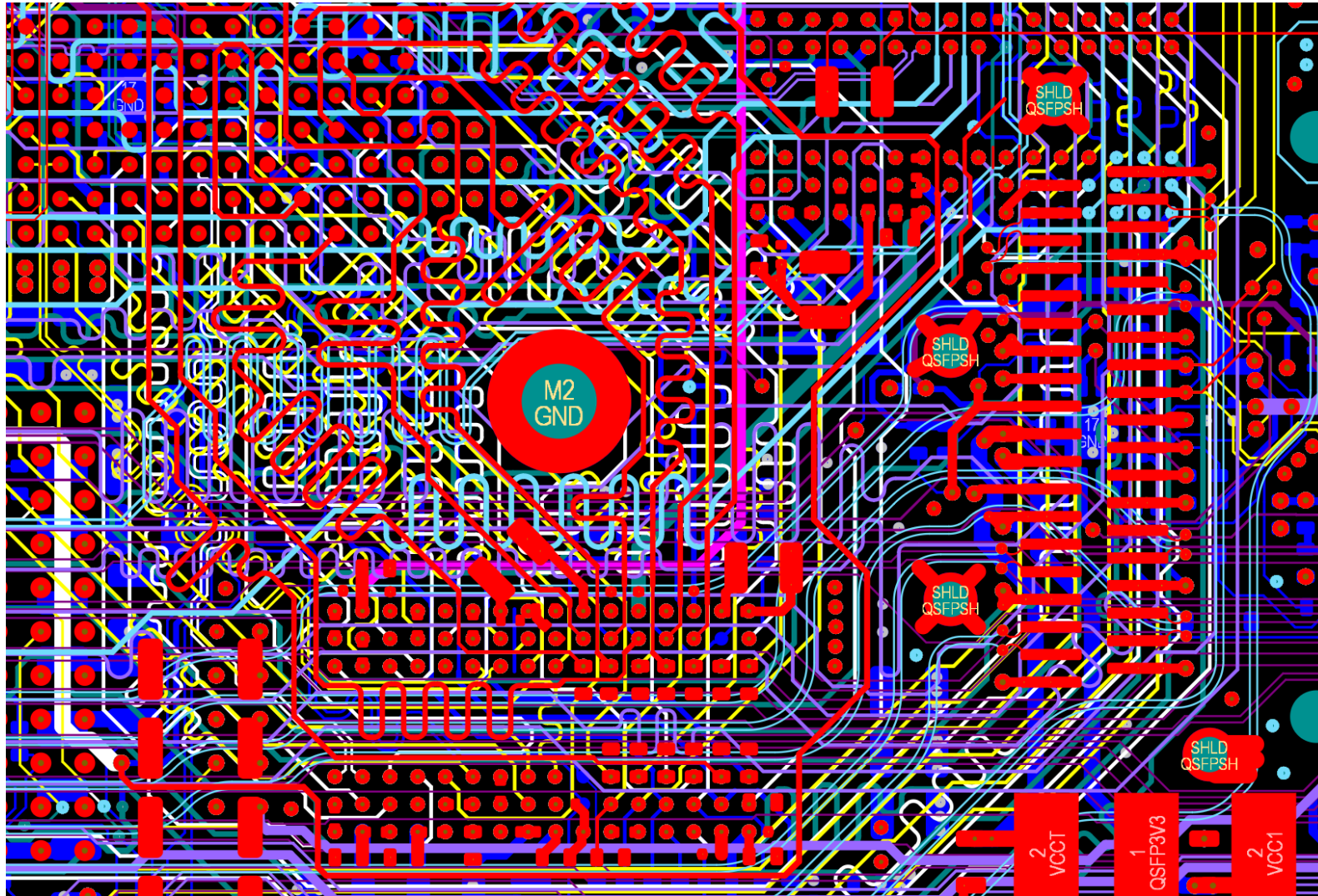


courtesy of J. Zink

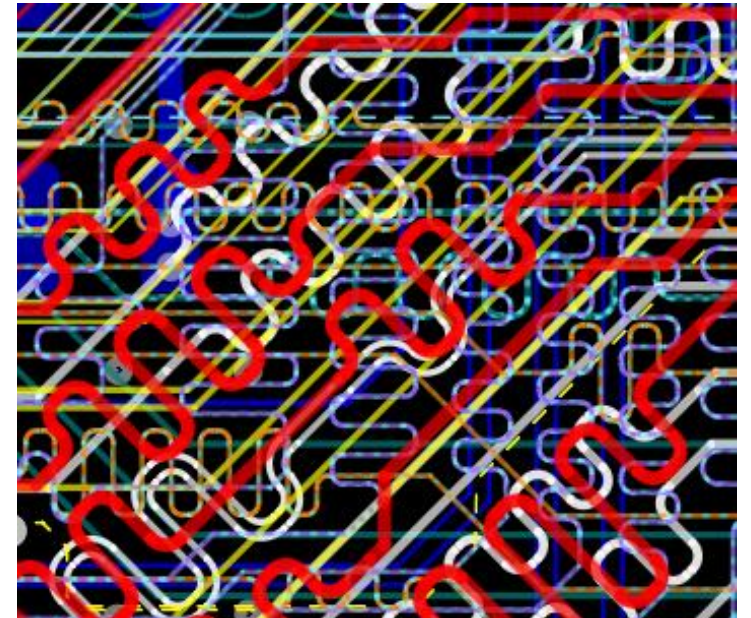


- Stack-up allows high density
- Less dependency between upper/lower sections
- Perfect signal integrity

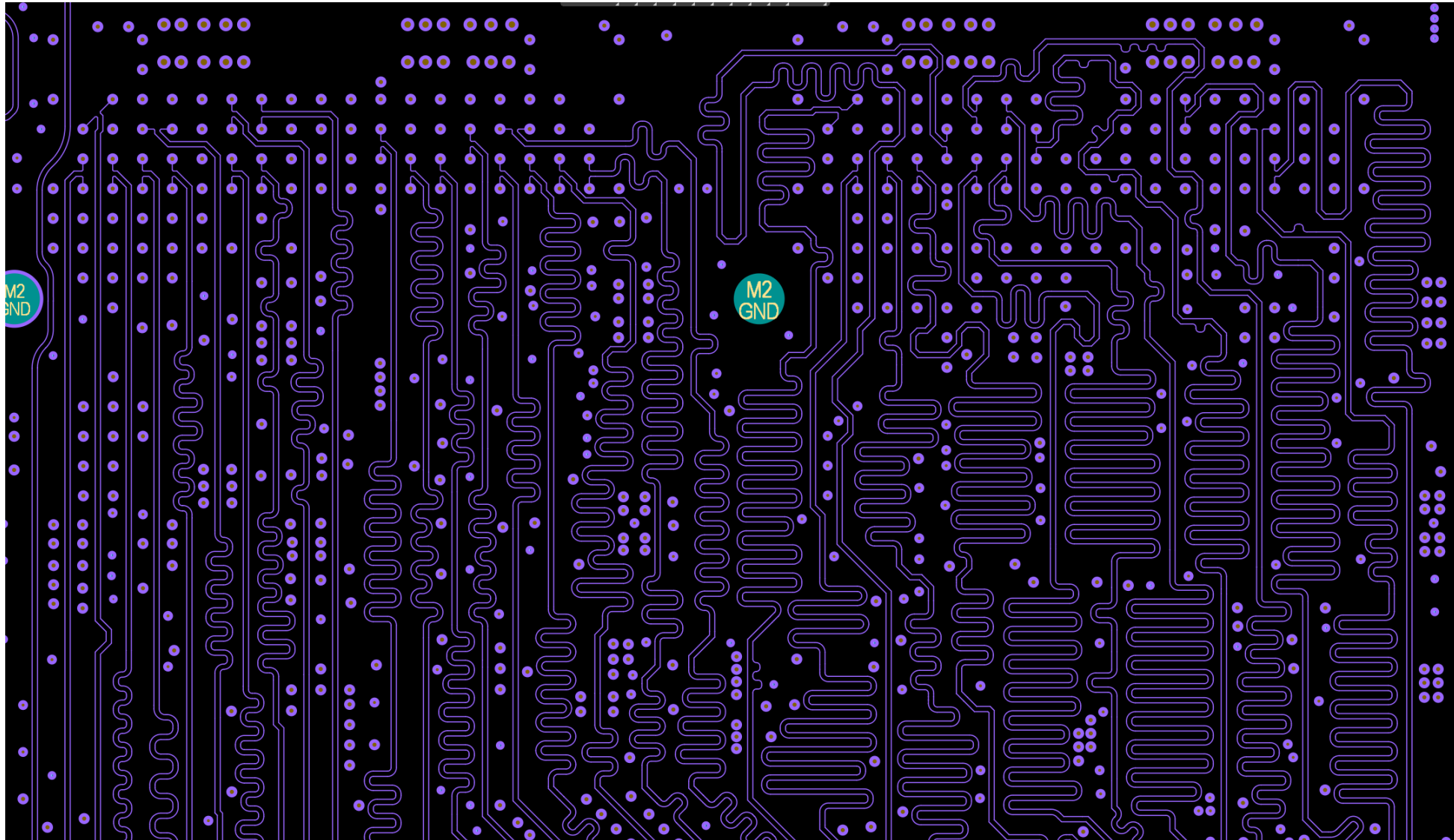
DAMC-DS812ZUP Layout details



- Zooming-in reveals complexity
- almost impossible to layout
- (many tricks used)

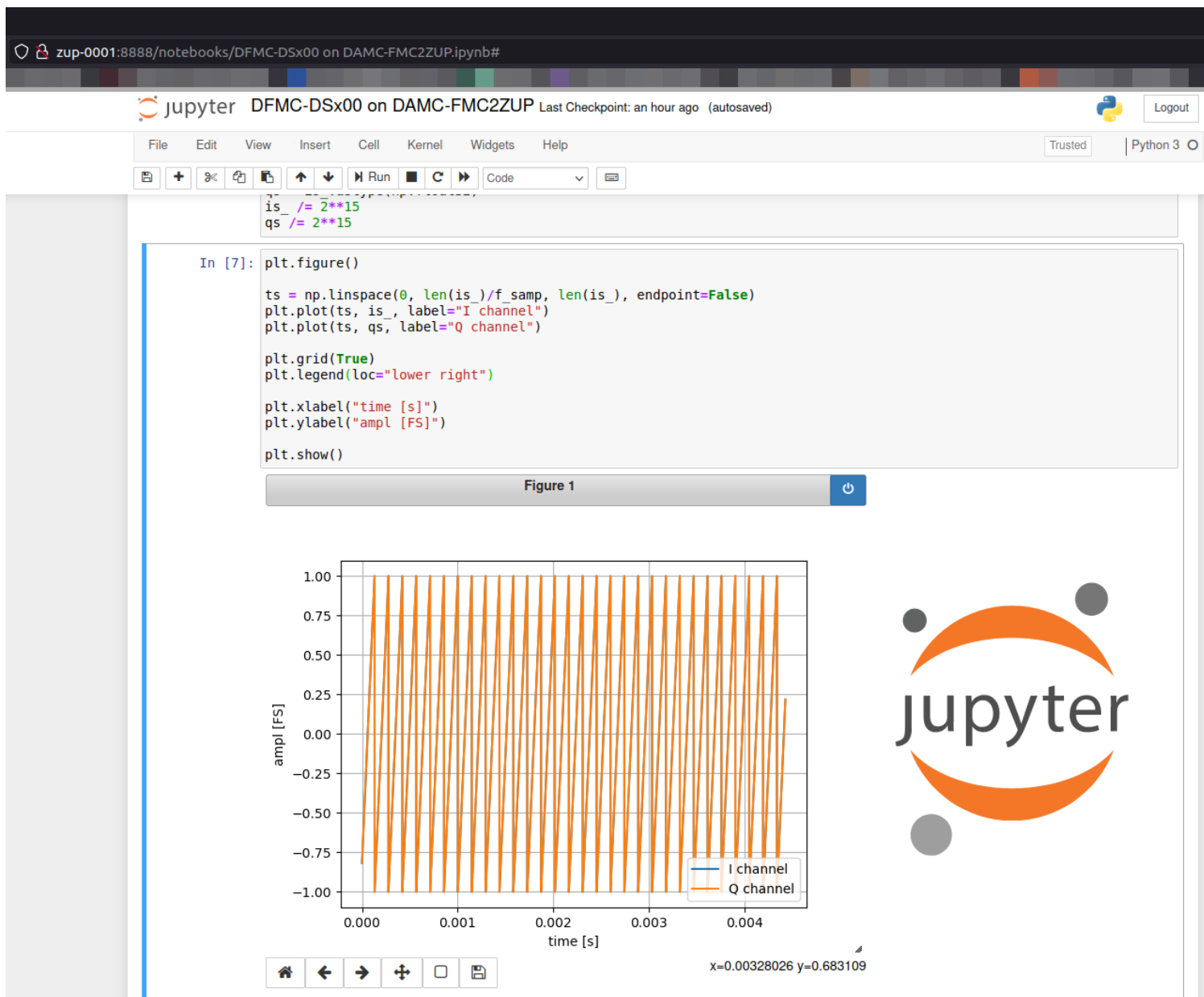


DAMC-DS812ZUP Layout details

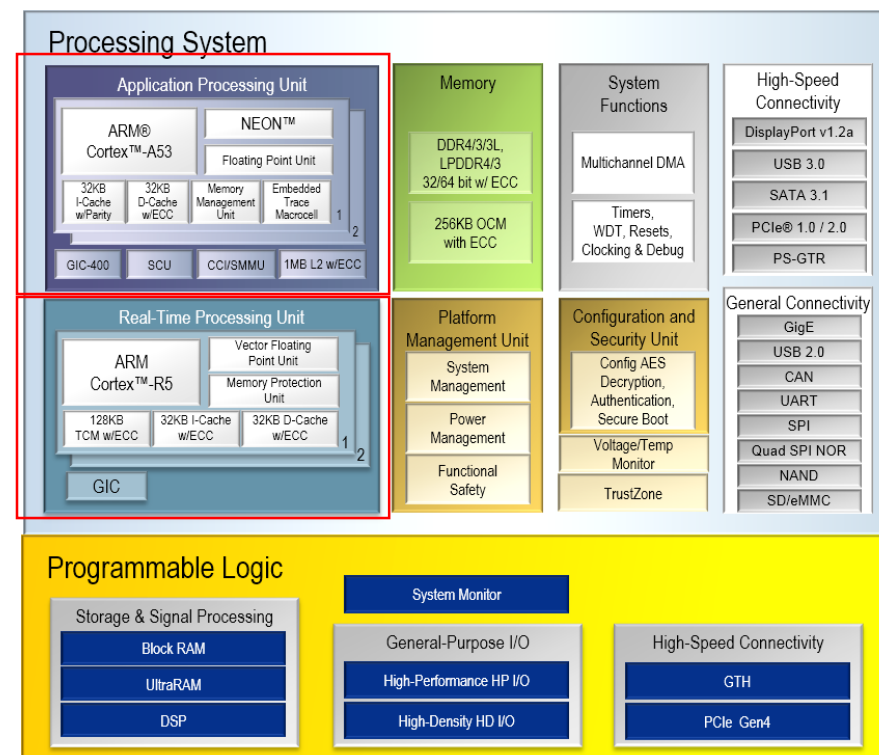


- All ADCs channels are length-matched
- Length match was difficult to achieve for center ADCs

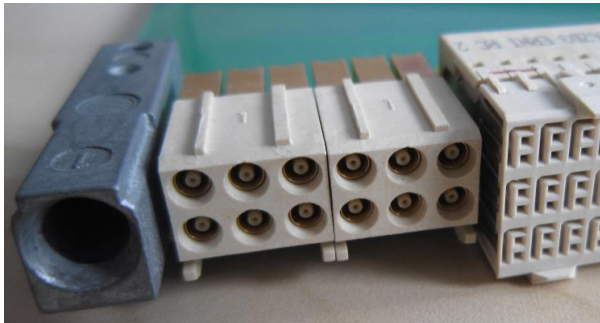
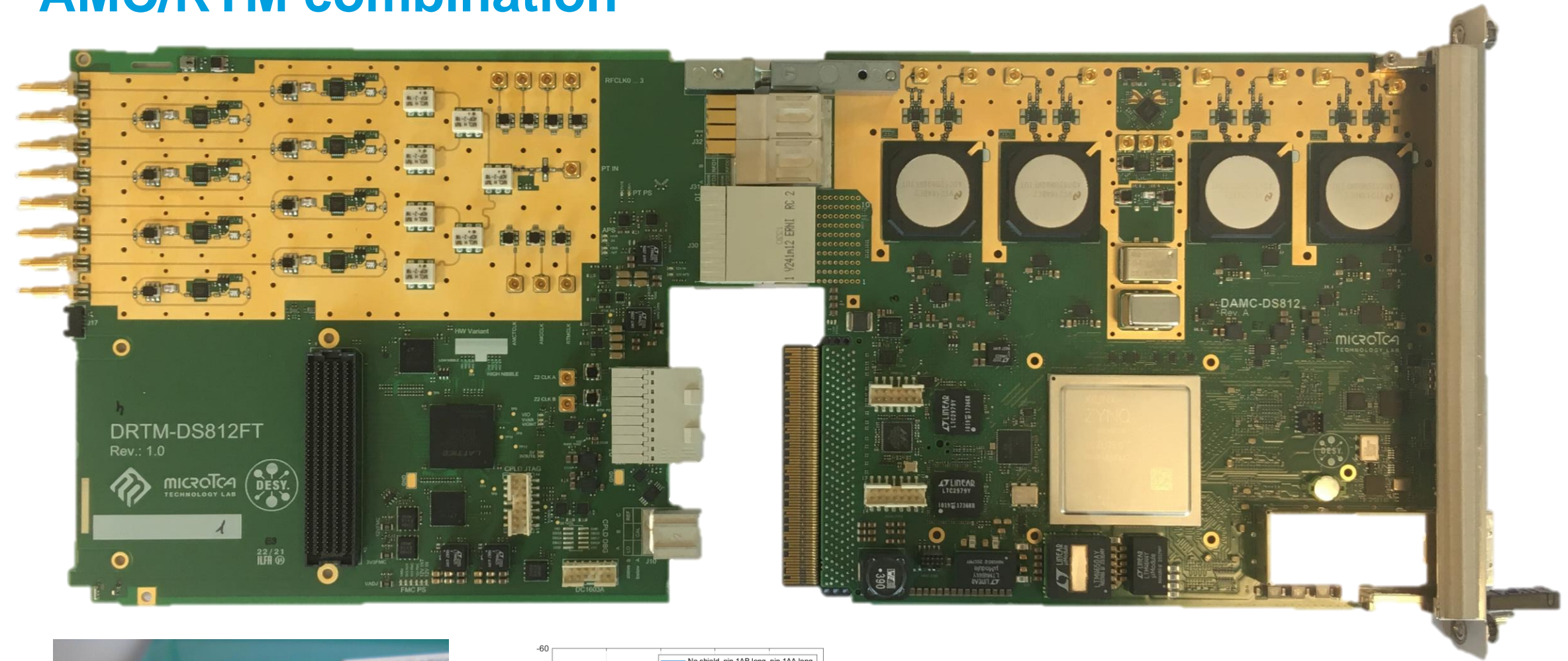
DAMC-DS812ZUP – MPSoC provides new Approach



- Board can run “fully self-contained”
- Interface via web-server
- Instant data-taking using Jupyter Notebook
- Python libraries available
- Uses RPU for bare-metal low-level housekeeping (HW configuration)

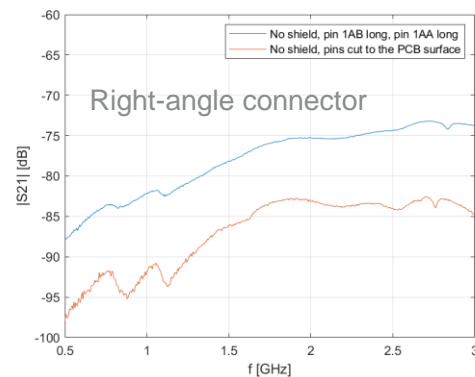


AMC/RTM combination



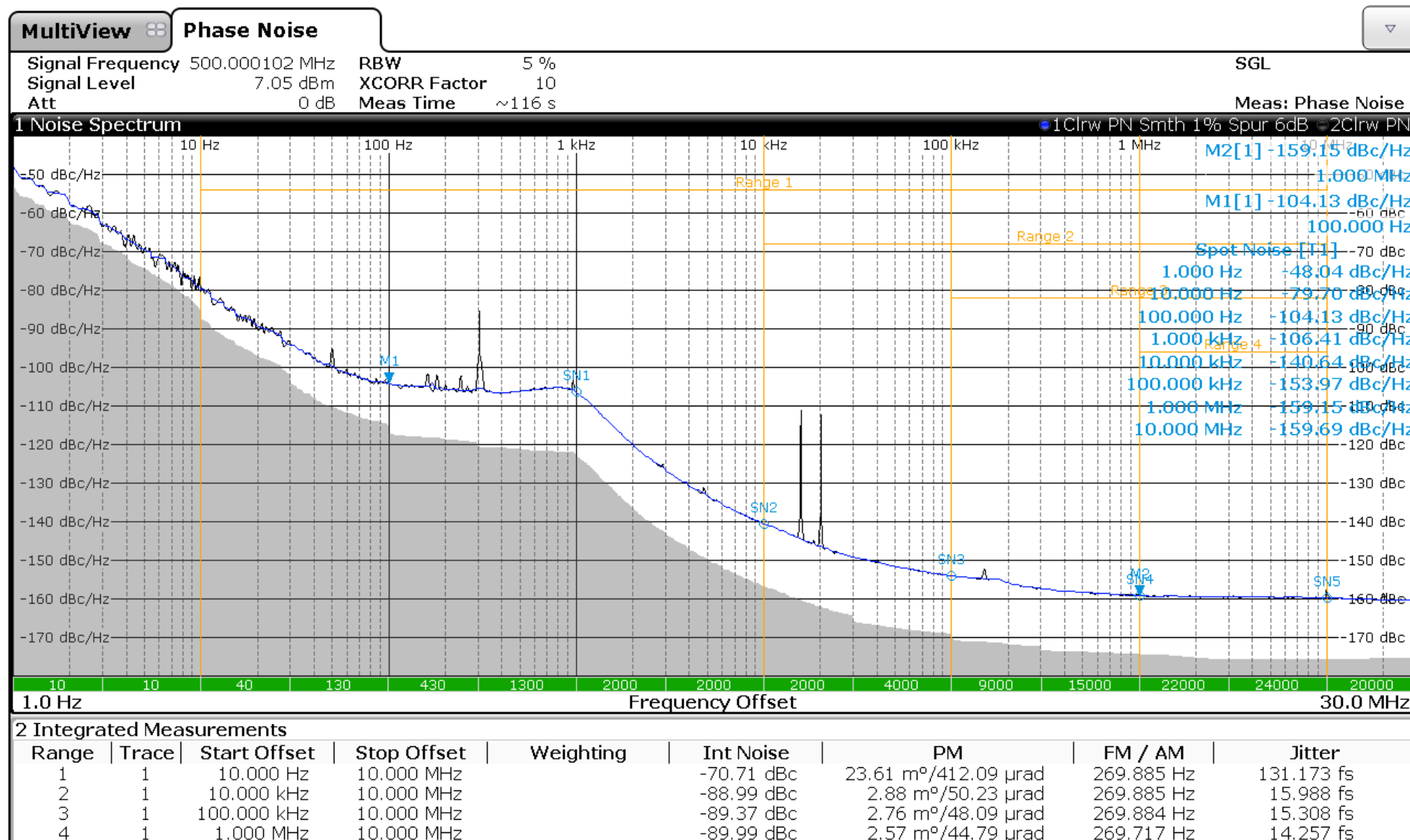
DESY.

courtesy of J. Zink



- Feed-Through RTM is available
- AMC: cables / RTM: right-angle connector
- Shielding between channels better than -85dB

On-Board Clock Performance

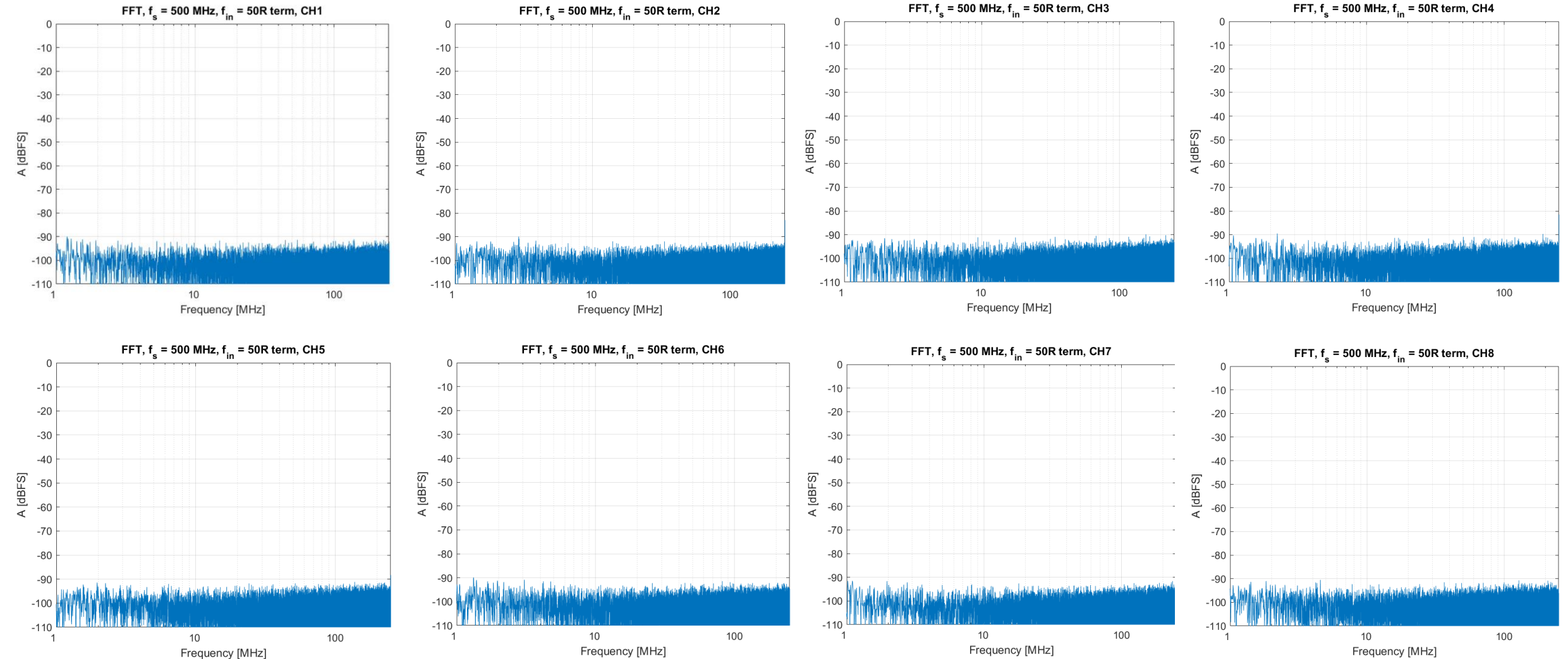


- On-board OCXO, PLL, clock fanout
- Achieves 14.25fs Jitter (at 500 MHz)

courtesy of J. Zink

Direct Sampling RF performance

- Investigations ongoing
- Excellent direct sampling performance

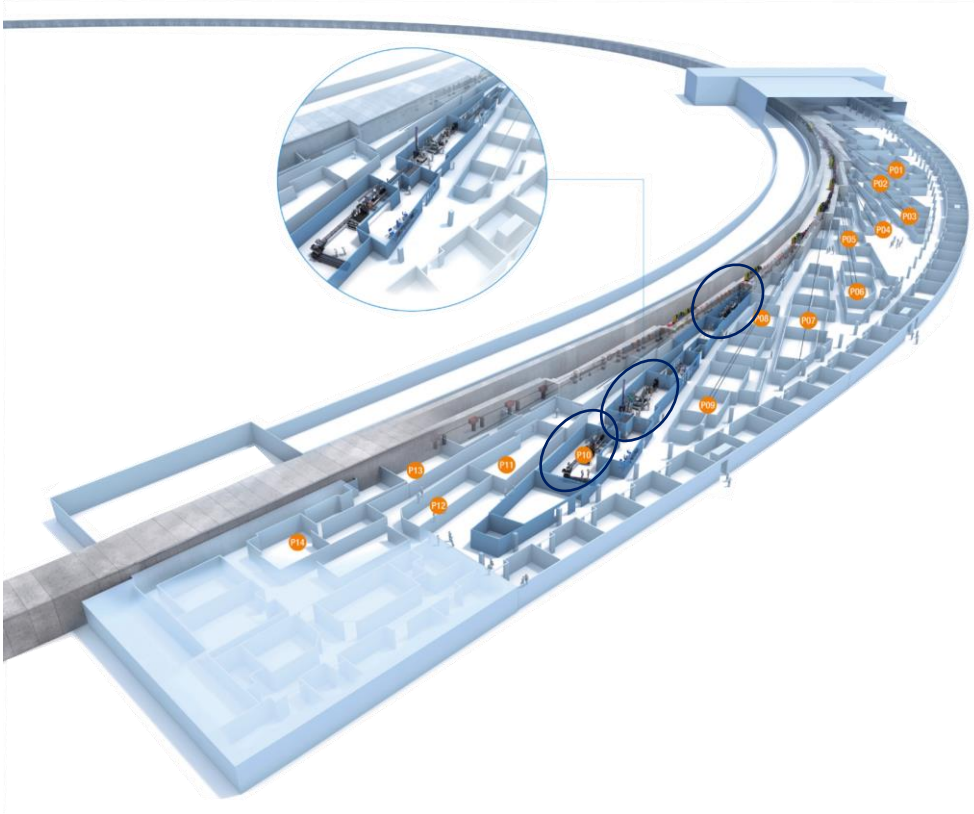


All images courtesy of J. Zink

MicroTCA.4 Motion Controller

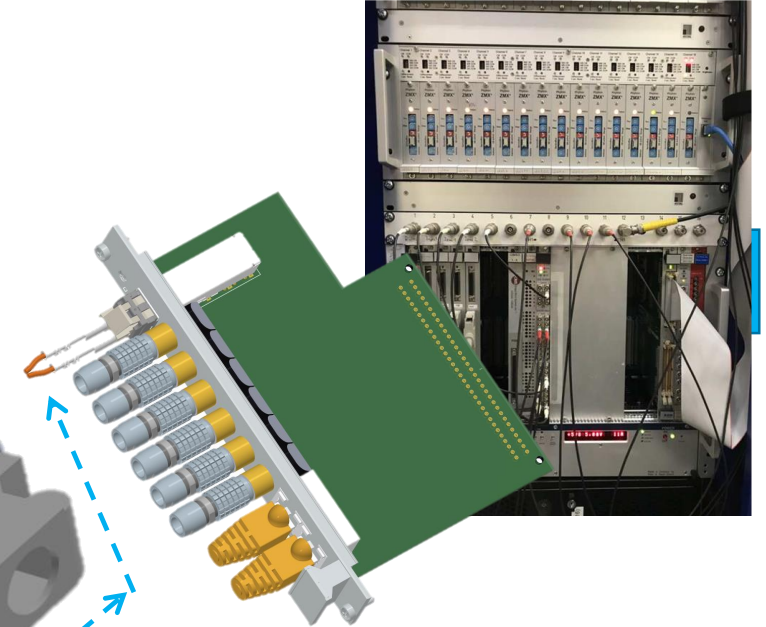
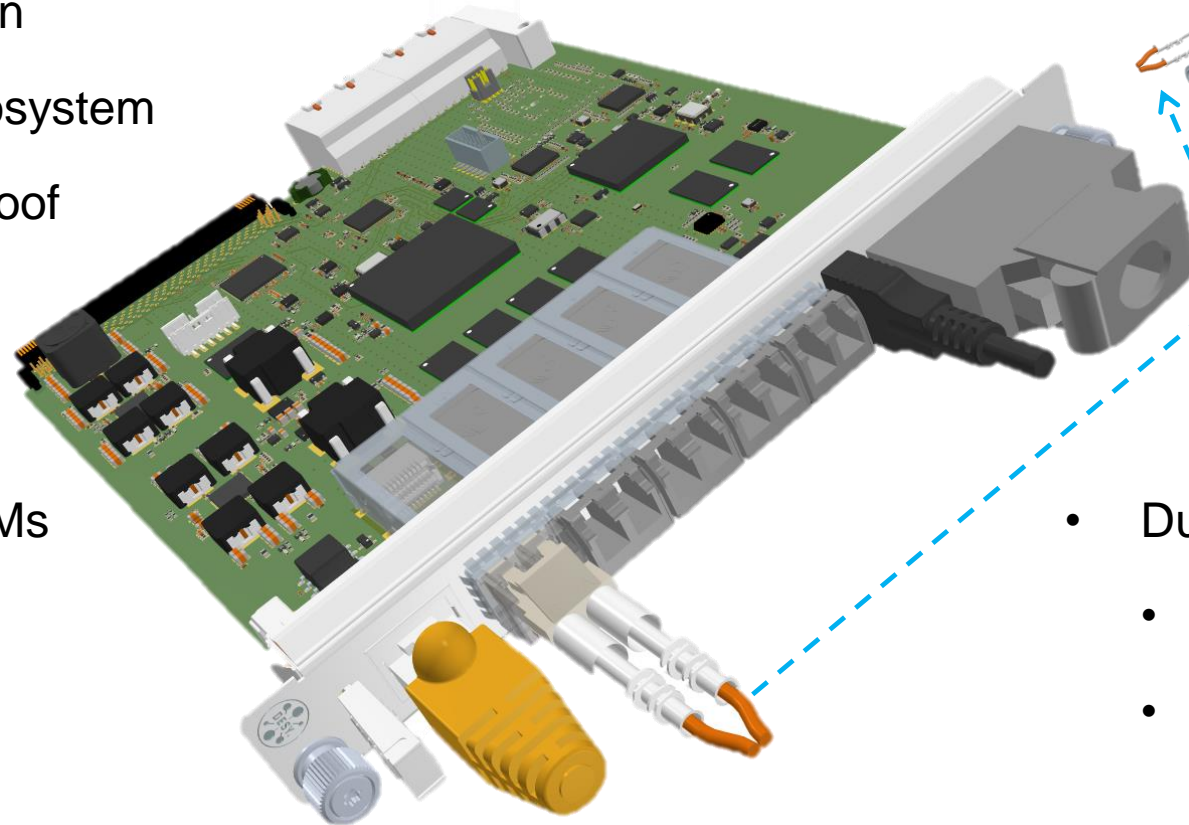
MicroTCA Motion Controller

- We need to move motors in experiments
- Existing solution not suited for new installations
- We decided to develop a motion controller card



The new MTCA.4 Motion Controller Card

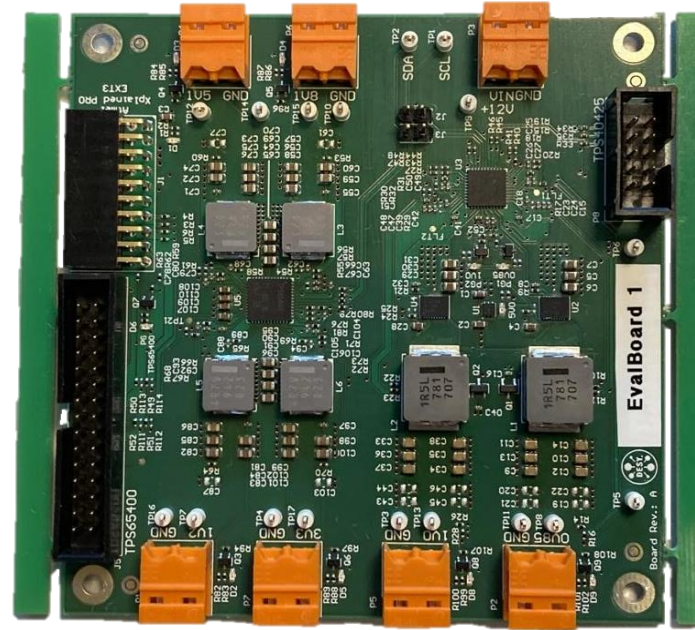
- Can control 16 motors / axes per board
- Scalable (interconnection of several cards) in the crate and campus-wide
- Support of triggers (cards can communicate with each other)
- Backward compatibility with existing installations at, DESY DOOCS and Tango connection
- Integration in the ecosystem
- Based on a future-proof standard
- Significantly less rigid cables
- Expandable with RTMs



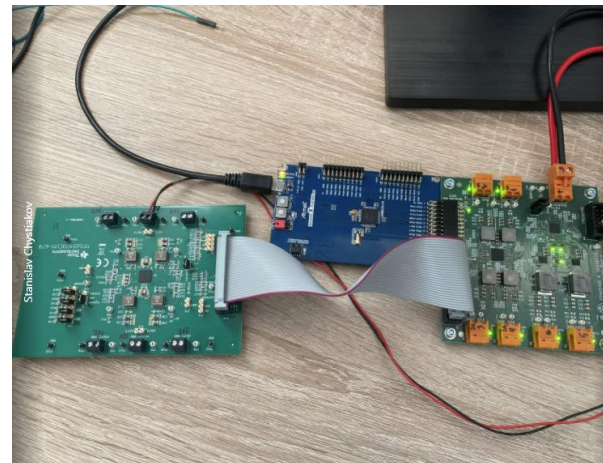
- Dual FPGA:
 - Uses Kintex-7 for real-time tasks
 - Uses US+ MPSoC for Communication

Cost-Optimization

- Two FPGAs with small pin count (no FMC support)
- components shared with DAMC-FMC2ZUP, DAMC-Z7IO and DAMC-DS812
- Omission of White-rabbit, bi-directional clock cross point switch, etc.
- Application-specific clocking
- Optimized **power system**



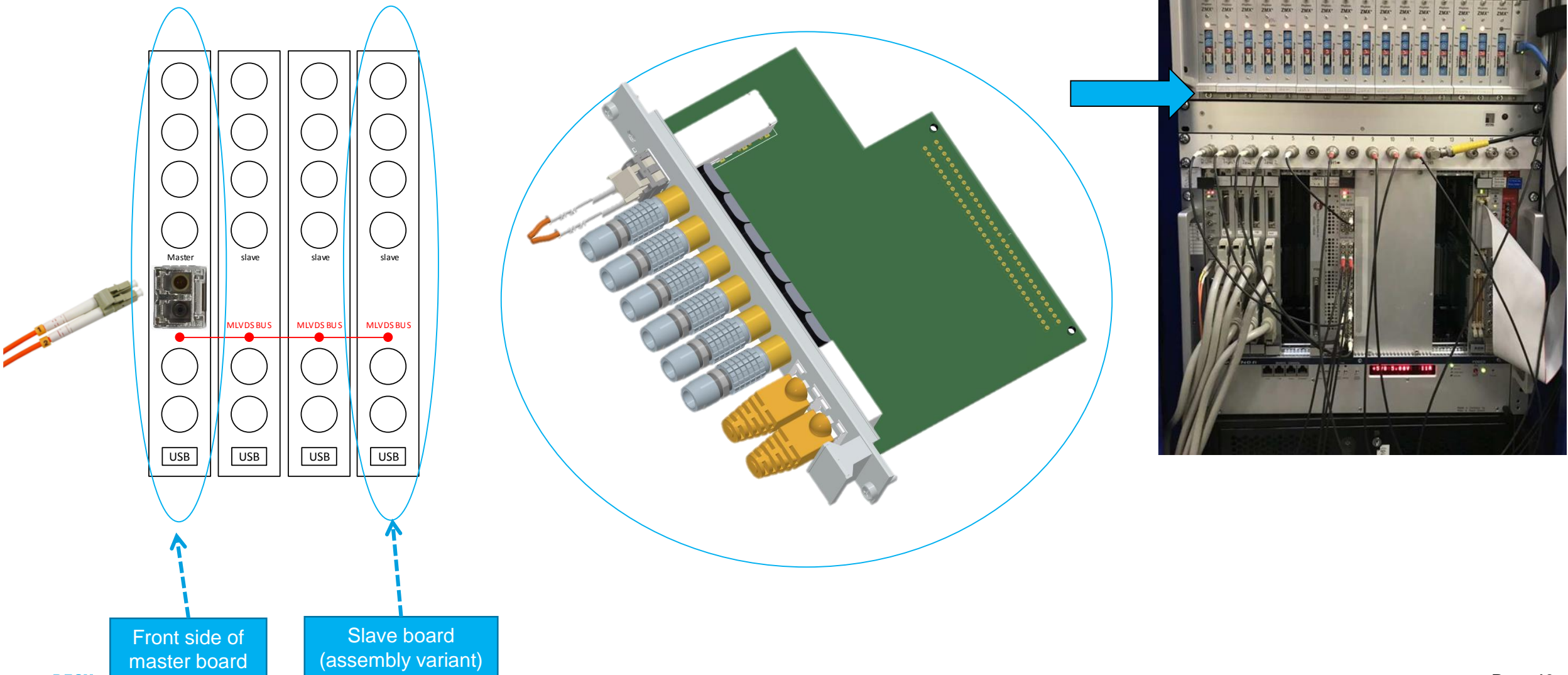
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1V8	TPS65400	NaN	PG_ERR	OTH OFF
1V5	TPS65400	NaN	PG_ERR	OTH OFF
1V2	TPS65400	NaN	PG_ERR	OTH OFF
0V85	TPS40425	0.014 V	PG_OK	OFF
1V0	TPS40425	0.000 V	PG_OK	OFF
Your board name> pu				
Your board name> cf				
CHAN	DEVICE	VOLTAGE	PGOOD	FAULTS
3V3	TPS65400	NaN	PG_OK	
1V8	TPS65400	NaN	PG_OK	
1V5	TPS65400	NaN	PG_OK	
1V2	TPS65400	NaN	PG_OK	
0V85	TPS40425	0.848 V	PG_OK	
1V0	TPS40425	1.000 V	PG_OK	
Your board name> pd				
Your board name>				



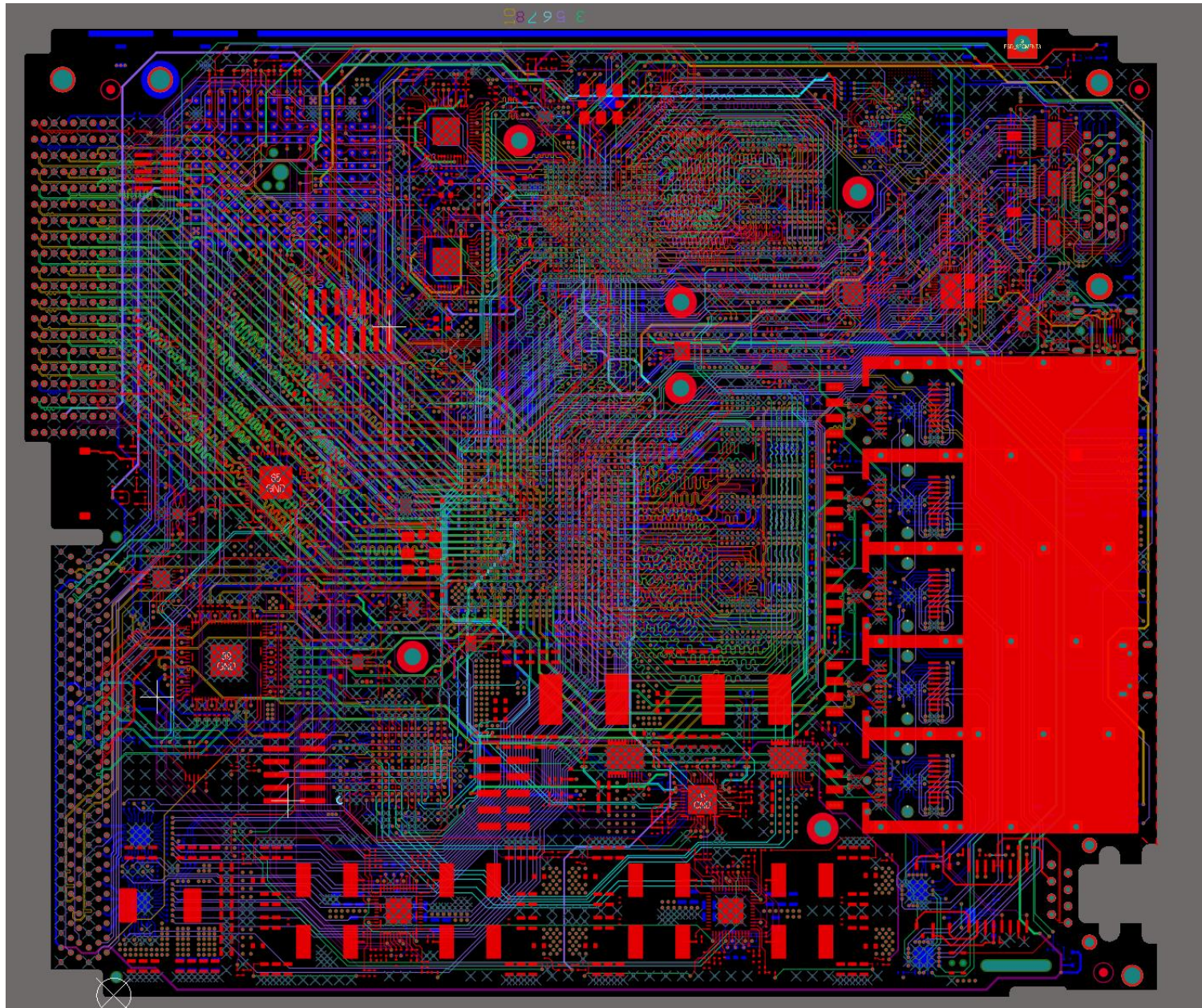
courtesy of S. Chystiakov

Fan-out board – backwards compatibility to existing motor drivers

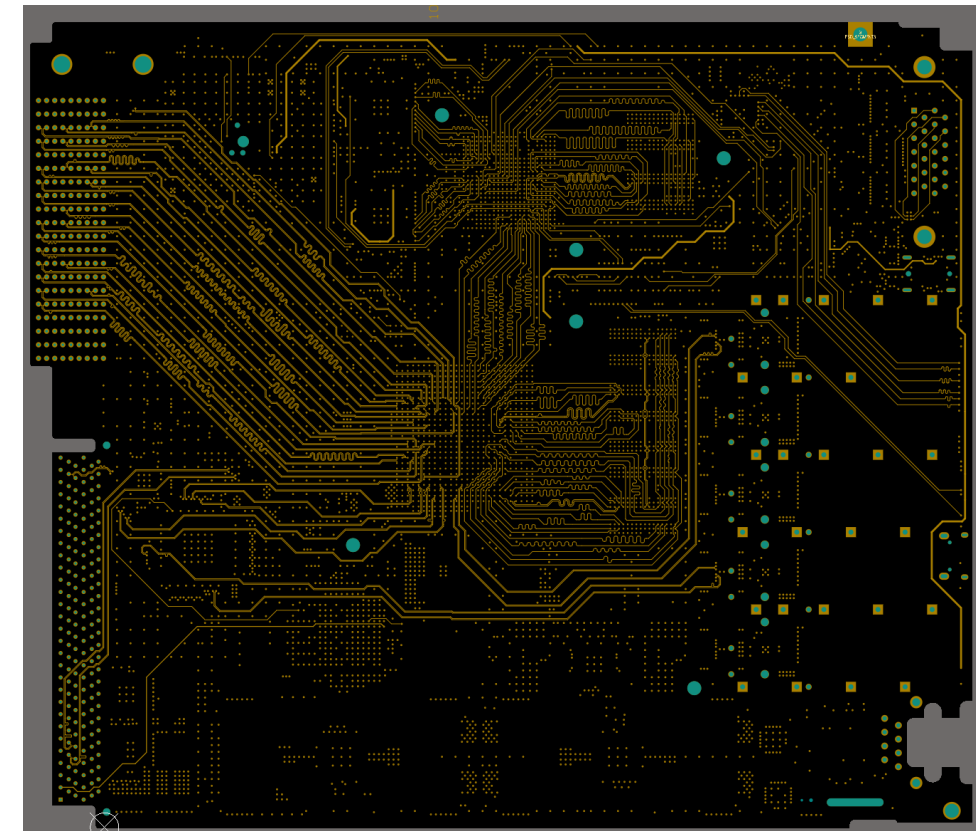
- Optical SFP+ Interface to STEP/DIR motor drivers – no SCSI cables anymore
- Encoder support (1 per axis)



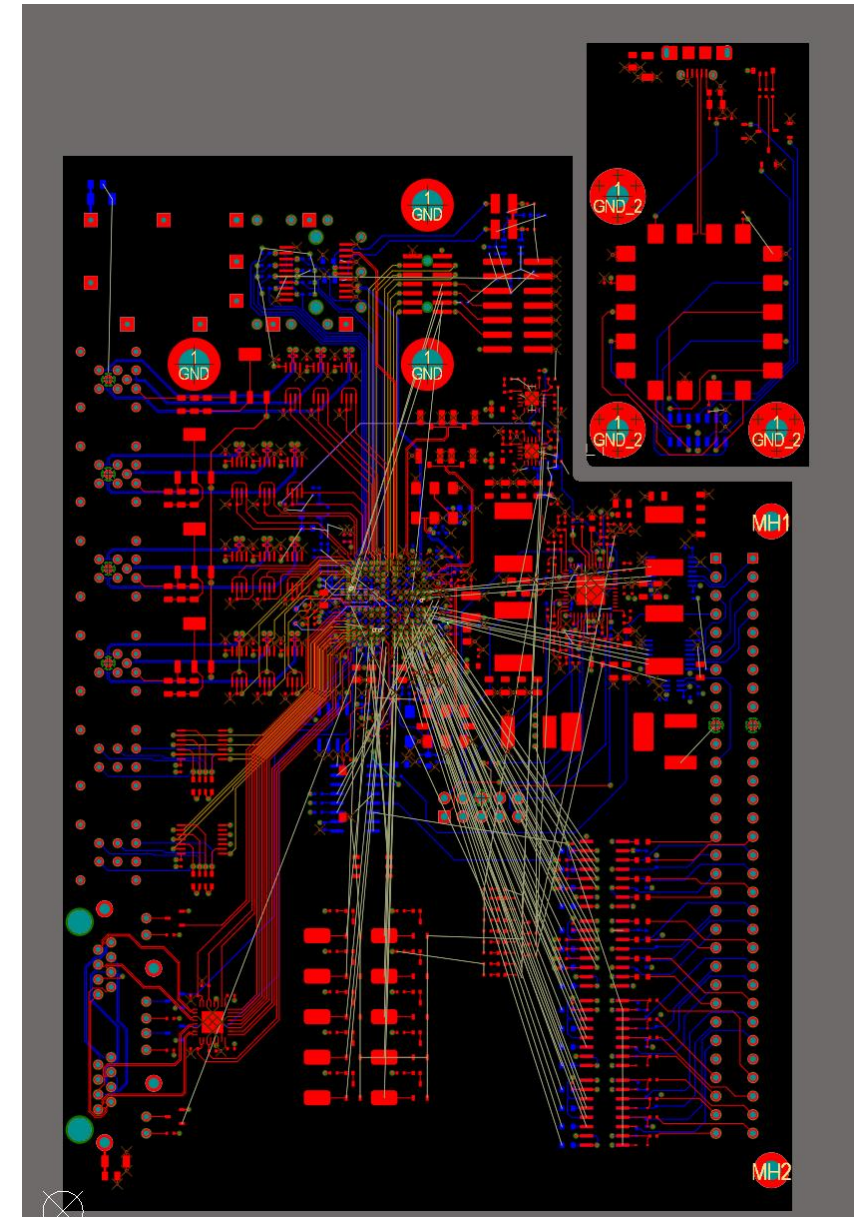
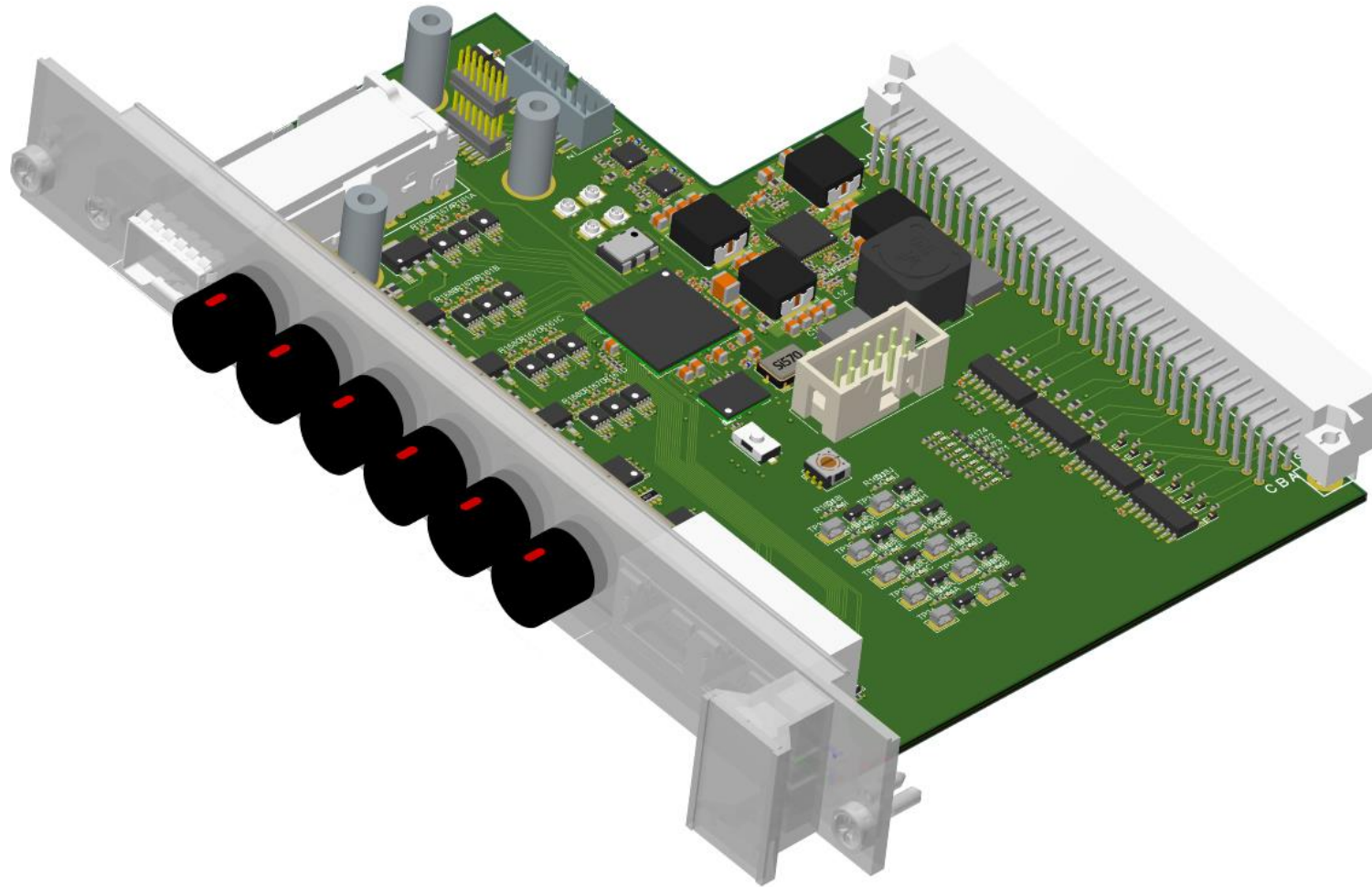
Current State of work: Motion controller



- Everything is fully routed and matched
- All components in house
- We are checking the design



Current State of work: Fan-out Board



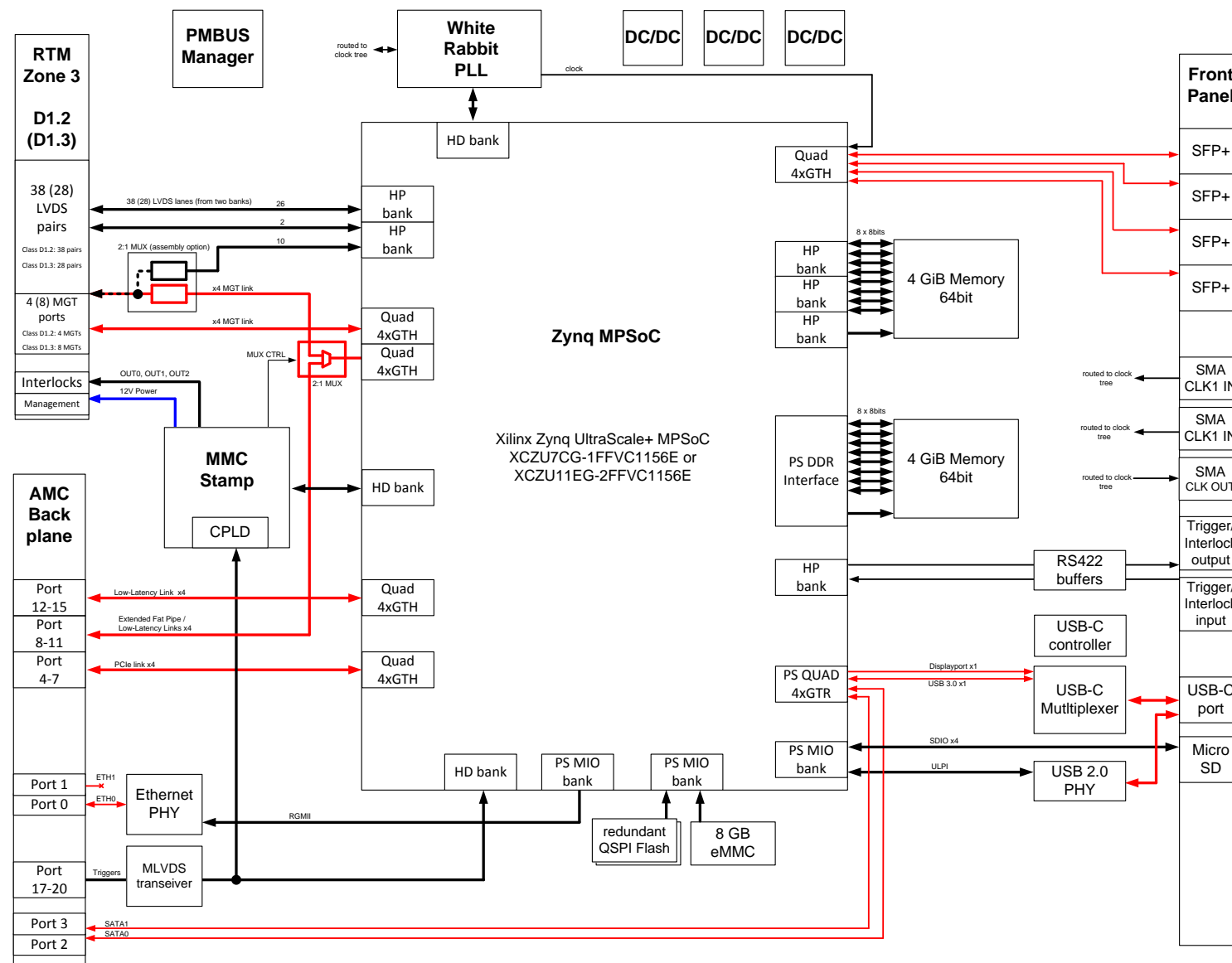
DAMC-BPMZUP

DAMC-BPMZUP - outlook

- Is a board under development
- Allows D1.2 / D1.3 class RTM
- up to 8 MGTs to RTM
- Very flexible clocking system with White Rabbit support
- Targets JESD204B applications
- Shares components with DAMC-Supercarrier FMC2ZUP
- Cost-Optimized version
- Uses Ultrascale+ MPSoC (smaller package than Supercarrier)
- 2 interfaces with 4GiB of DDR4 each
- Trigger input/output on front panel
- SFP+ Output on the front panel



DAMC-BPMZUP – block diagram

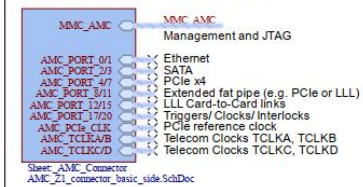


Design Support

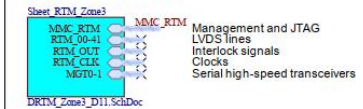
AMC Template

DESY MicroTCA.4 AMC Implementation Proposal

AMC Connector (Backplane)

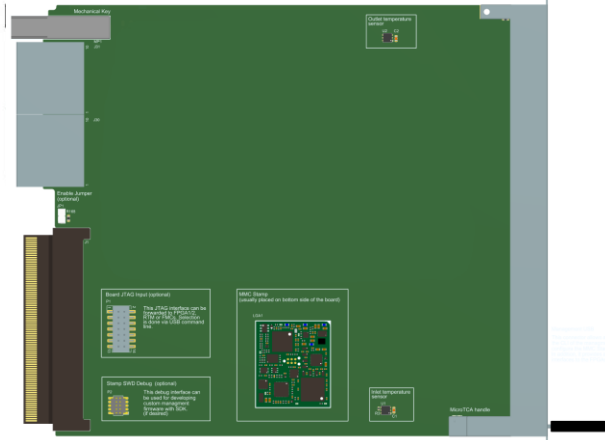


RTM Connector



Altium Designer® Board Template

The schematics and PCB files are provided free-of-charge. Please contact DESY.



Preview. Do not distribute.

Note

This is an example AMC implementation proposal according to MicroTCA 4.

By publishing recommendations, DESY aims to ease the design of custom MicroTCA boards. This solution bases on the DESY MMC stamp, which was designed to allow fast development of MicroTCA boards with maximum interoperability between different components.

The MMC stamp is delivered pre-programmed and is intended to avoid any management firmware development by the user. If AMC developers wish to vendor-specific management extensions, they can be realized by licensing the MMC Software Development Kit.

Always cross-check with the MicroTCA standard. If in doubt, higher priority shall be given to the standard. The user is responsible to verify that all implementation details fit to his design requirements.

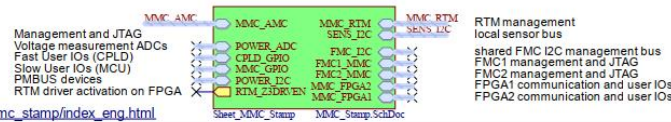
License

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MMC Stamp LGA Module

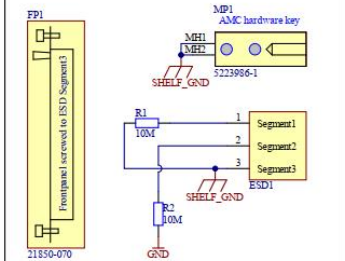
Detailed information about MMC-STAMP can be found here:
https://techlab.desy.de/products/module_management_controller/mmc_stamp/index_eng.html



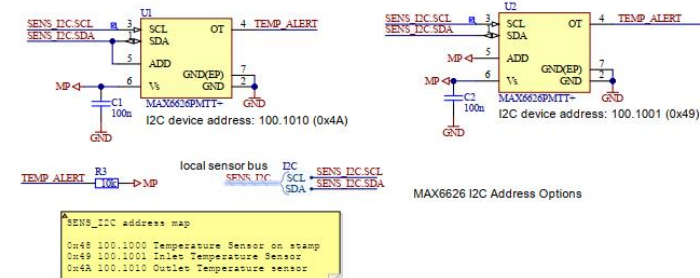
Change List

V0.1 - initial revision
V0.2 - spelling corrections; License set to "TBD".

MicroTCA Mechanics



Temperature Sensors (mandatory according to MTCA standard)



Fiducials (recommended)



microTCA
TECHNOLOGY LAB

Noikstrasse 85
22607 Hamburg
mtca-techlab@desy.de

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FILENAME: MTCA_AMC-Template_Top.SchDoc

Project Title:
MTCA_AMC-Template_Protob
Schematic Title:
AMC Template Top
DATE: 09.10.2021 10:43:58

Engineer 1: Michael Ferner
Engineer 2: Robert Wedel

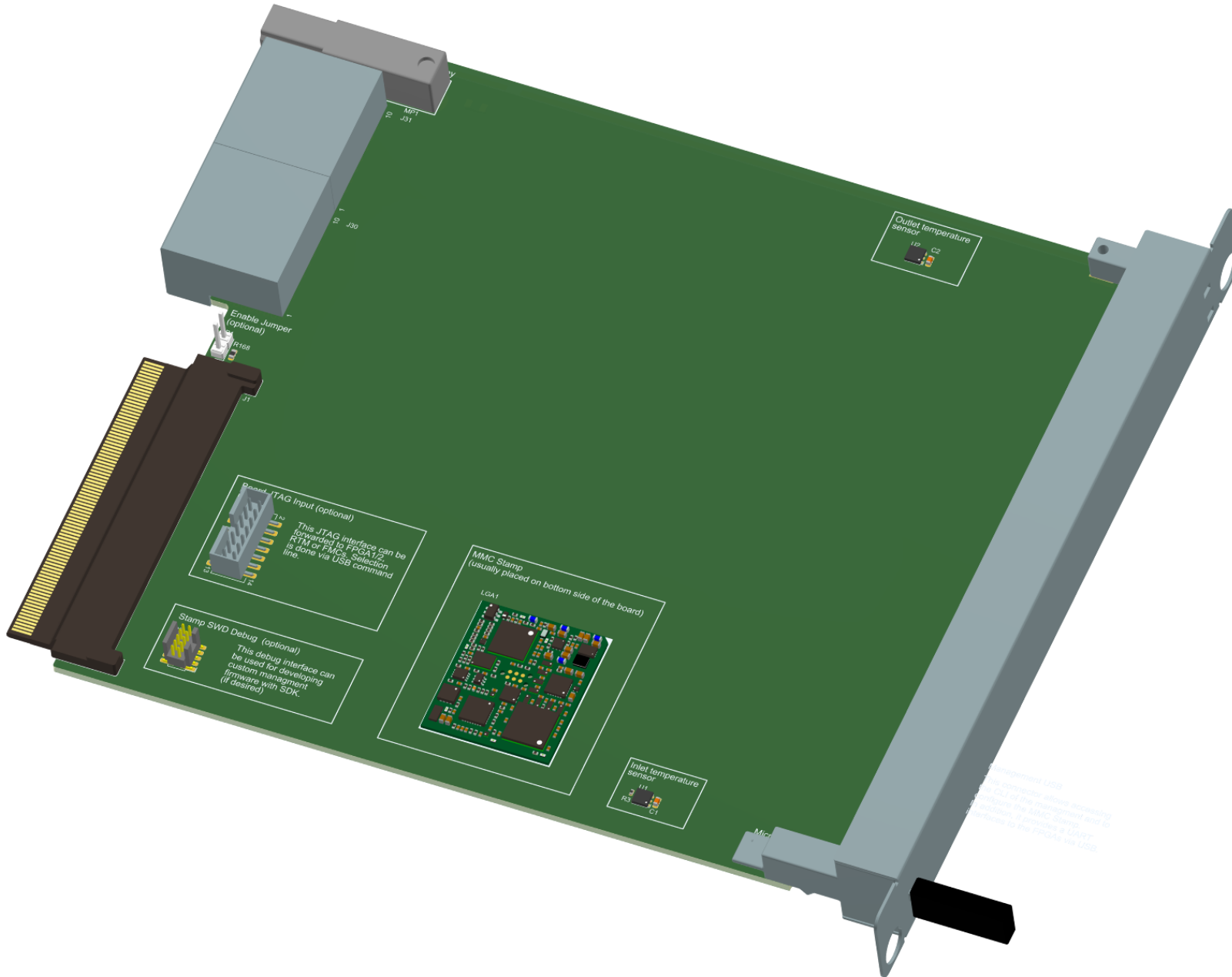


Rev: 0.1
Size: A3
Sheet:

1 of 4

- DESY encourages custom HW developments
- We provide a design template
- Includes lots of explanations and hints

AMC Template - Altium™ Designer board



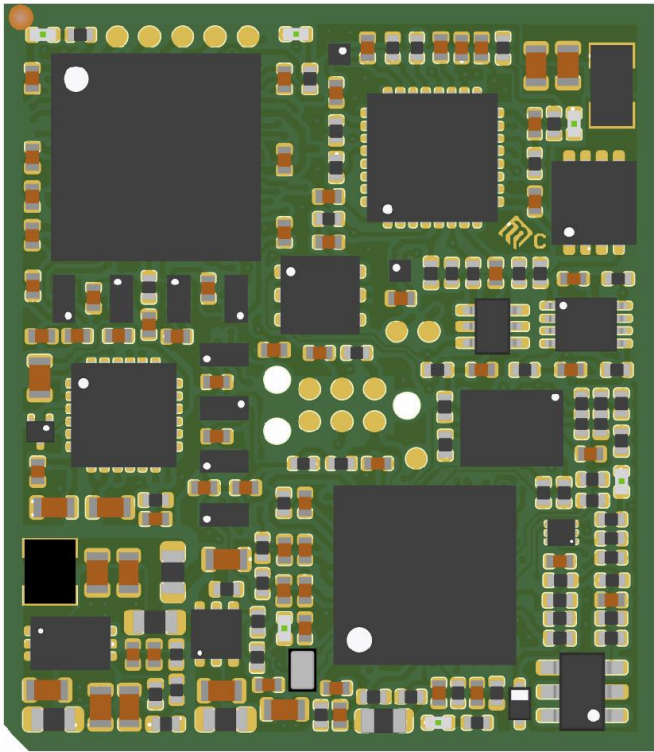
- Schematics and Layout available for free
- Proven mechanical shapes, footprints and symbols
- Jump-Start MicroTCA design
- 3D bodies included

AMC Template - Based on MMC Stamp

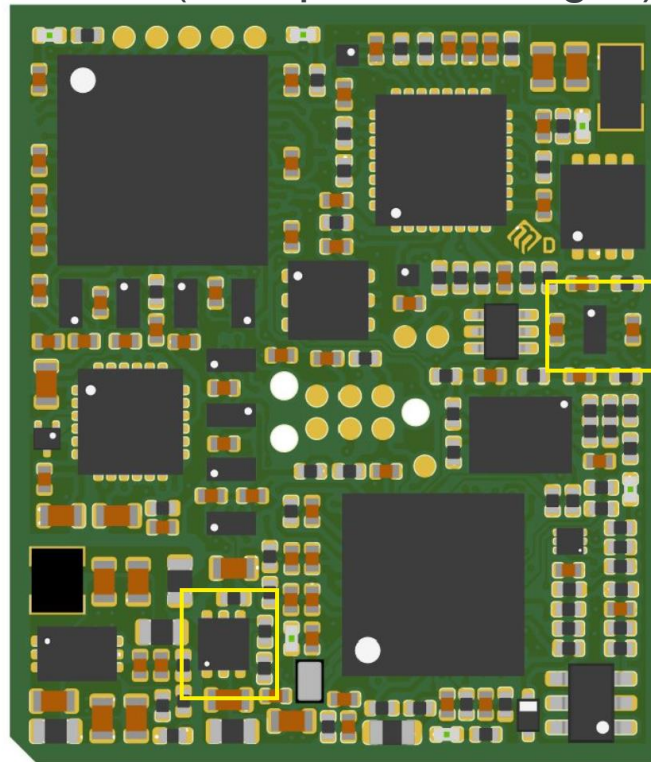
MMC Stamp is available (Obsolescence Management is done by DESY)

- All changes transparent to the user (we take care of firmware)

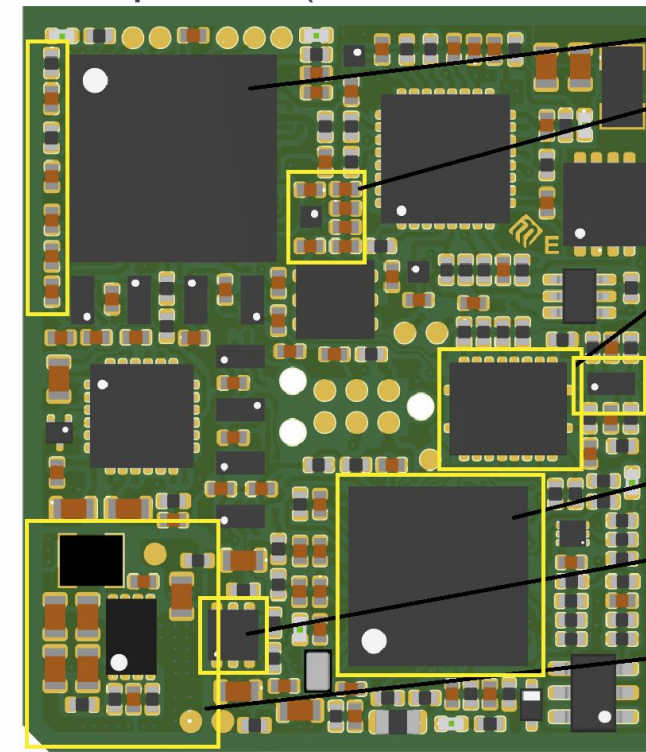
out of stock



current (transparent changes):



Backup 2022 (under verification):



Low-Power CPLD

New LDO (because of CPLD):

I2C Multiplexer (same but different package, old one is EOL)

Same I2C Buffer in different footprint (availability)

SAM4LC8CA instead if SAM4LS8CA
Same core, two more peripherals,

different LDO

different DC/DC
converter (on same switching
frequency)

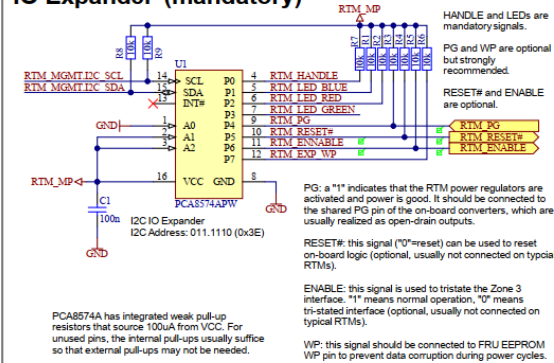
Firmware upwards/backwards compatibility

RTM Template

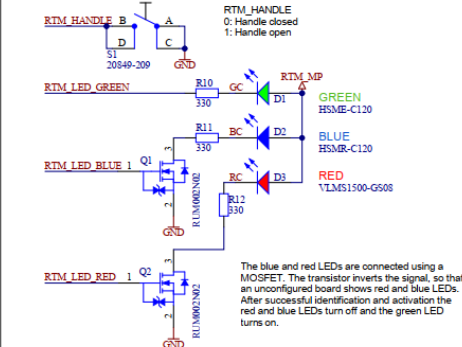
DESY MicroTCA.4 RTM Implementation Proposal

Preview. Do not distribute.

IO Expander (mandatory)



Handle and LEDs (mandatory)



Note

This is an example RTM implementation proposal. By publishing recommendations, DESY seeks compatibility of RTMs to different AMCs. The DESY MMC management solution is intended to be compatible to this recommendation.

However, AMCs can require vendor-specific management solutions on the RTM, including requirement of different ICs, I2C addresses or special compatibility records in the FRU.

Always consult the AMC designer for specific RTM implementation requirements.

Always cross-check with the MicroTCA standard. If in doubt, higher priority shall be given to the standard.

Carefully cross-check this proposal and verify that all implementation details fit to your design requirements.

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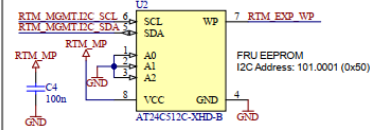
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TBD

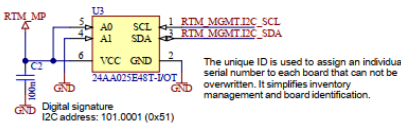
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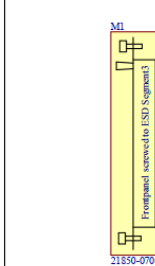
FRU (mandatory)



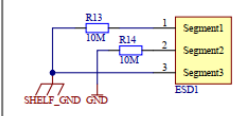
Unique ID (recommended)



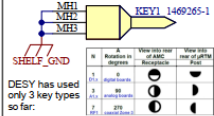
Rear panel (mandatory)



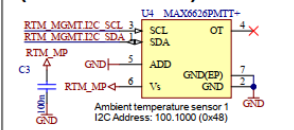
ESD segment (mandatory)



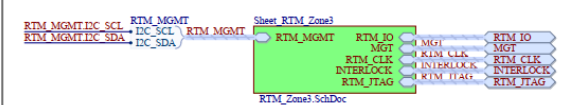
Mechanical key (mandatory)



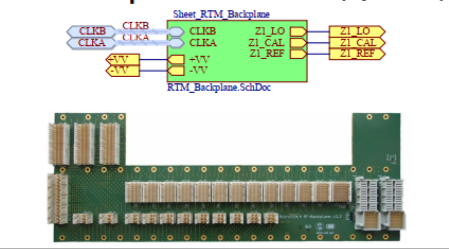
Temperature sensor (recommended)



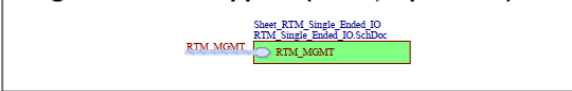
Zone 3 Connector (mandatory)



RTM backplane connectors (optional)

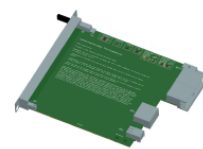


Single-ended IO support (avoid, if possible)



Altium Designer® Board Template

The schematics and PCB design files are provided free-of-charge. Please contact DESY.



Fiducials (recommended)



Change List

V0.1 - initial revision
V0.2 - added table of used mechanical keys; changed license text
V0.3 - added change list; added notice on license terms
V0.4 - corrected PG and ENABLE signals to match MTCA.4 standard (had inverted logic draft MTCA standard)
V0.5 - license set to "TBD".

MICROTCA
TECHNOLOGY LAB

Notkestrasse 85
22607 Hamburg
mtca-techlab@desy.de

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FILENAME: DRTM-Template_TOP.SchDoc

Project Title:
RTM-Template.PjPcb

Schematic Title:
RTMManagement Top

DATE: 12.04.2021 15:19:39
Engineer 1: Michael Fenner
Engineer 2: Robert Wedel



Rev: 0.4
Size: A3
Sheet

1 of 4

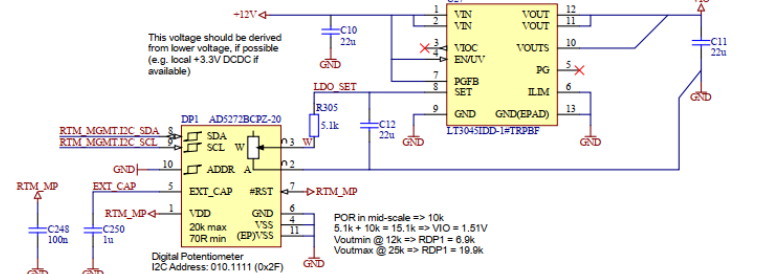
- Same as for AMC
- Explanations beyond standard
- Collection of best practices

Single-Ended IOs (optional)

No extra components needed, ignore this page!

DESZY recommends to use only LVDS signals at RMT-HIO pins. LVDS is a common standard will always be compatible, independent of FPGA bank I/O voltage. By using LVDS signals only, no glue logic, no voltage translation and no coupling capacitors are necessary. Translating single-ended interfaces (such as SPI) to LVDS to cross zone 3 is preferred and requires no variable voltage supply or interaction with MMC management. However, there are cases (e.g. where more signals need to be transferred over Zone 3 than pins are available) where the user decides to use single-ended I/Os. In this case, a variable I/O voltage on all these signals is needed. Depending which FPGA type and which bank voltage was chosen on the AMC, the voltage of the Zone 3 has to be configured to precisely match the FPGA bank voltage. Failing to adhere to the specific bank voltage requirement will exceed the absolute maximum ratings of the I/Os on the AMC and may lead to permanent damage. The user has to ensure that the voltage of the I/Os is within the range of the supported I/O voltages supported by the module management controller (MMC) on the AMC. The following implementations are supported by DESZY MMC. Single-ended RMT-HIOs shall be avoided wherever possible.

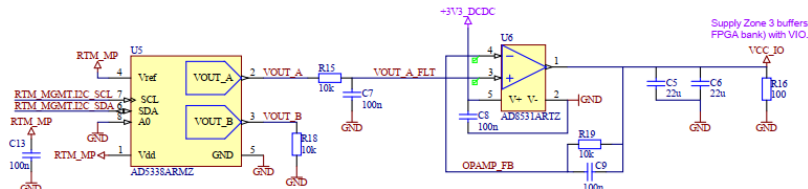
Supply Zone 3 buffers (c
FPGA bank) with 1/10



Depending on the chosen FPGA bank voltage, the MMC, a matching Z3 voltage has to be selected. Old FPGAs (Virtex®-4, Virtex®-5) support bank voltages of up to 3.3V. Most DESY boards used 2.5V bank voltage on the Z3nc3 interface. Modern FPGAs (Virtex®-6 and newer) support 1.8V on Z3 only. If single ended I/Os on Z3 are needed, DESY recommends the choice of the MMC on the AMC will set up the digital potentiometer in such a way that LDO generate the I/O voltage that matches the specific FPGA bank voltage. It is supported by DESY MMC Stamp and soon will be added to the MMC of other DESY designs such as JMMC-EM25, DMMC-FMC10 and DMMC-T037.

The digital potentiometer can be programmed to a fixed start-up value (non-volatile memory). Support of one specific 3rd-party AMC board can be achieved by programming a fixed value into the resistor, resulting in a correct (but fixed) Zone 3 voltage. If the AMC board is changed, the potentiometer may have to be re-programmed with a different value. This solution is, even if it is proprietary, the most flexible way to allow single-ended IO compatibility across multiple vendors and MMC solutions, respectively.

Apply Zone 3 buffers (or GA bank) with VIO.



This is the solution used in all legacy DES3 RTMs (DRTM-AD84, DRTM-P274, DRTM-DWC10, DRTM-DWC8VM1, etc.). It is also supported by Struck SIS8300L2 and SIS8325 and SIS8300K. This solution concept uses an MMC controlled by the AMC to manage the RTM. The RTM will only support up to 2500000000 (2.5G) of data rate (2500000000/3+3V3_DCCD) here and the AMC has to be aware of this solution and has to specifically support it. 3rd-party AMCs that are not adapted to this solution, can not operate the RTM at all. However, all existing AMCs with DES3 MMC V1.0.0 or DES3 MMC Struck will support this solution out-of-the-box.

```

RTM_MGMT
├── 12C_SCL
├── 12C_SDA
└── RTM_MGMT.12C_SCL
    └── RTM_MGMT.12C_SDA

```



MicroTCA
TECHNOLOGY

Notkestrasse 85
22607 Hamburg
mtca-techlab@desy.de

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FILENAME: RTM_Single_Ended_IO.SchDoc

Project Title:

RTM-Template.PriPcb

Schematic Title:

Zone 3 single-ended IC

DATE: 12.02.2021 15:19:40

Engineers 1: Michael Fenger

Engineer I.	Michael Fennie
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Rev: 0.3
Size: A3
Sheet:

3 of 4

- yes
DESY boards only
legacy implementation

- RTM Backplane design information included

RTM Backplane Connectors (optional)

The MicroTCA specification Revision 4.1 defines an optional RTM backplane. It is used for distribution of high-precision clocks inside the chassis to MicroTCA RTMs. In addition, a clean bipolar supply voltage can be distributed on this backplane. Special eRTMs (without connection to AMC backplane) generate precision clocks and reference signals for the RTMs. A special rear power module can generate a clean supply voltage for the RTMs. Management of the eRTMs and rear power supplies is realised by using a MCH-RTM, which forwards the rear management signals the front MCH.

A 12-slot chassis with the shown RTM backplane is available from nVent / Schroff GmbH. A modular rear power module and the MCH-RTM are available from N.A.T. GmbH. The DRTM-LOG1300 is available from DESY.

RTM Backplane Zone 1
RF cock input

connector pinout for slots #4-#12

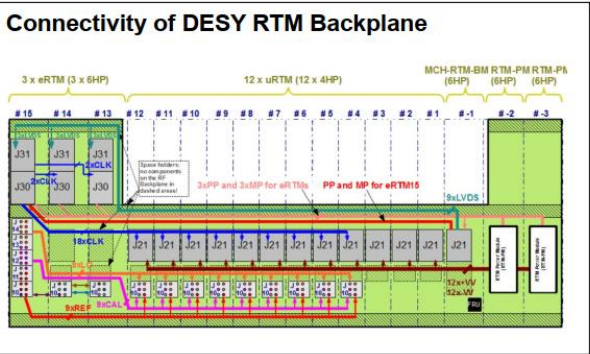
	A	B
1A	rfu	LO
1B	CAL	rfu
1C	rfu	REF

rfu – pins reserved for future use

RTM Backplane Zone 2
Analog voltage and additional clocks

+VVI/-VVI is a clean analog voltage that can be generated by the optional rear power module.

RF_CONF: Clock assignment defined with resistive divider or electronic potentiometer.



DRTM-LOG1300 - eRTM clock generator

RF_CONF Settings

The voltage on RF_CONF is used to request a specific clock assignment on the Zone1 and Zone2 connectors. A fixed voltage coming from a simple resistor divider can be presented here. Alternatively the voltage can be generated using an electronic potentiometer for maximum flexibility. (5V supply is required for full scale setting.)

Table 3: RF_CONF signal voltage levels and their assignment

State	CLKs LO CAL REF [Type, div]	Required DC level [V]	Lower limit [V]	Upper limit [V]
1	0000	0.4	0.26	0.54
2	0001	0.68	0.54	0.82
3	0010	0.96	0.82	1.1
4	0011	1.24	1.1	1.38
5	0100	1.52	1.38	1.66
6	0101	1.8	1.66	1.94
7	0110	2.08	1.94	2.22
8	0111	2.36	2.22	2.5
9	1000	2.64	2.5	2.78
10	1001	2.92	2.78	3.06
11	1010	3.2	3.06	3.34
12	1011	3.48	3.34	3.62
13	1100	3.76	3.62	3.9
14	1101	4.04	3.9	4.18
15	1110	4.32	4.18	4.46
16	1111	4.6	4.46	4.74

Table 20: J21 connector pinout for slots #4-#12

	a	b	ab	c	d	cd	e	f	ef
1	CLKA_P	CLKA_N	GND	rfu	rfu	GND	rfu	rfu	GND
2	CLKB_P	CLKB_N	GND	rfu	rfu	GND	rfu	rfu	GND
3	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
4	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
5	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
6	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
7	rfu	rfu	GND	GND	GND	GND	+VV	+VV	GND
8	GND	GND	GND	GND	GND	GND	+VV	+VV	GND
9	GND	GND	GND	-VV	-VV	GND	+VV	+VV	GND
10	PS1#	RF_CONF	GND	-VV	-VV	GND	+VV	+VV	GND

rfu – pins reserved for future use

MICROTCA
TECHNOLOGY LAB

Notkestrasse 85
22607 Hamburg
mtca-techlab@desy.de

Project Title:
RTM-Template.PjPob

Schematic Title:
RTM Backplane Connectors

DATE: 12.02.2021 15:19:40

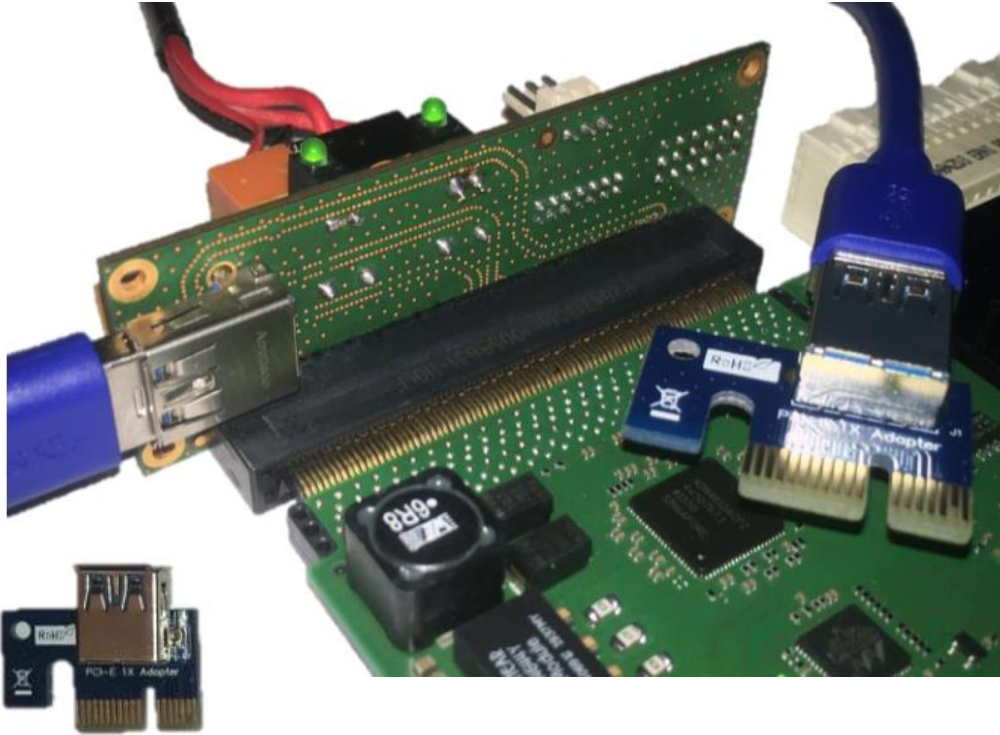
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Engineer 1: Michael Fenner
Engineer 2: Johannes Zink

DESY

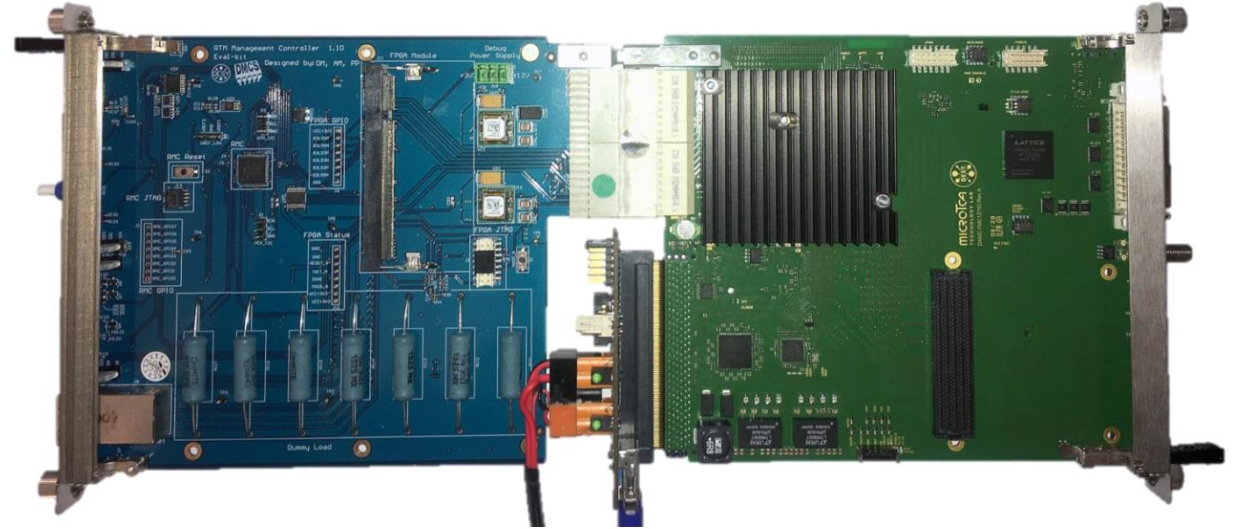
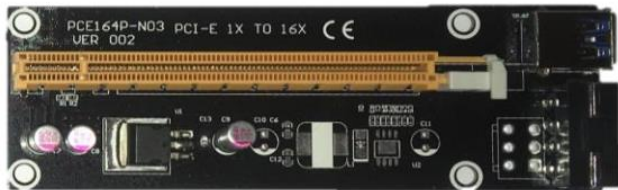
Rev: 0.3
Size: A3
Sheet:
4 of 4

MicroTCA Bring-up adapter



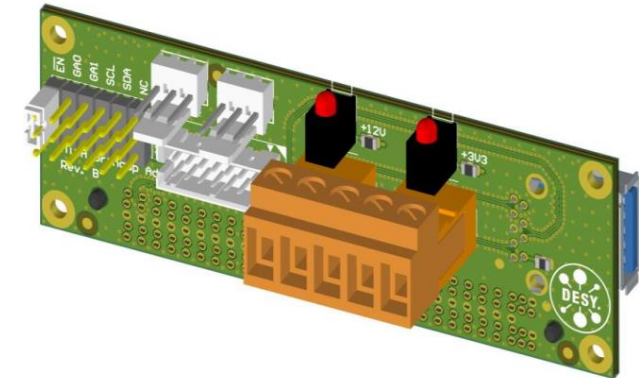
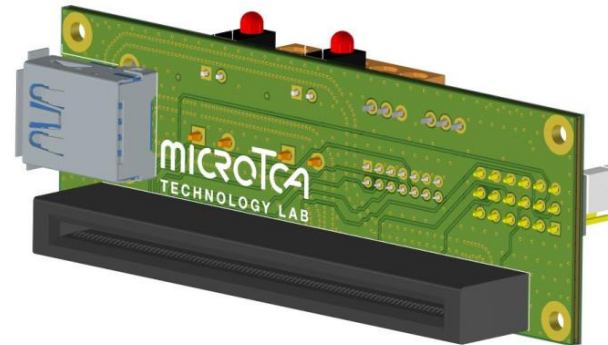
Laboratory bringup tool

DESY provides production files for free

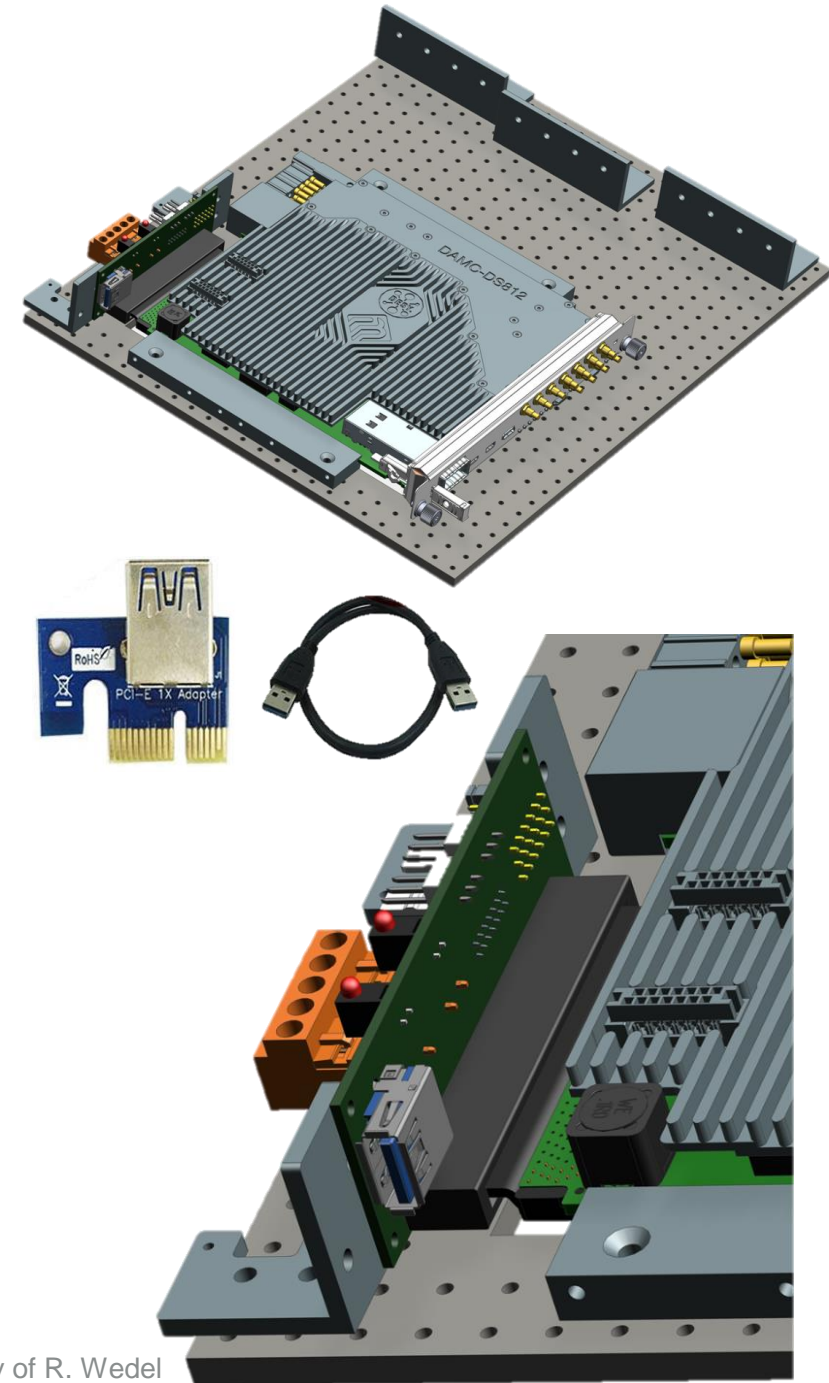
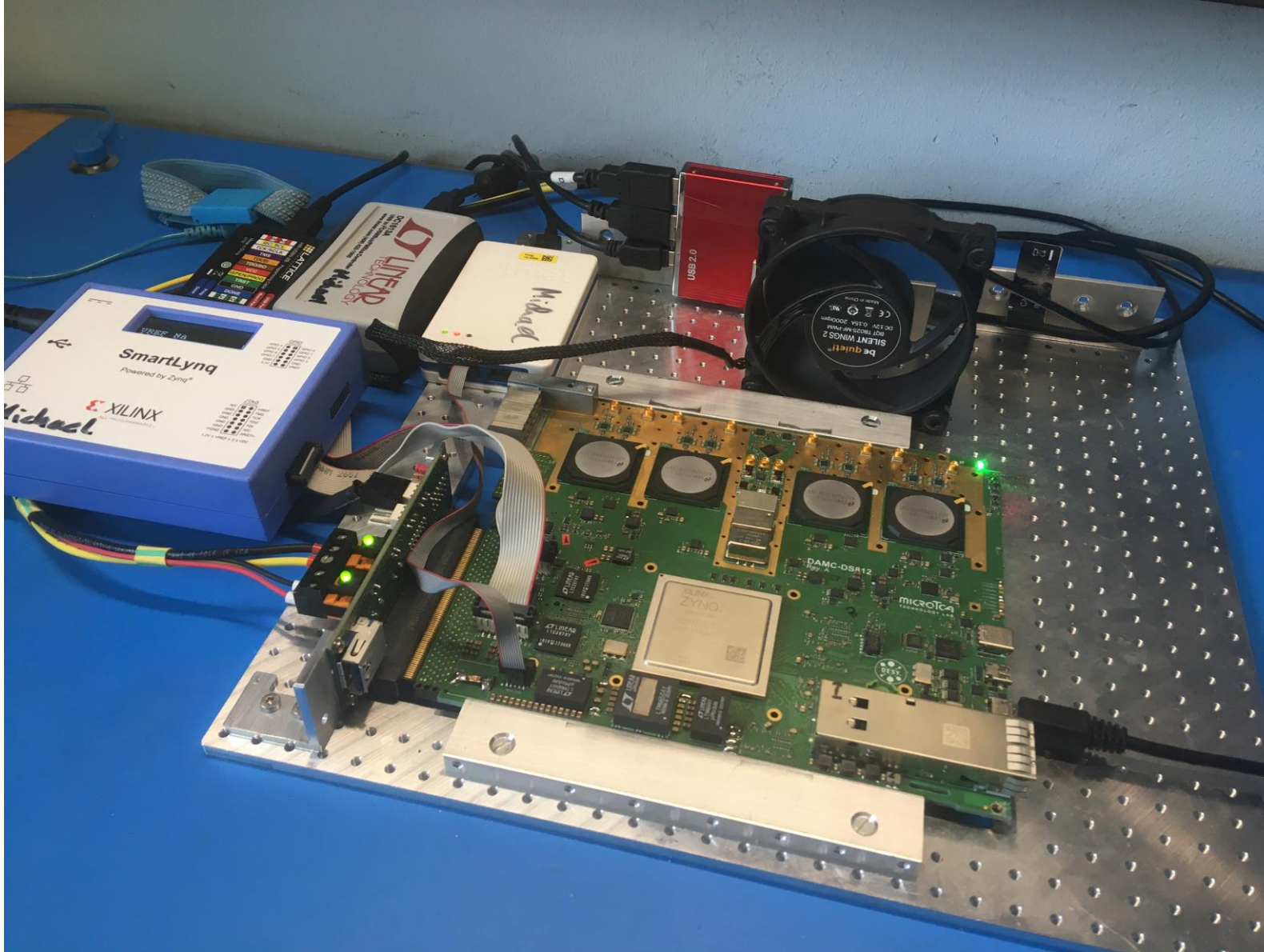


Top view

Bottom view



MicroTCA Bring-up adapter



Thank you!

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Kontakt

DESY. Deutsches
Elektronen-Synchrotron

www.desy.de

Michael Fenner
MSK
michael.fenner@desy.de
+49 (0) 40-8998-1885