Latest Hardware Developments in MicroTCA.4

Michael Fenner, Johannes Zink, Jan Marjanović, Nikola Radaković

Hamburg, 9. November 2021

HELMHOLTZ SPITZENFORSCHUNG FÜR GROSSE HERAUSFORDERUNGEN

DESY.

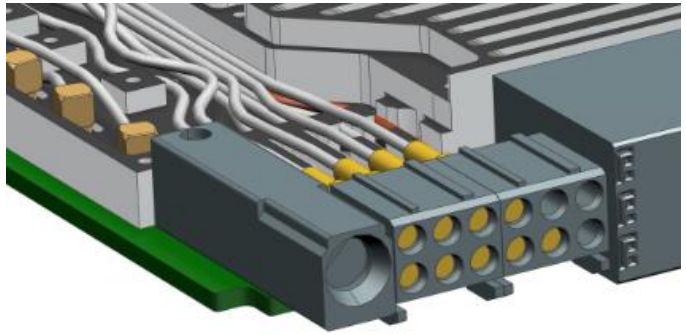
Topics

- **DAMC-DS812ZUP**
- **MicroTCA.4 Motion Controller**
- **DAMC-BPMZUP**
- **Support tools available to the community**

DAMC-DS812ZUP

DAMC-DS812ZUP – 8-Channel RF Low-Latency Digitizer

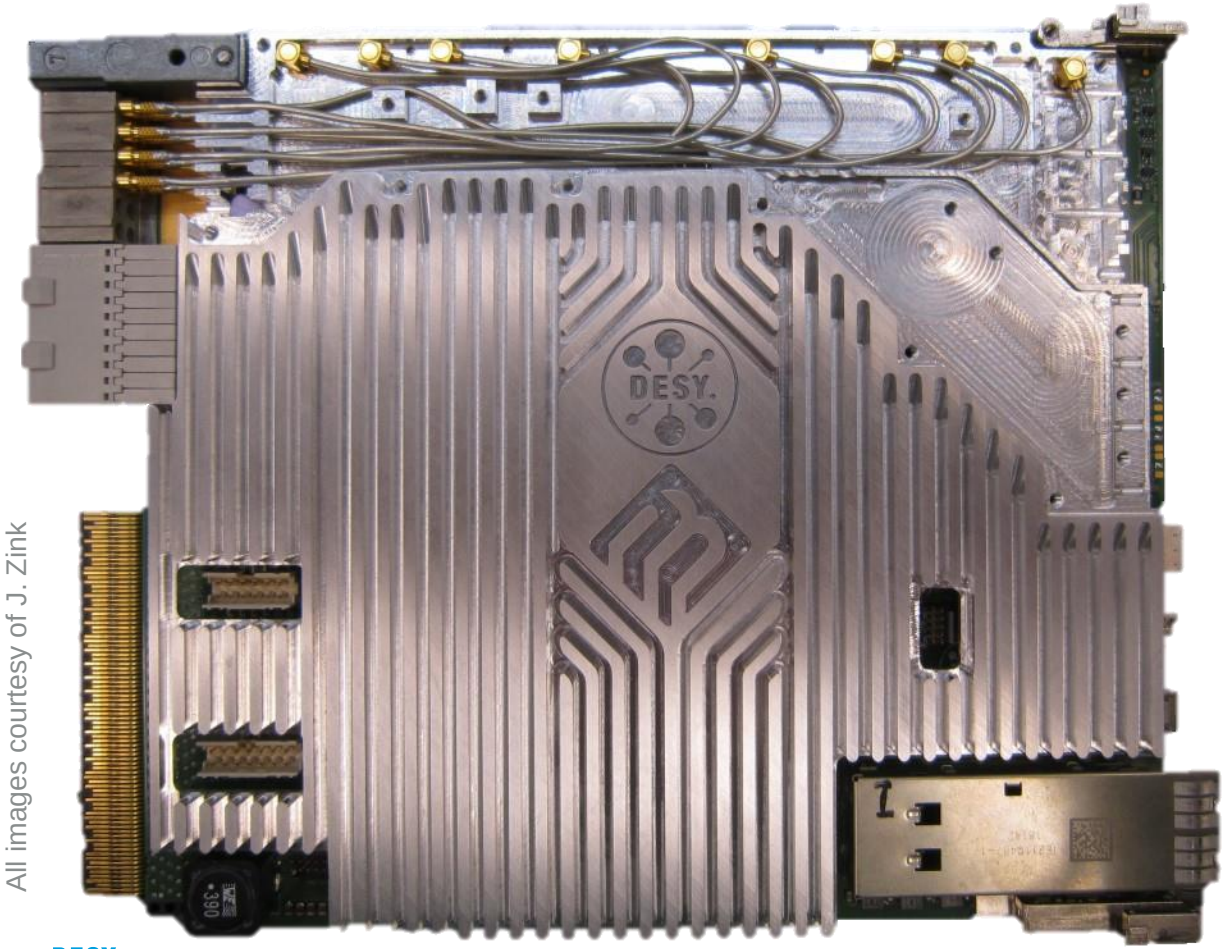
- **First Board that uses analog Zone 3 RF Class**
- 2.7GHz input BW, 12 bits, 8-channels
- Amplifier bandwidth: 4.8 GHz
- 50ns end-to-end latency
- **Uses coaxial semi-rigid cables for transmission**
- RF input from front panel or RTM
- 800 MSPS / 1600 MSPS
- On-board PLL: 14fs jitter
- PCIe Gen. 3 x4 or x8 connectivity
- QSFP+ support (4x10G)
- Stand-Alone Mode (with USB-C alternate mode)
- State-of-the-art high-level language support

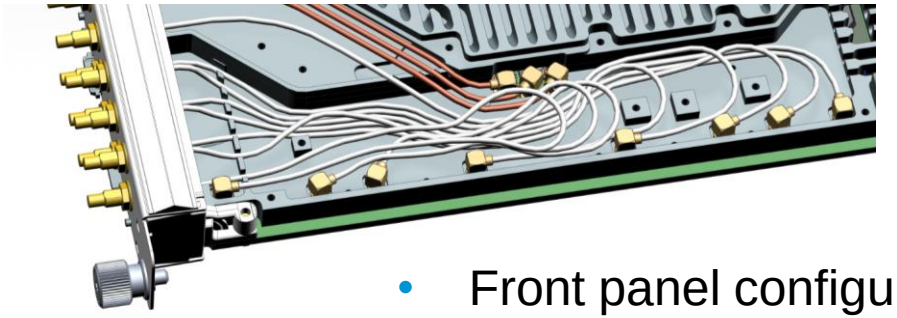


courtesy of J. Zink

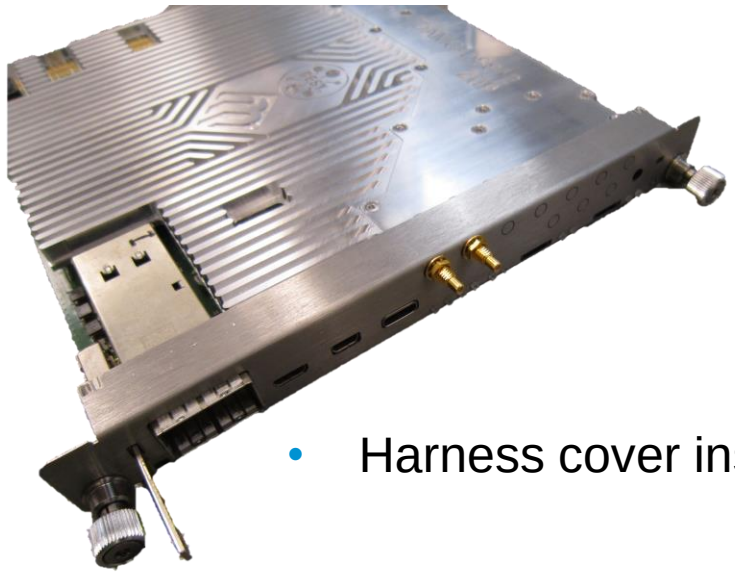
DAMC-DS812ZUP – Coaxial Harness

- Coaxial cables offer excellent RF performance
- Usage of harness allows front input / rear input configuration
- Zone3 RF class specification (based on Radiall Coaxipak 2) is available to the community





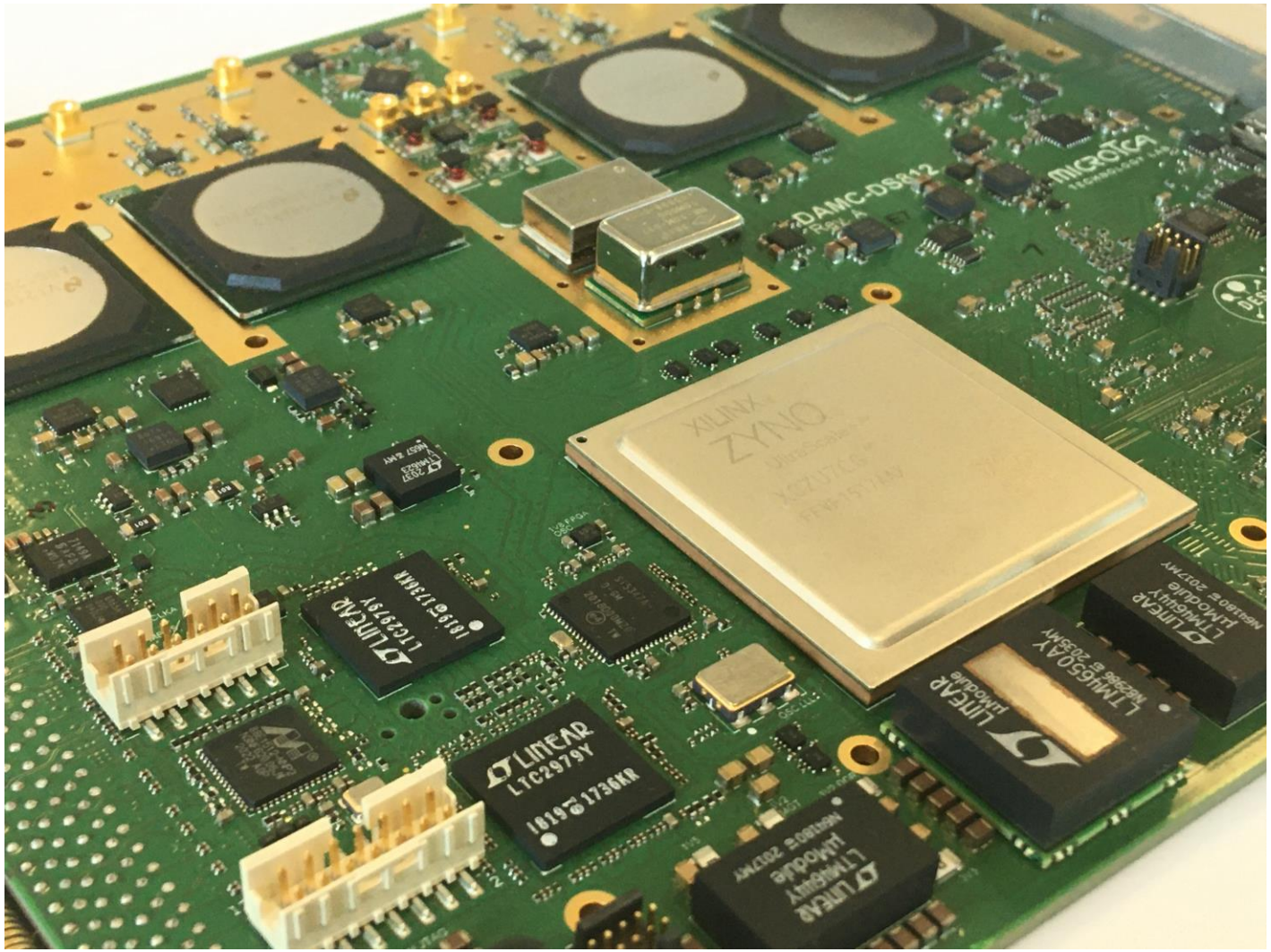
- Front panel configuration



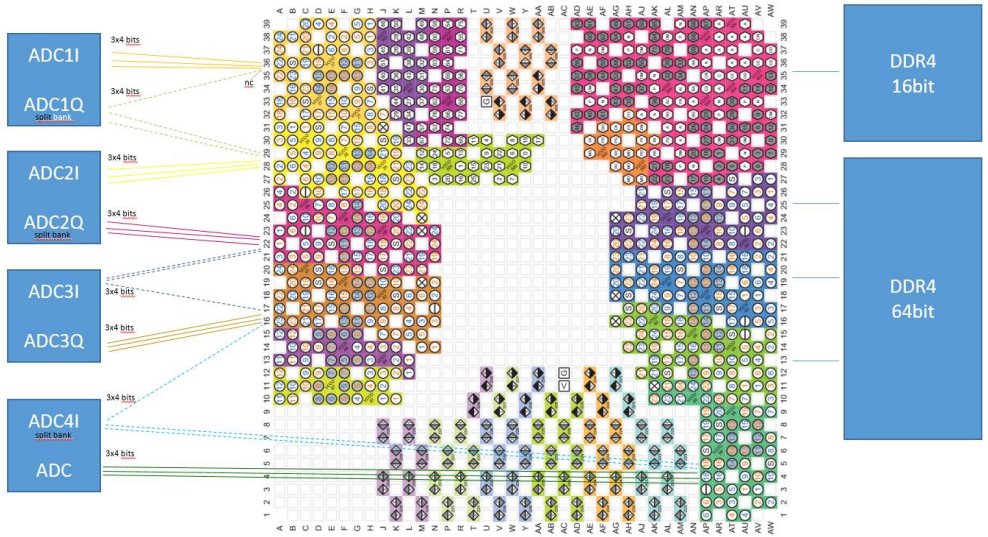
- Harness cover installed

All images courtesy of J. Zink

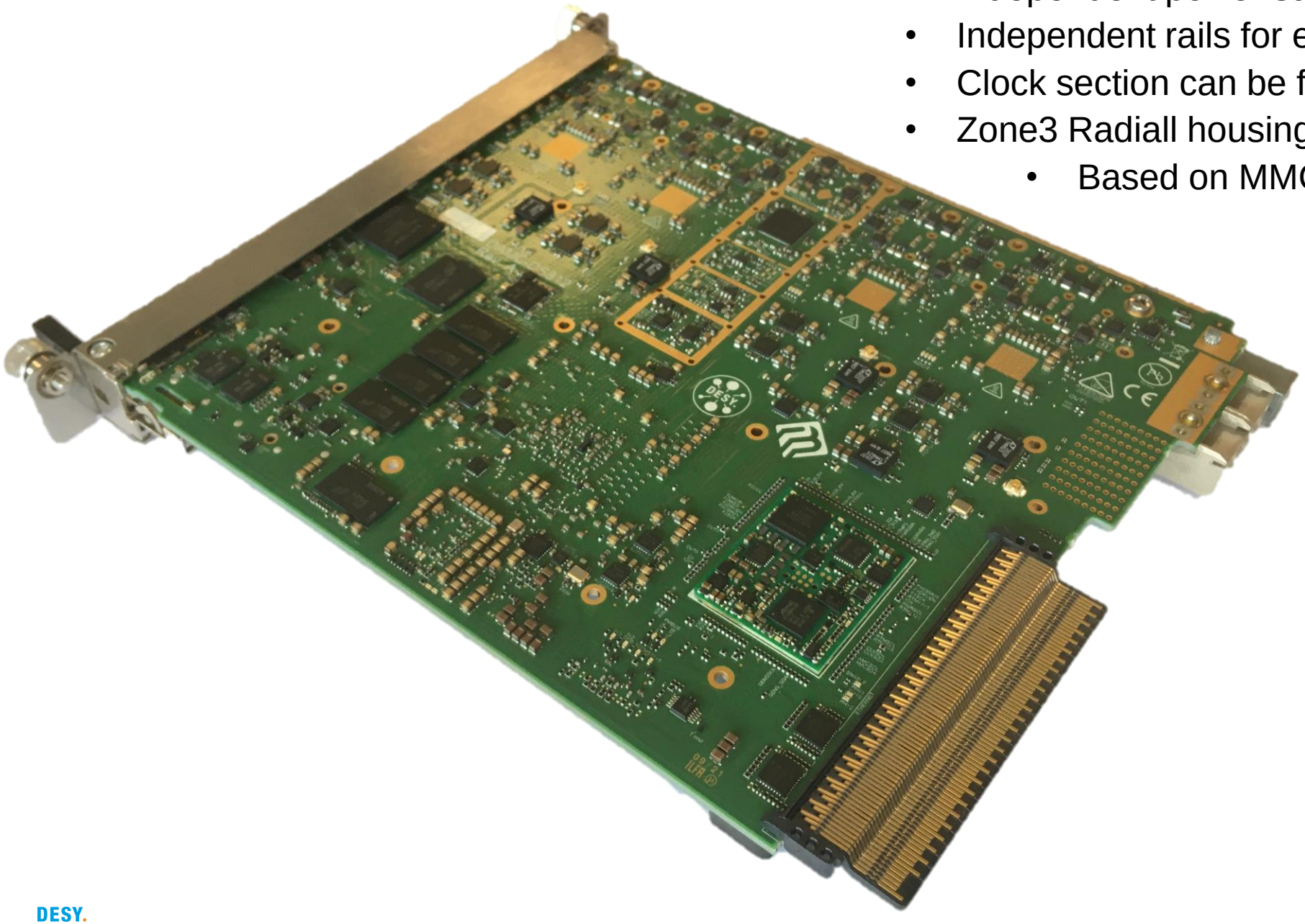
Based on Zynq Ultrascale+ MPSoC



- Most dense board developed in MSK group
- 4289 components down to 0201 size
- 16-Layer HDI stack-up
- Takes full advantage of the Ultrascale+ capabilities (bank assignment trick)

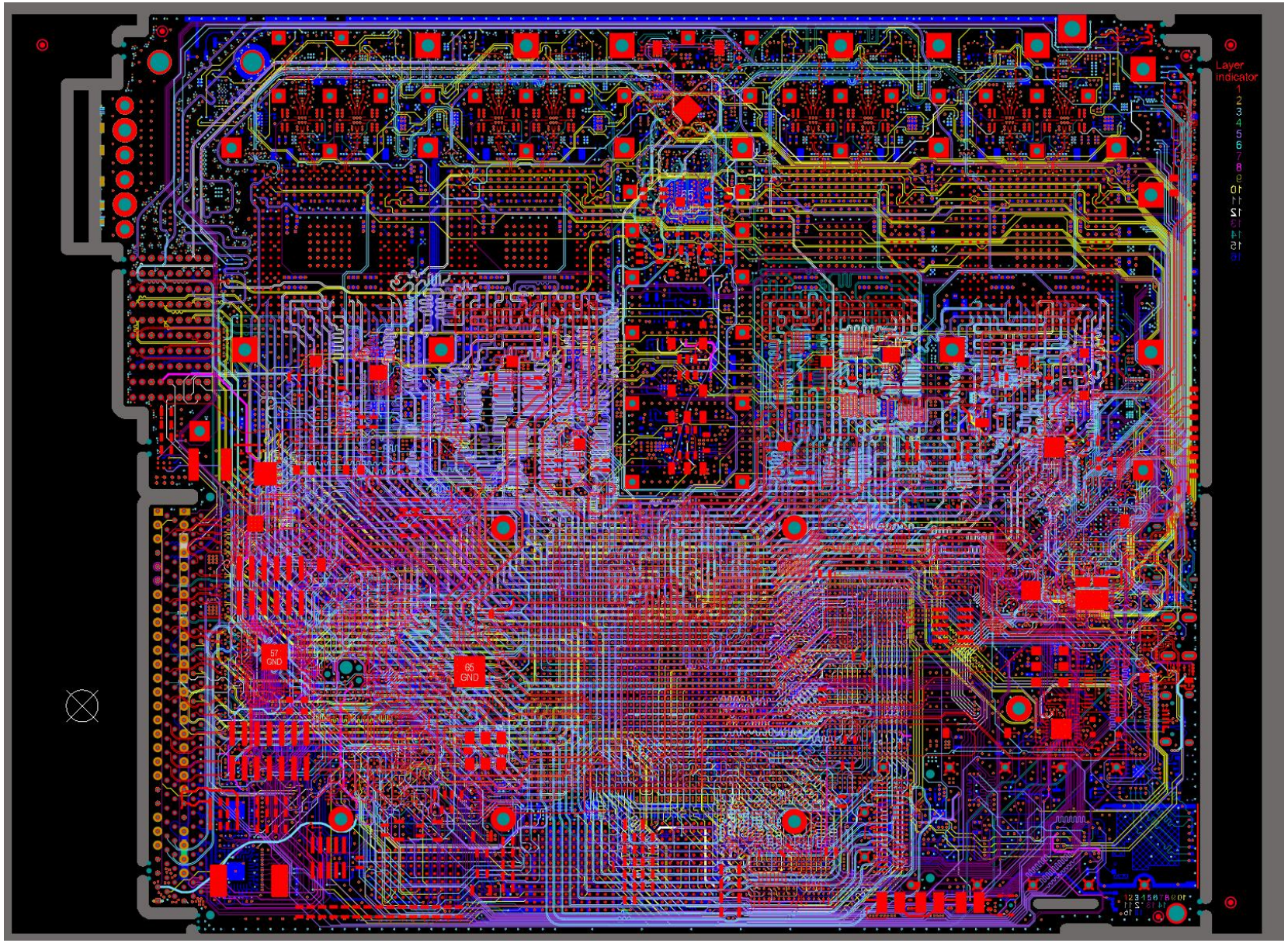


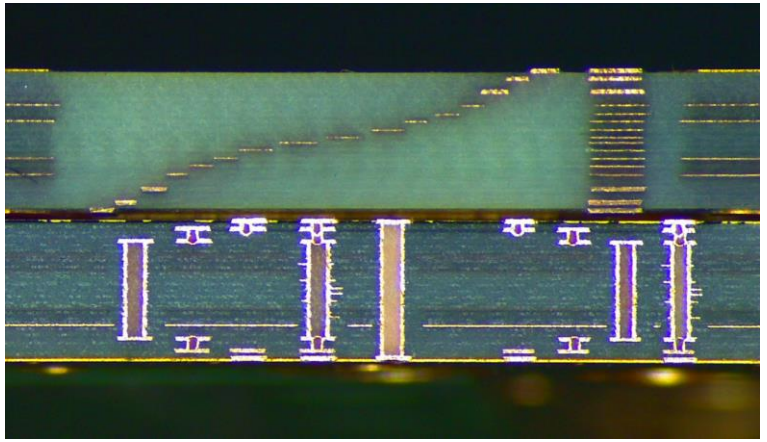
DAMC-DS812ZUP – bottom side



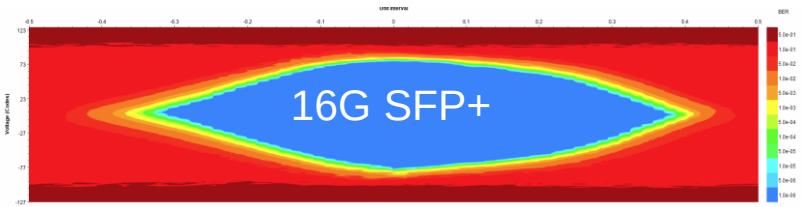
- Independent power supplies for digital/analog part
- Independent rails for each ADC channel
- Clock section can be fully shielded from both sides
- Zone3 Radiall housing is metalized and soldered
  - Based on MMC Stamp

DAMC-DS812ZUP Layout details



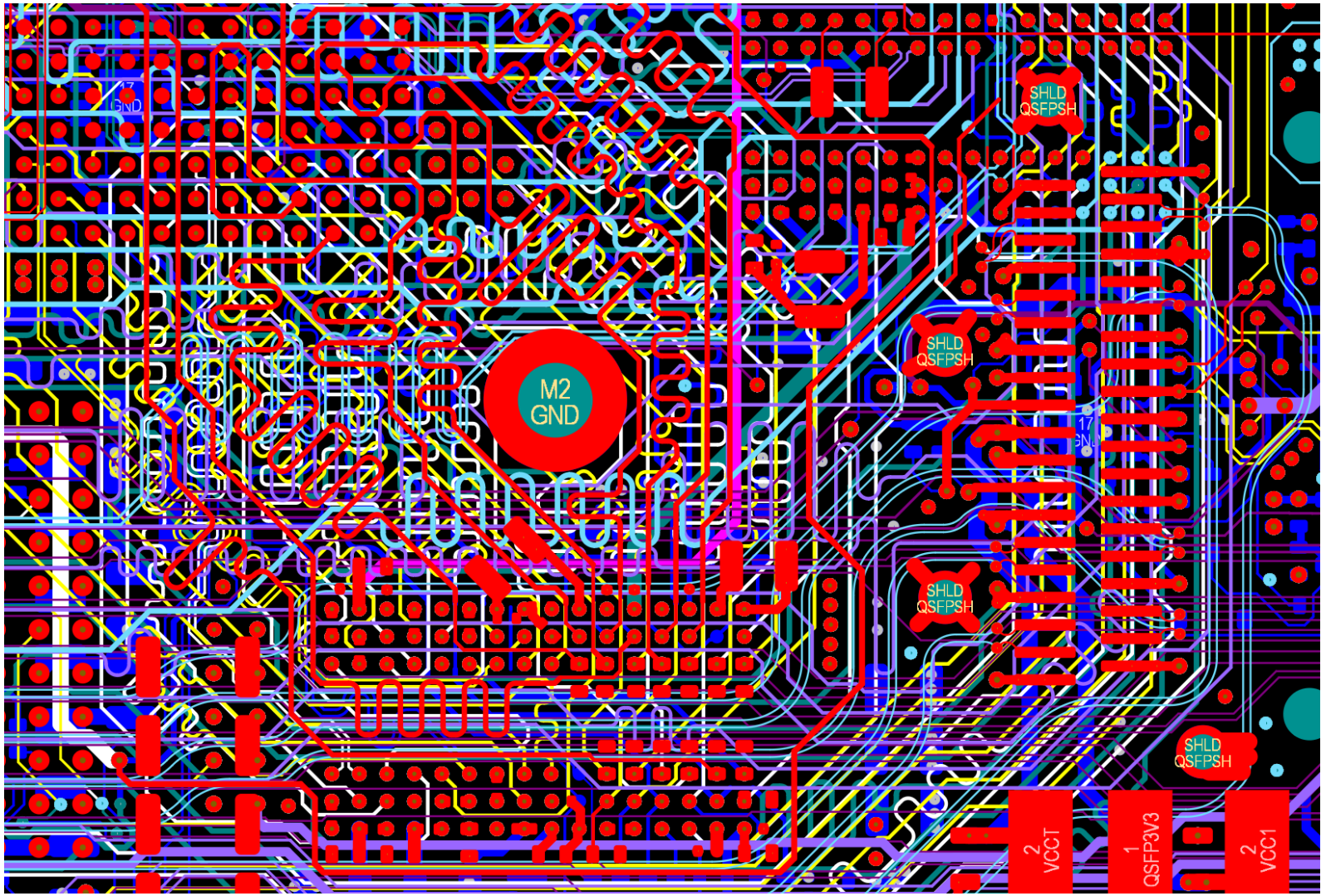


courtesy of J. Zink

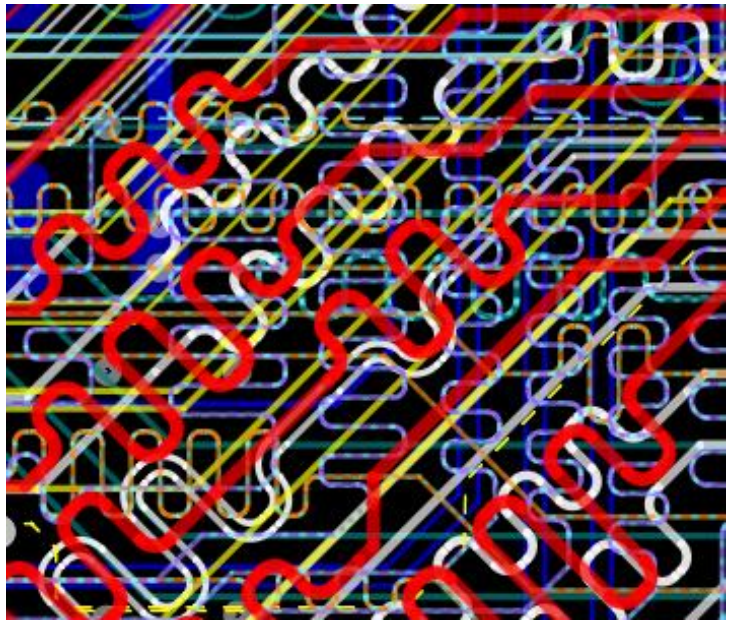


- Stack-up allows high density
- Less dependency between upper/lower sections
- Perfect signal integrity

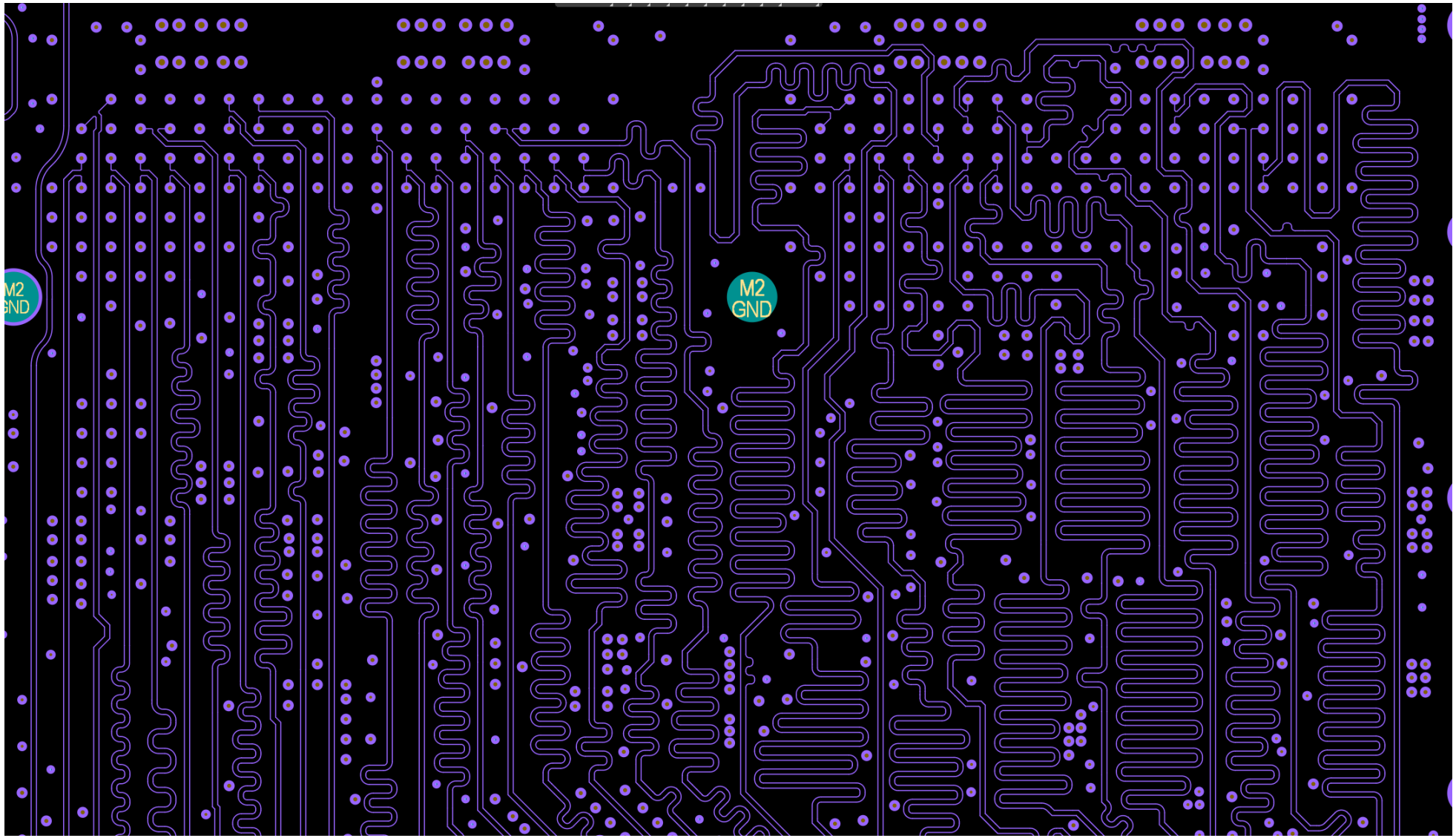
DAMC-DS812ZUP Layout details



- Zooming-in reveals complexity
- almost impossible to layout
- (many tricks used)

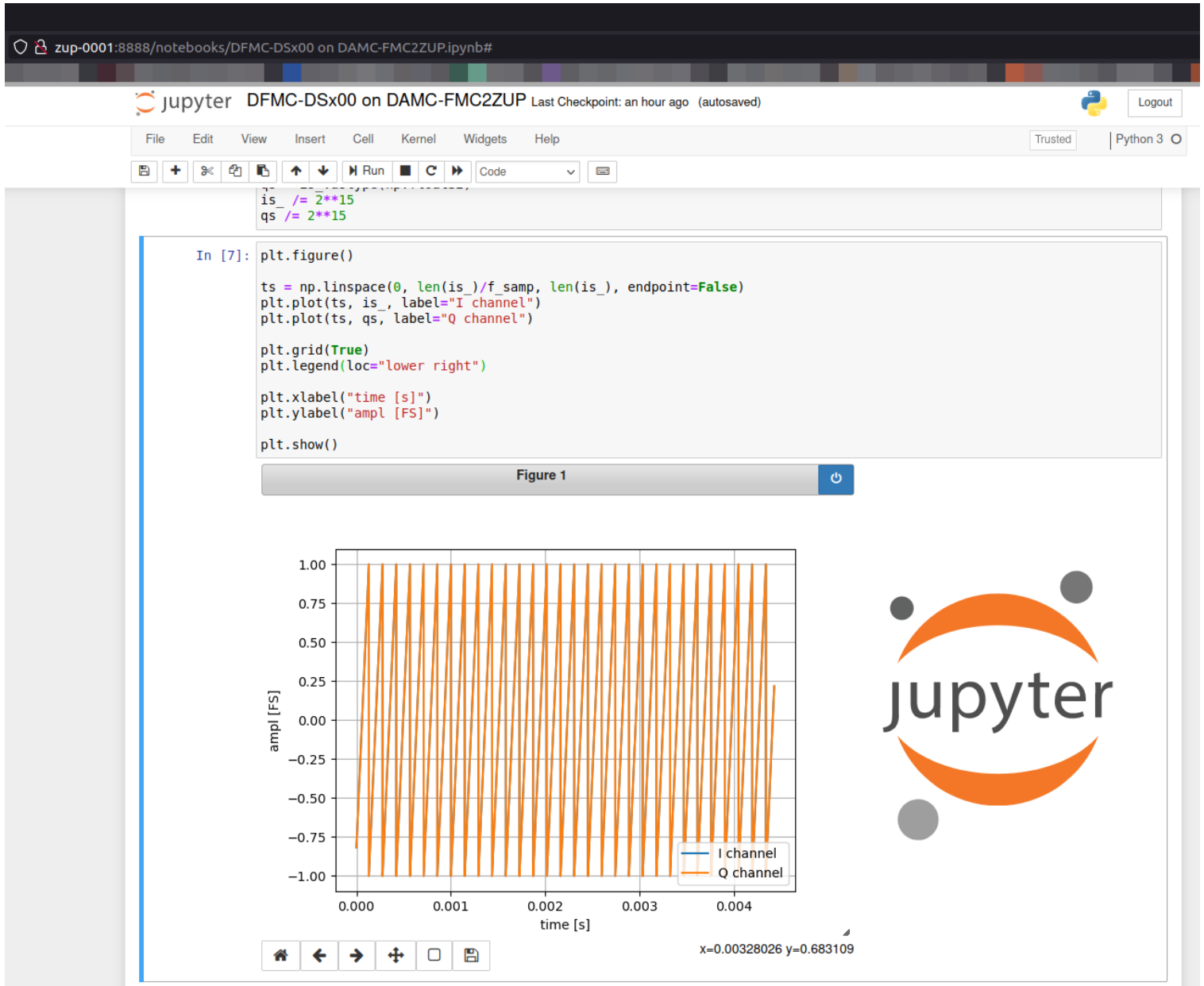


DAMC-DS812ZUP Layout details

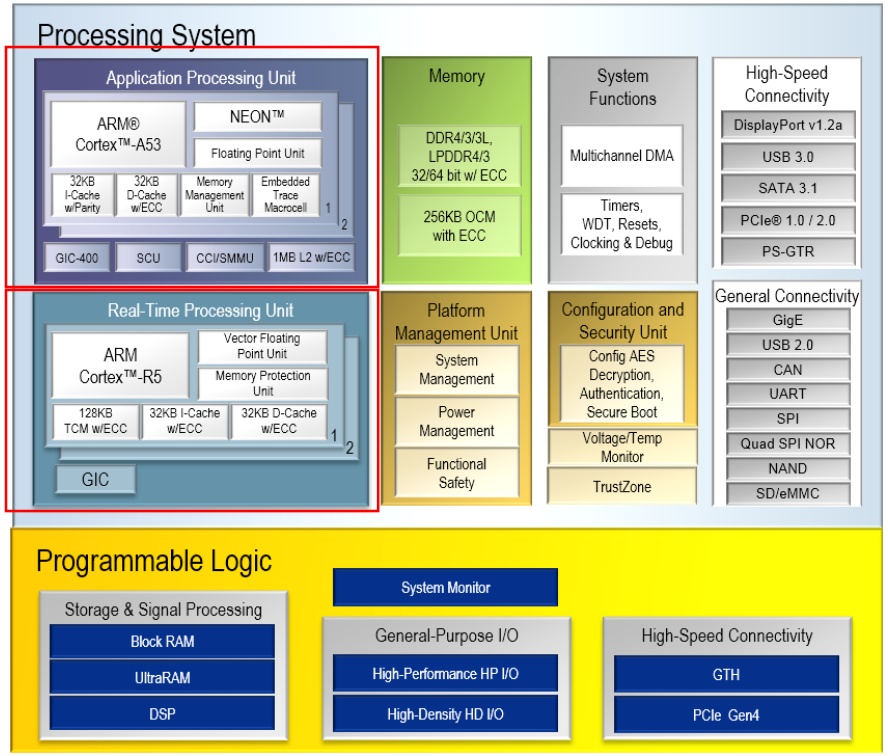


- All ADCs channels are length-matched
- Length match was difficult to achieve for center ADCs

DAMC-DS812ZUP – MPSoC provides new Approach

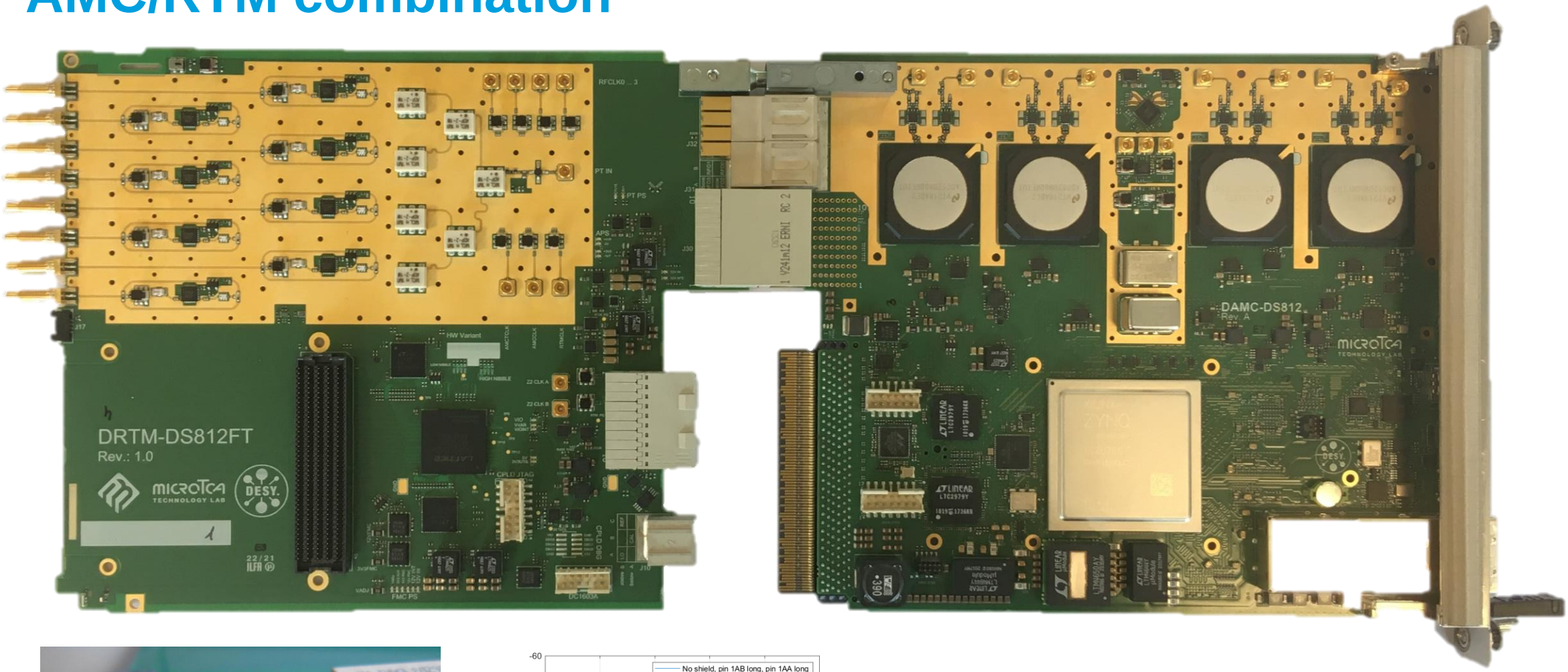


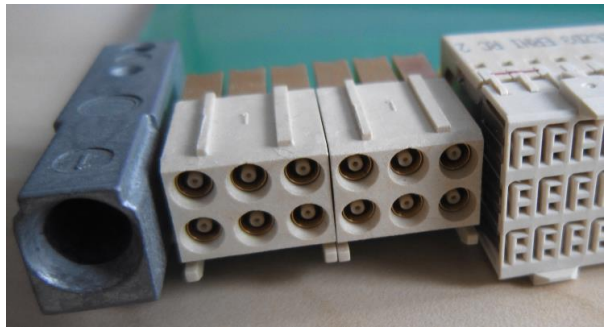
- Board can run “fully self-contained”
- Interface via web-server
- Instant data-taking using Jupyer Notebook
- Python libraries available
- Uses RPU for bare-metal low-level housekeeping (HW configuration)

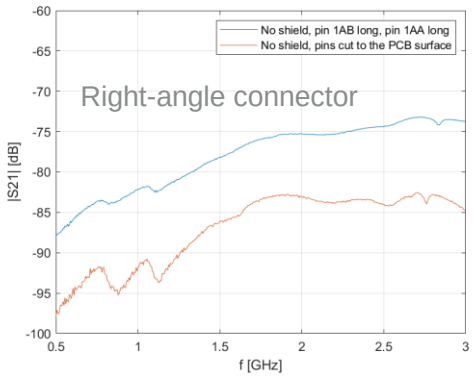


courtesy of J. Marjanović

AMC/RTM combination



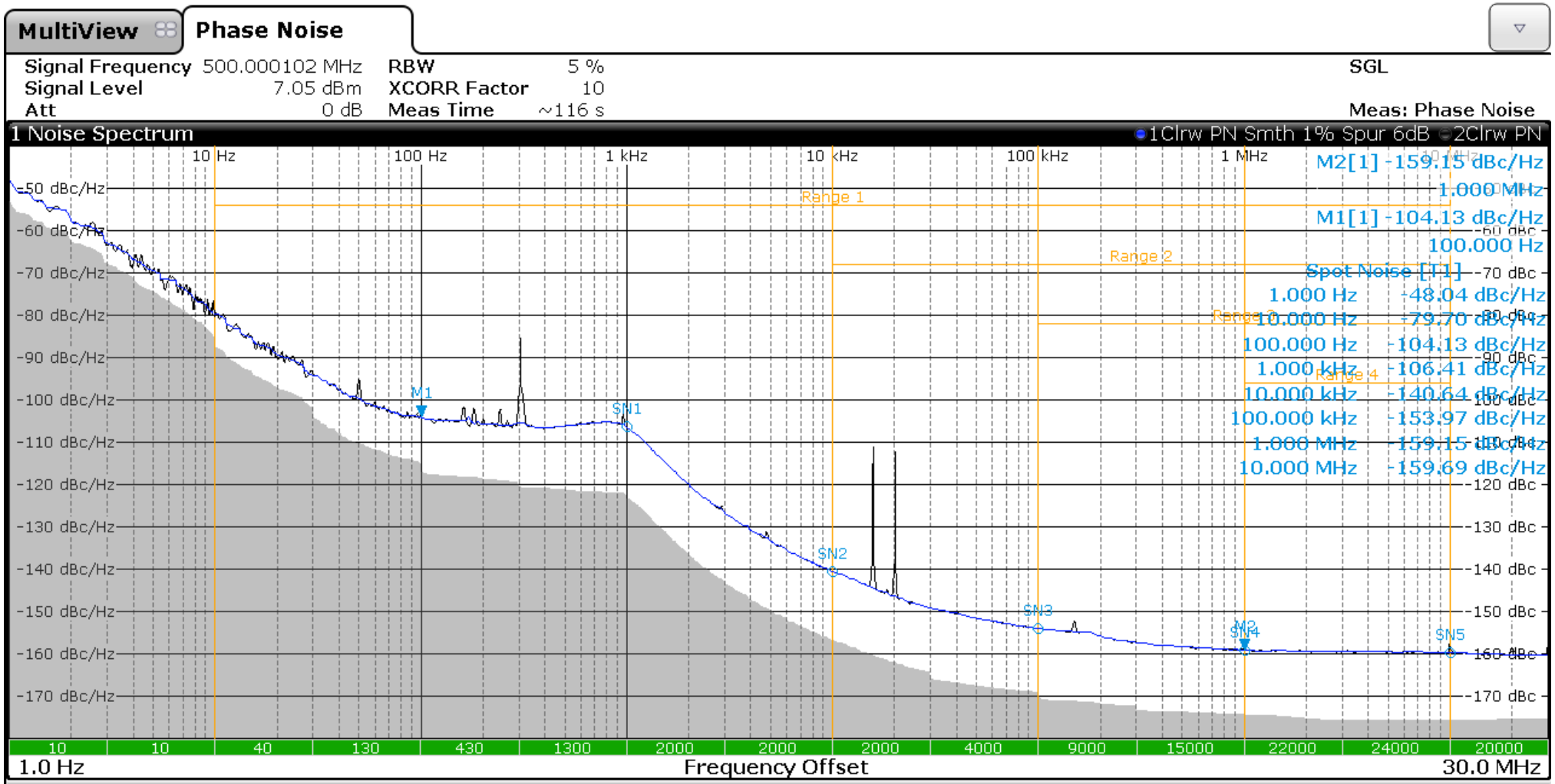




- Feed-Through RTM is available
- AMC: cables / RTM: right-angle connector
- Shielding between channels better than -85dB

courtesy of J. Zink

On-Board Clock Performance



2 Integrated Measurements

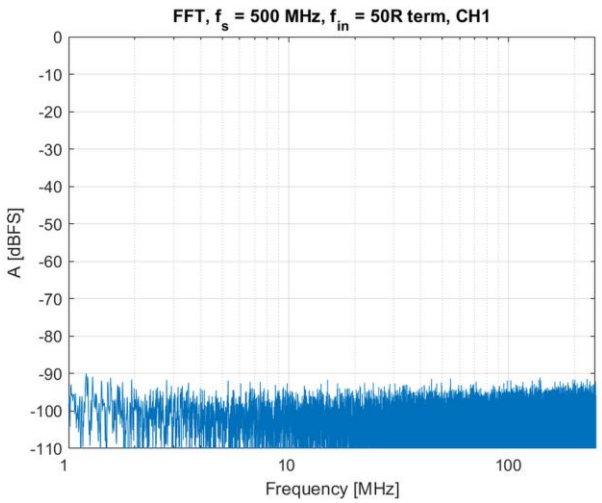
Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	10.000 Hz	10.000 MHz		-70.71 dBc	23.61 m°/412.09 µrad	269.885 Hz	131.173 fs
2	1	10.000 kHz	10.000 MHz		-88.99 dBc	2.88 m°/50.23 µrad	269.885 Hz	15.988 fs
3	1	100.000 kHz	10.000 MHz		-89.37 dBc	2.76 m°/48.09 µrad	269.884 Hz	15.308 fs
4	1	1.000 MHz	10.000 MHz		-89.99 dBc	2.57 m°/44.79 µrad	269.717 Hz	14.257 fs

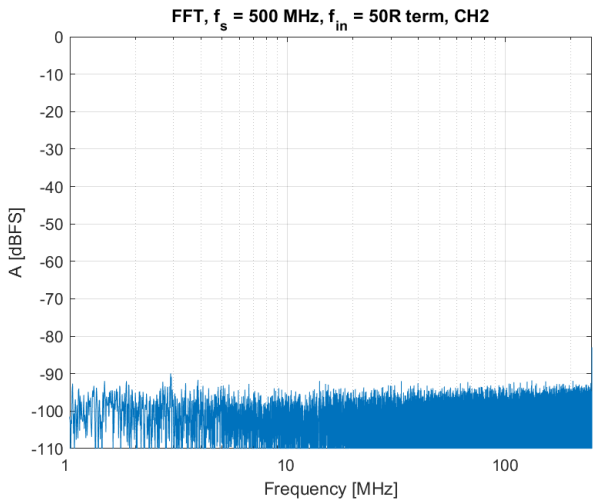
- On-board OCXO, PLL, clock fanout
- Achieves 14.25fs Jitter (at 500 MHz)

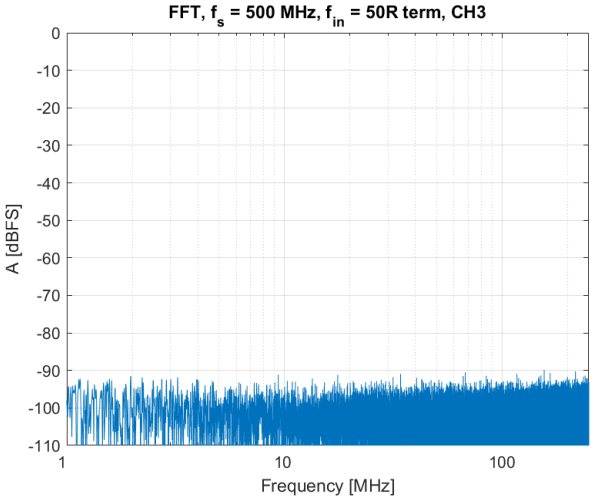
courtesy of J. Zink

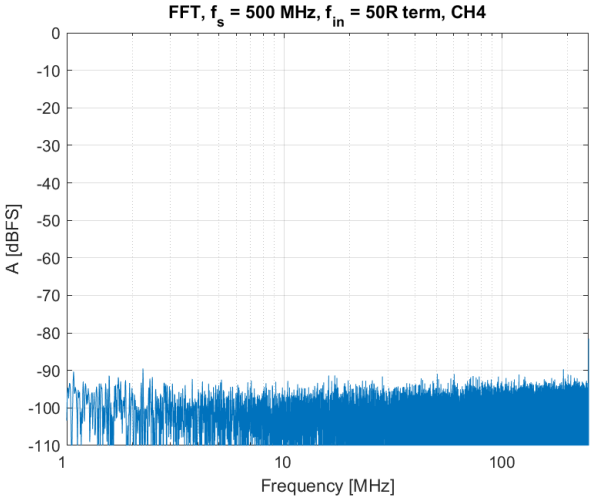
Direct Sampling RF performance

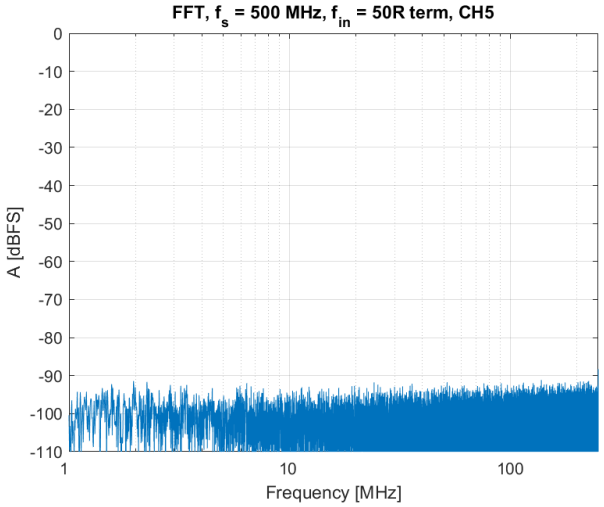
- Investigations ongoing
- Excellent direct sampling performance

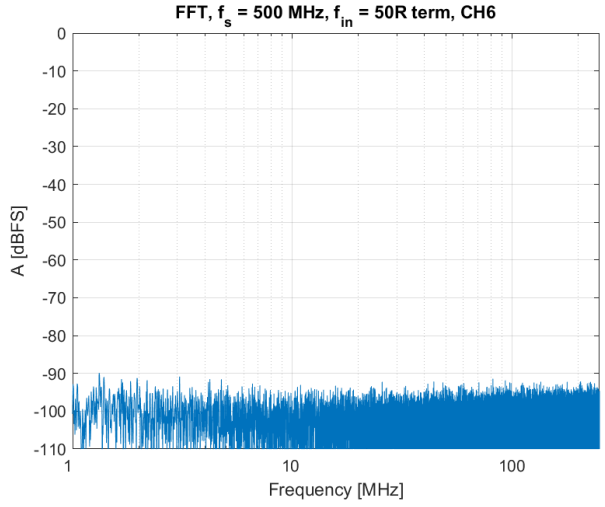


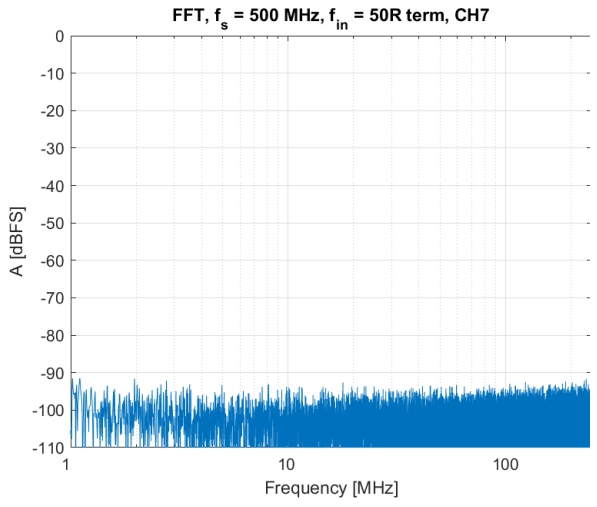


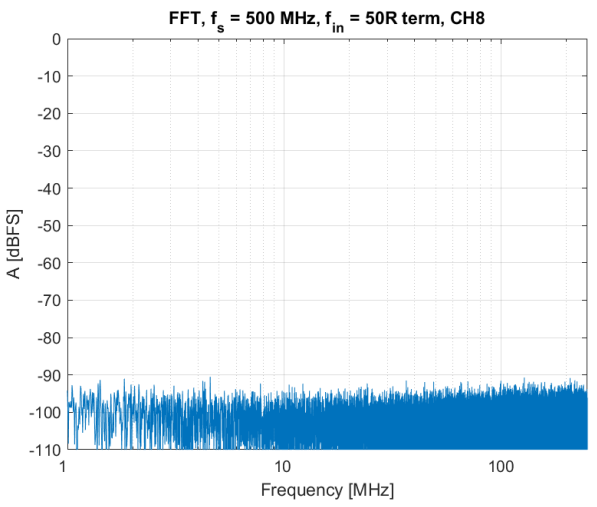










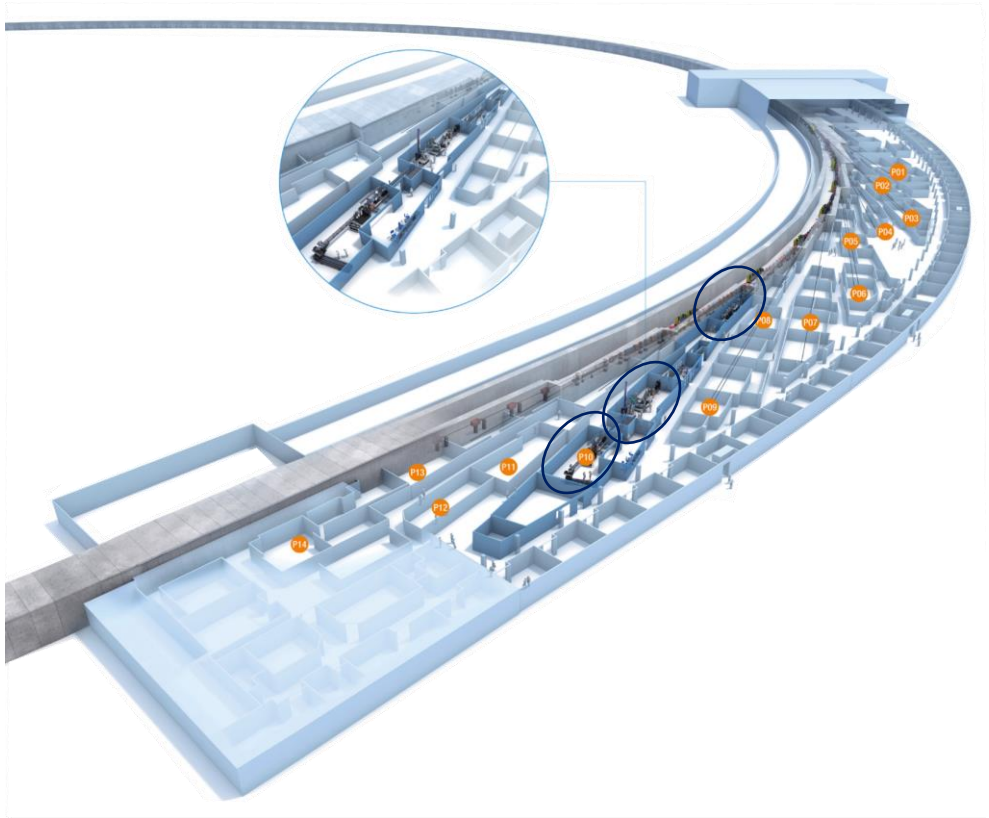


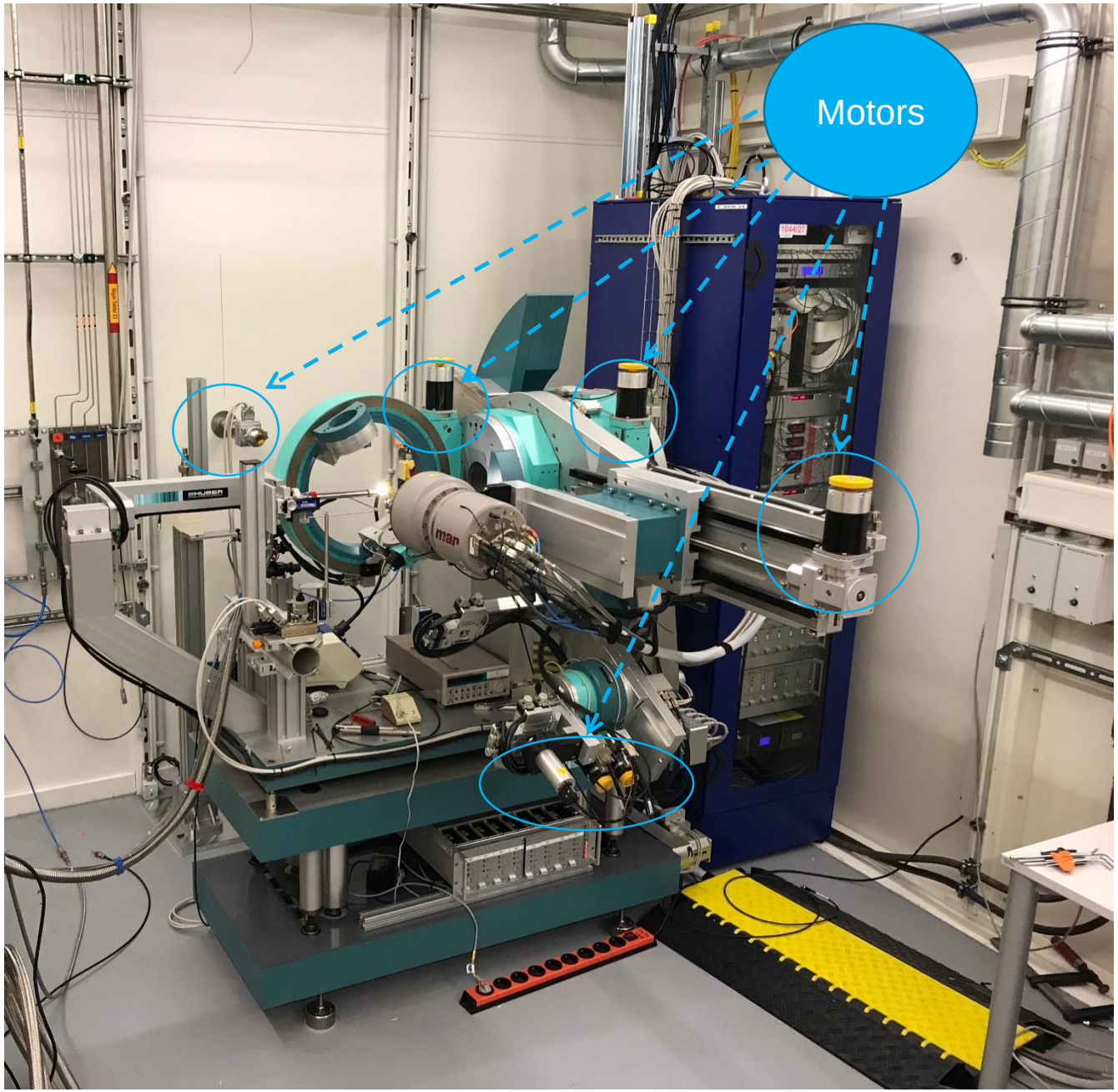
All images courtesy of J. Zink

MicroTCA.4 Motion Controller

MicroTCA Motion Controller

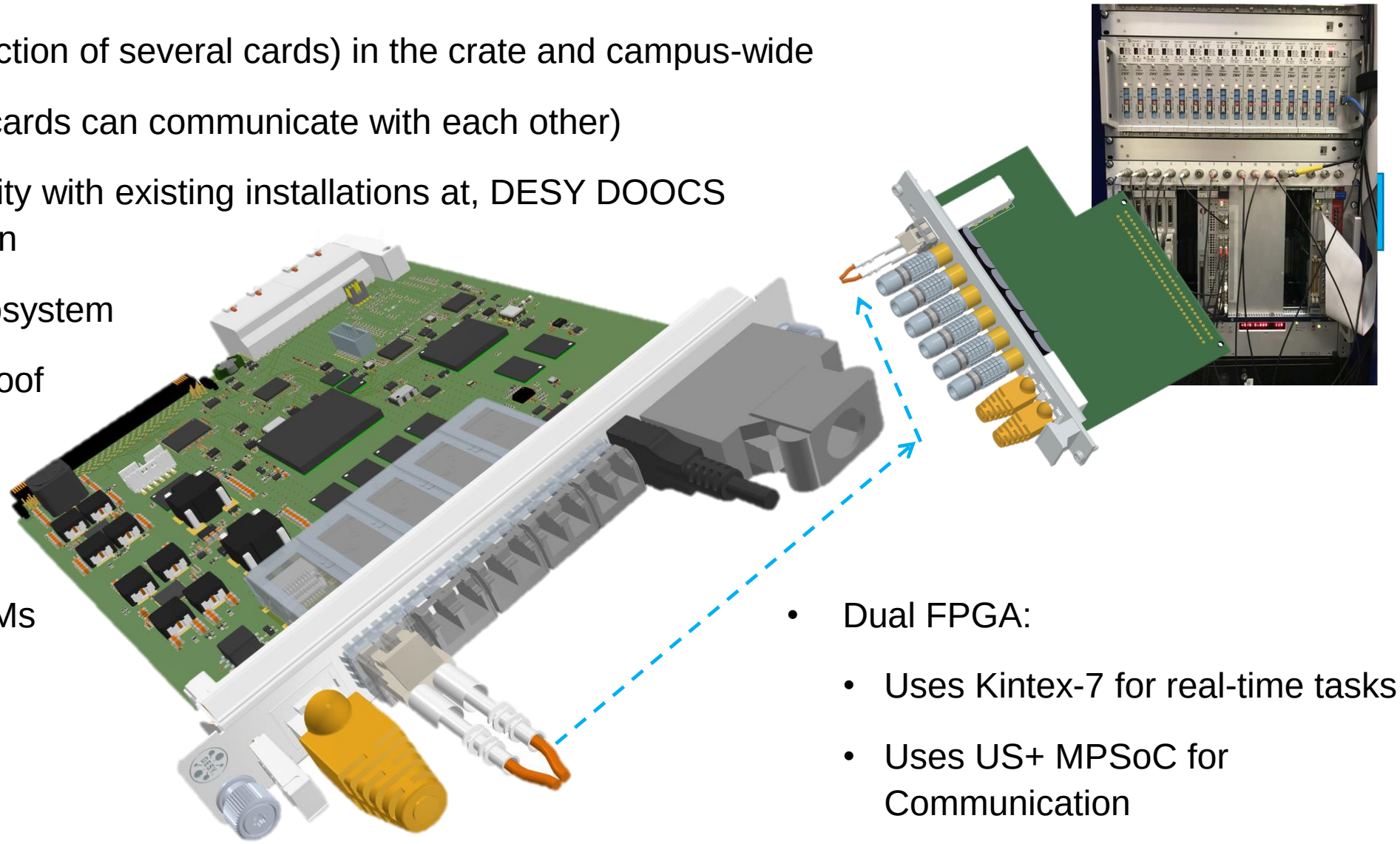
- We need to move motors in experiments
- Existing solution not suited for new installations
- We decided to develop a motion controller card





The new MTCA.4 Motion Controller Card

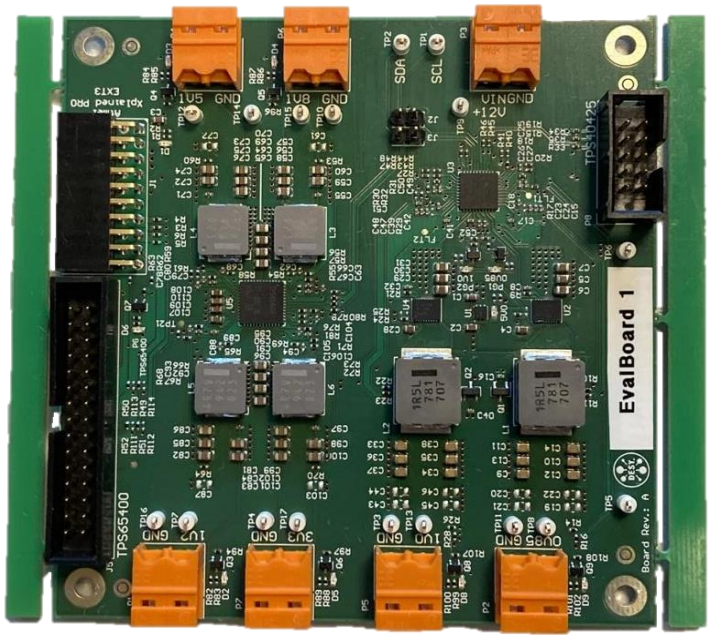
- Can control 16 motors / axes per board
- Scalable (interconnection of several cards) in the crate and campus-wide
- Support of triggers (cards can communicate with each other)
- Backward compatibility with existing installations at, DESY DOOCS and Tango connection
- Integration in the ecosystem
- Based on a future-proof standard
- Significantly less rigid cables
- Expandable with RTMs



- Dual FPGA:
  - Uses Kintex-7 for real-time tasks
  - Uses US+ MPSoC for Communication

Cost-Optimization

- Two FPGAs with small pin count (no FMC support)
- components shared with DAMC-FMC2ZUP, DAMC-Z7IO and DAMC-DS812
- Omission of White-rabbit, bi-directional clock cross point switch, etc.
- Application-specific clocking
- Optimized **power system**




```
CHAN  DEVICE     VOLTAGE   PGOOD  FAULTS
3V3   TPS65400   NaN       PG_ERR OTH OFF
1V8   TPS65400   NaN       PG_ERR OTH OFF
1V5   TPS65400   NaN       PG_ERR OTH OFF
1V2   TPS65400   NaN       PG_ERR OTH OFF
0V85  TPS40425   0.014 V   PG_OK  OFF
1V0   TPS40425   0.000 V   PG_OK  OFF
Your board name> pu
Your board name> cf

CHAN  DEVICE     VOLTAGE   PGOOD  FAULTS
3V3   TPS65400   NaN       PG_OK
1V8   TPS65400   NaN       PG_OK
1V5   TPS65400   NaN       PG_OK
1V2   TPS65400   NaN       PG_OK
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Your board name> pd
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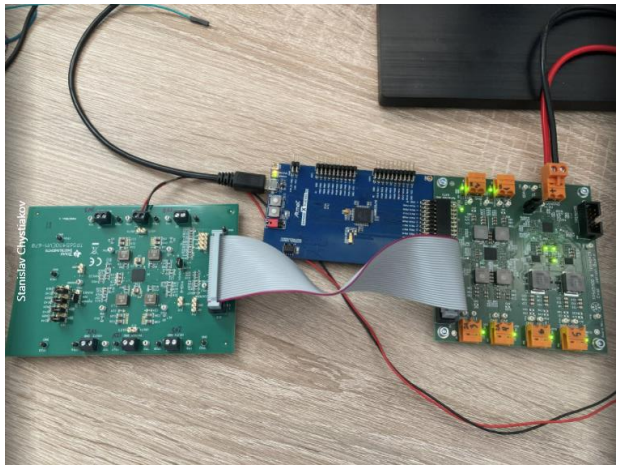
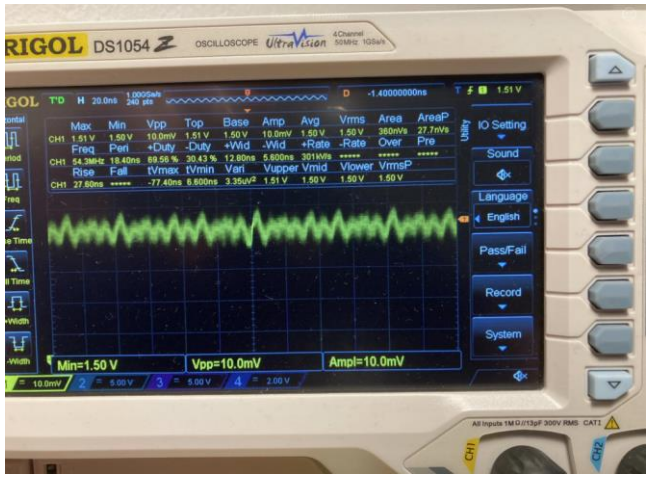
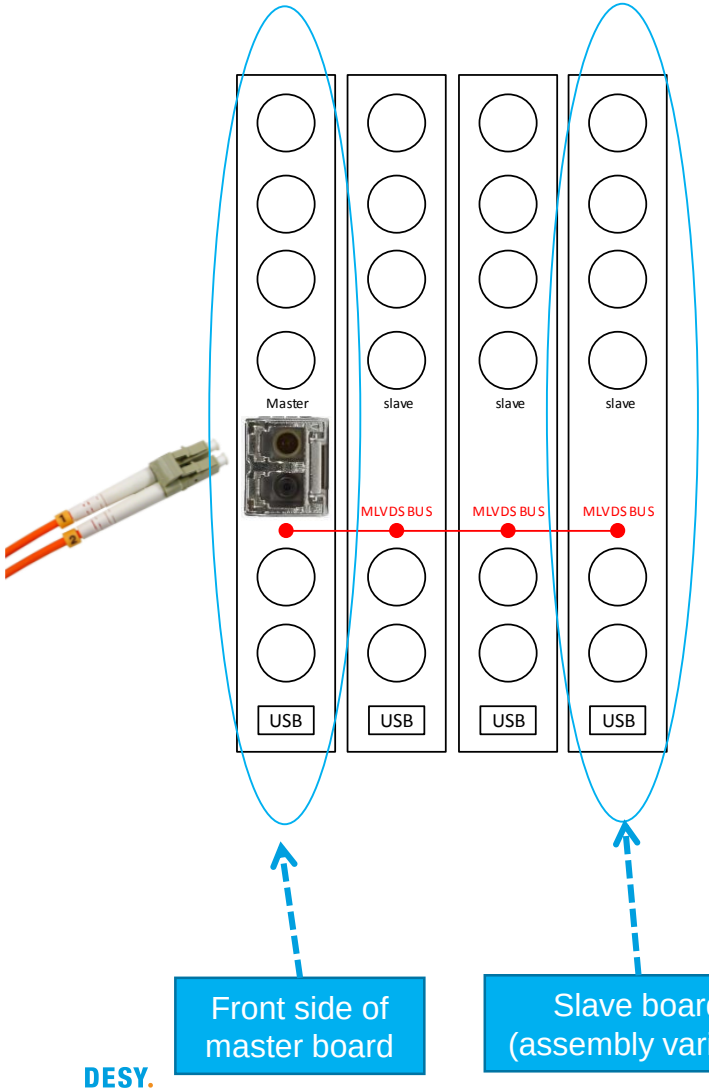


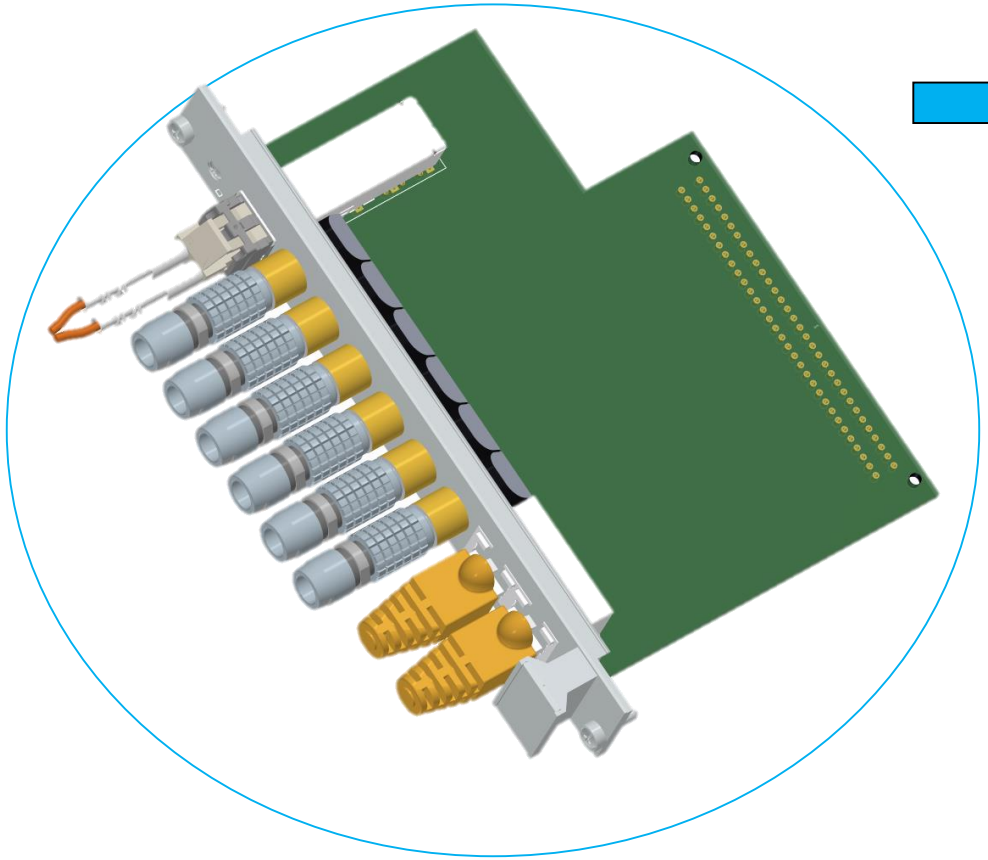


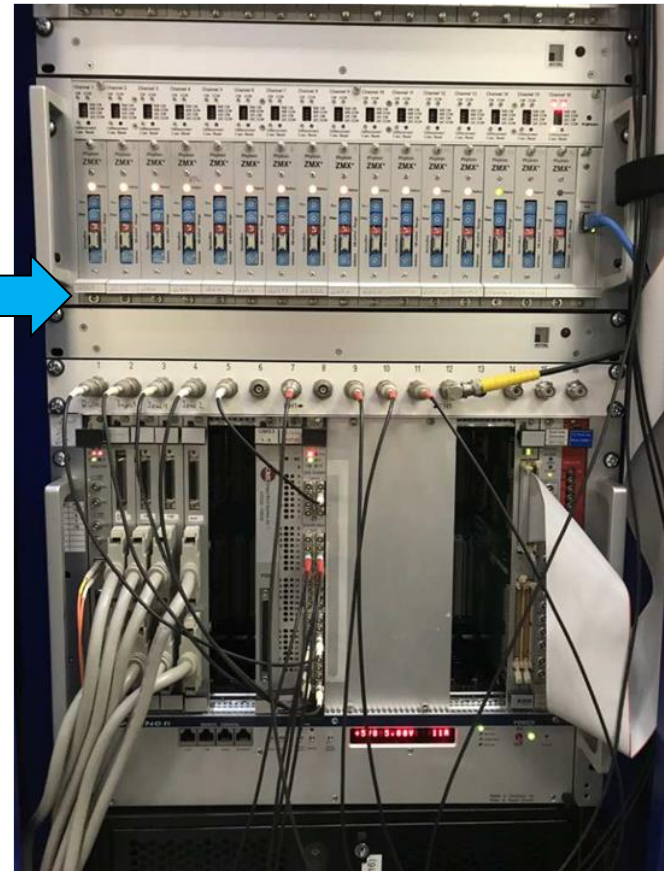
courtesy of S. Chystiakov

Fan-out board – backwards compatibility to existing motor drivers

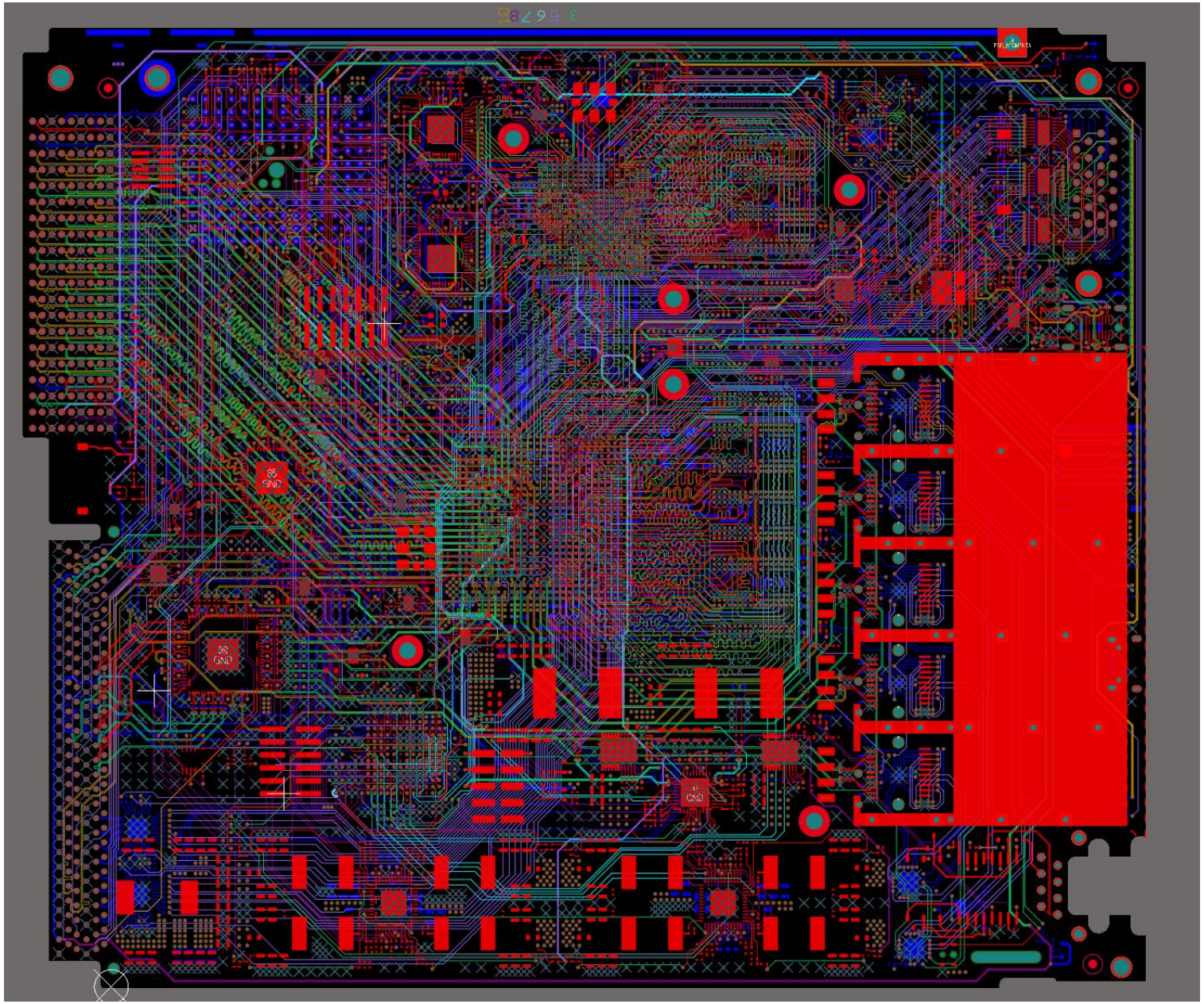
- Optical SFP+ Interface to STEP/DIR motor drivers – no SCSI cables anymore
- Encoder support (1 per axis)



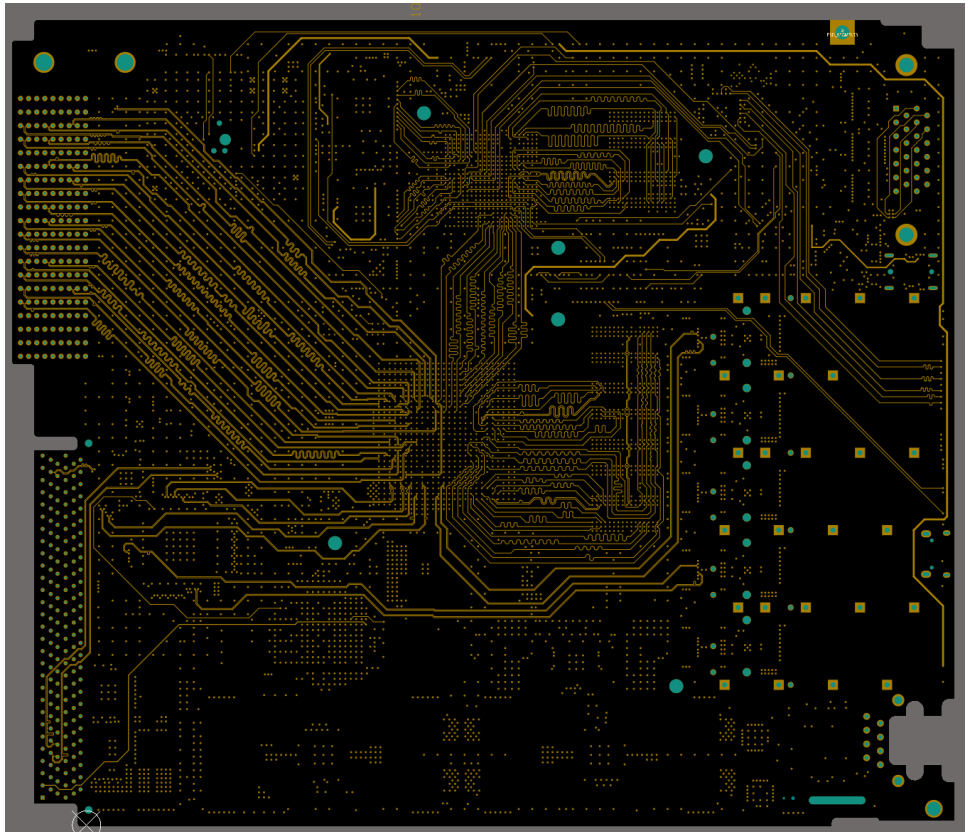




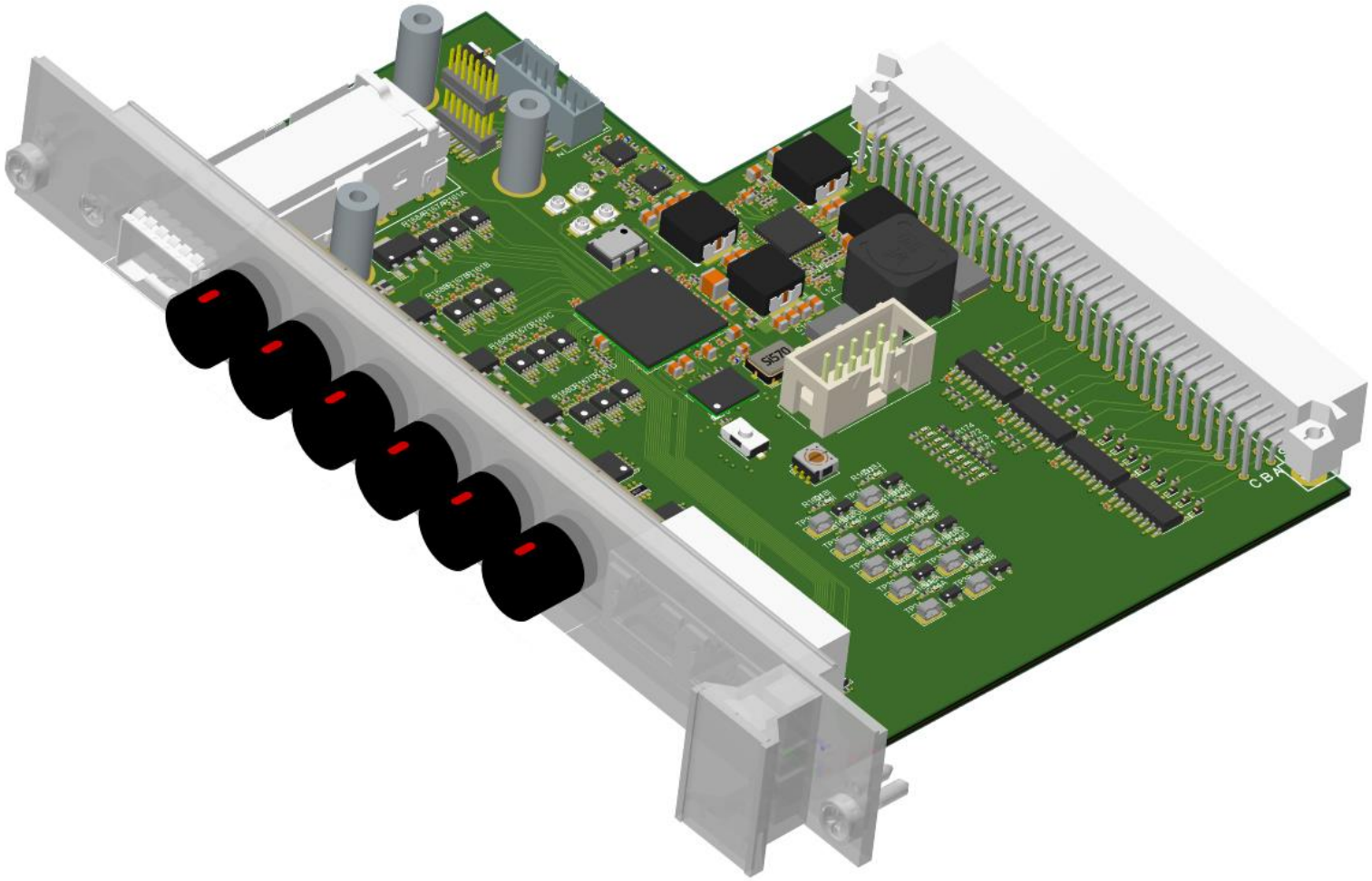
Current State of work: Motion controller

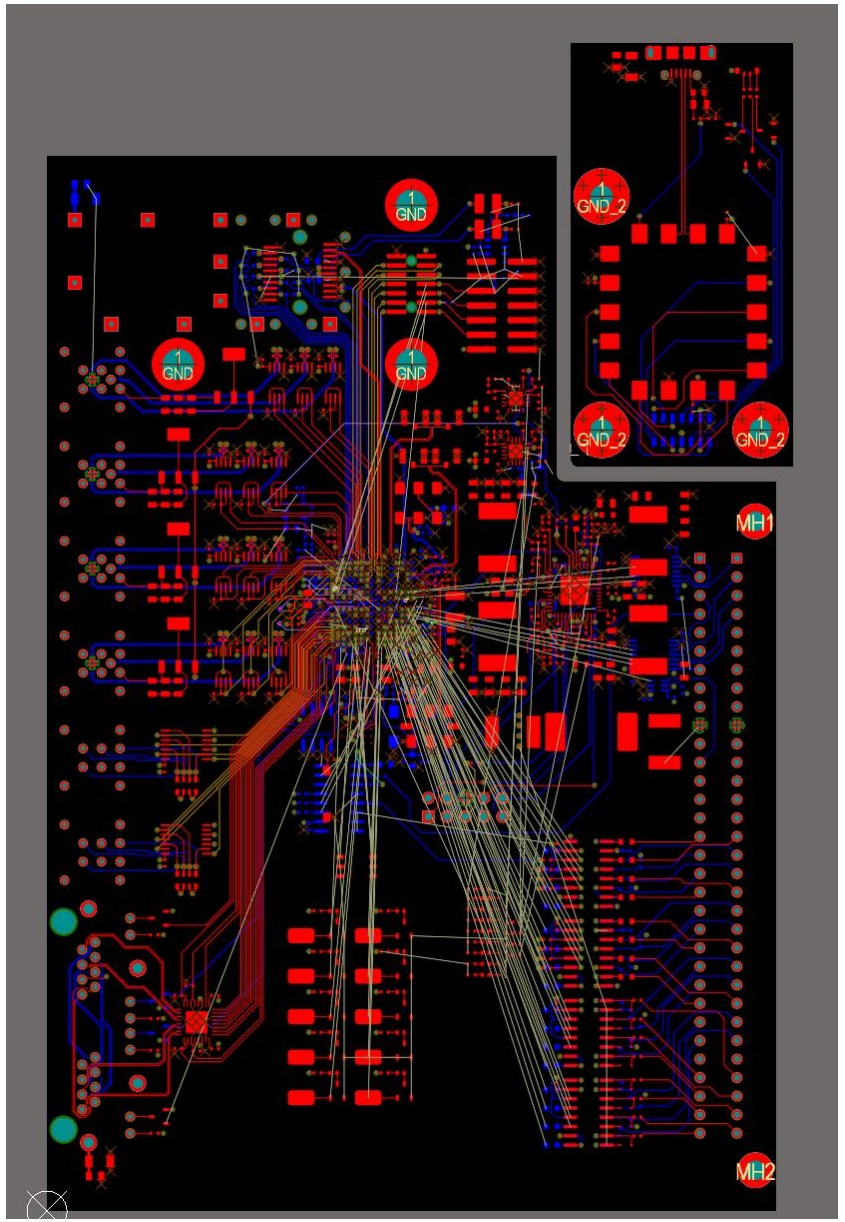


- Everything is fully routed and matched
- All components in house
- We are checking the desin



Current State of work: Fan-out Board



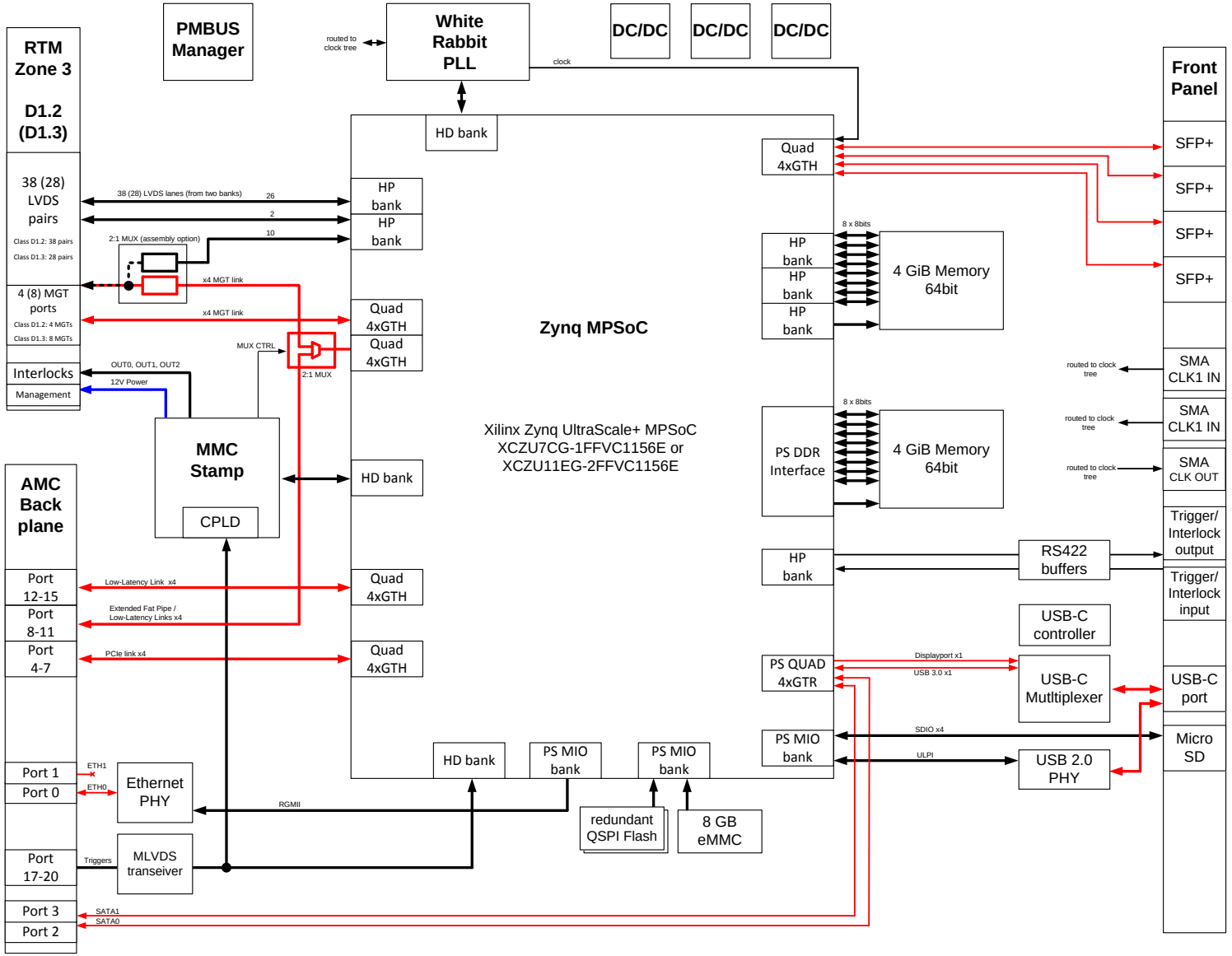


DAMC-BPMZUP

DAMC-BPMZUP - outlook

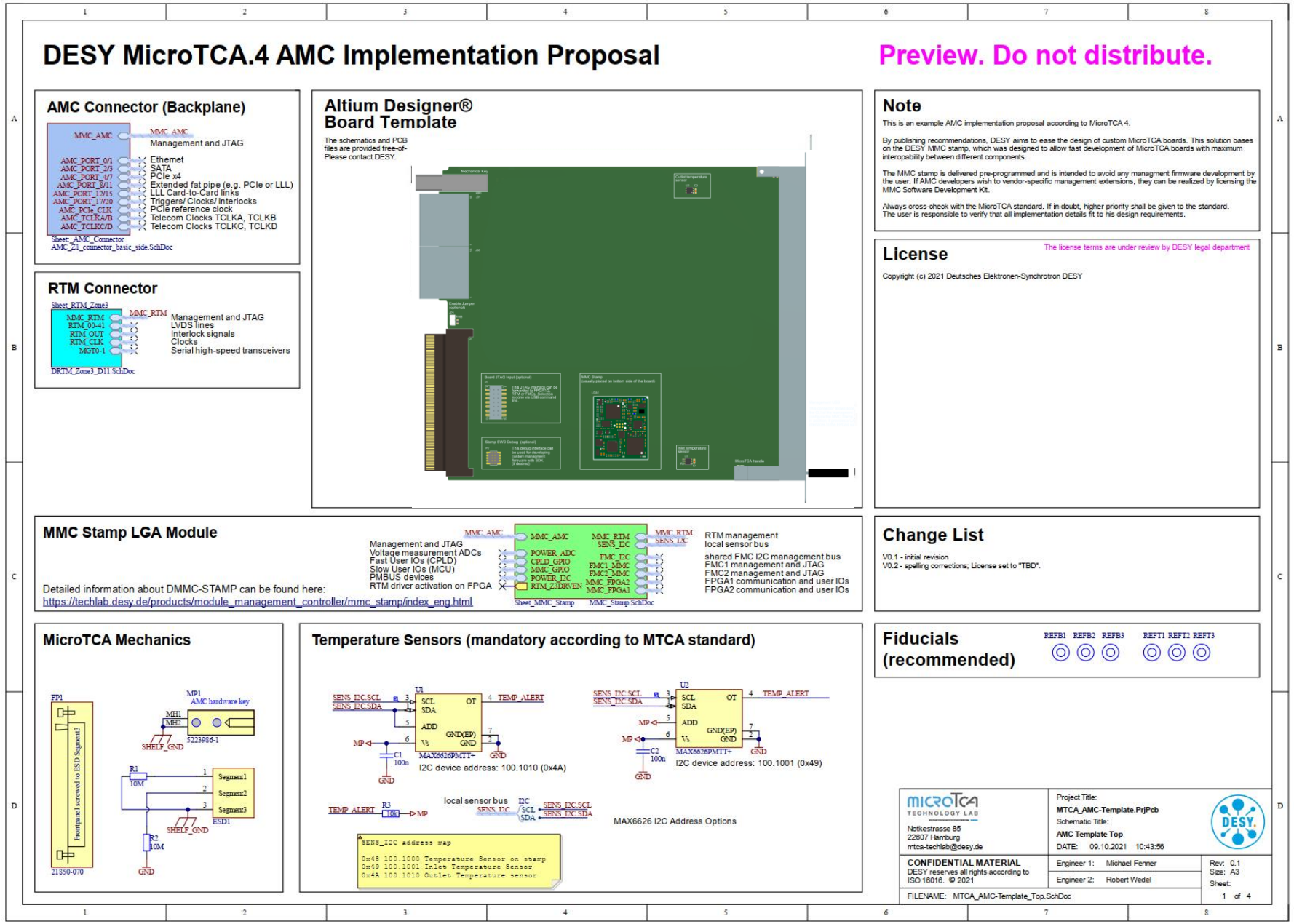
- Is a board under development
- Allows D1.2 / D1.3 class RTM
- up to 8 MGTs to RTM
- Very flexible clocking system with White Rabbit support
- Targets JESD204B applications
- Shares components with DAMC-Supercarrier FMC2ZUP
- Cost-Optimized version
- Uses Ultrascale+ MPSoC (smaller package than Supercarrier)
- 2 interfaces with 4GiB of DDR4 each
- Trigger input/output on front panel
- SFP+ Output on the front panel

DAMC-BPMZUP – block diagram



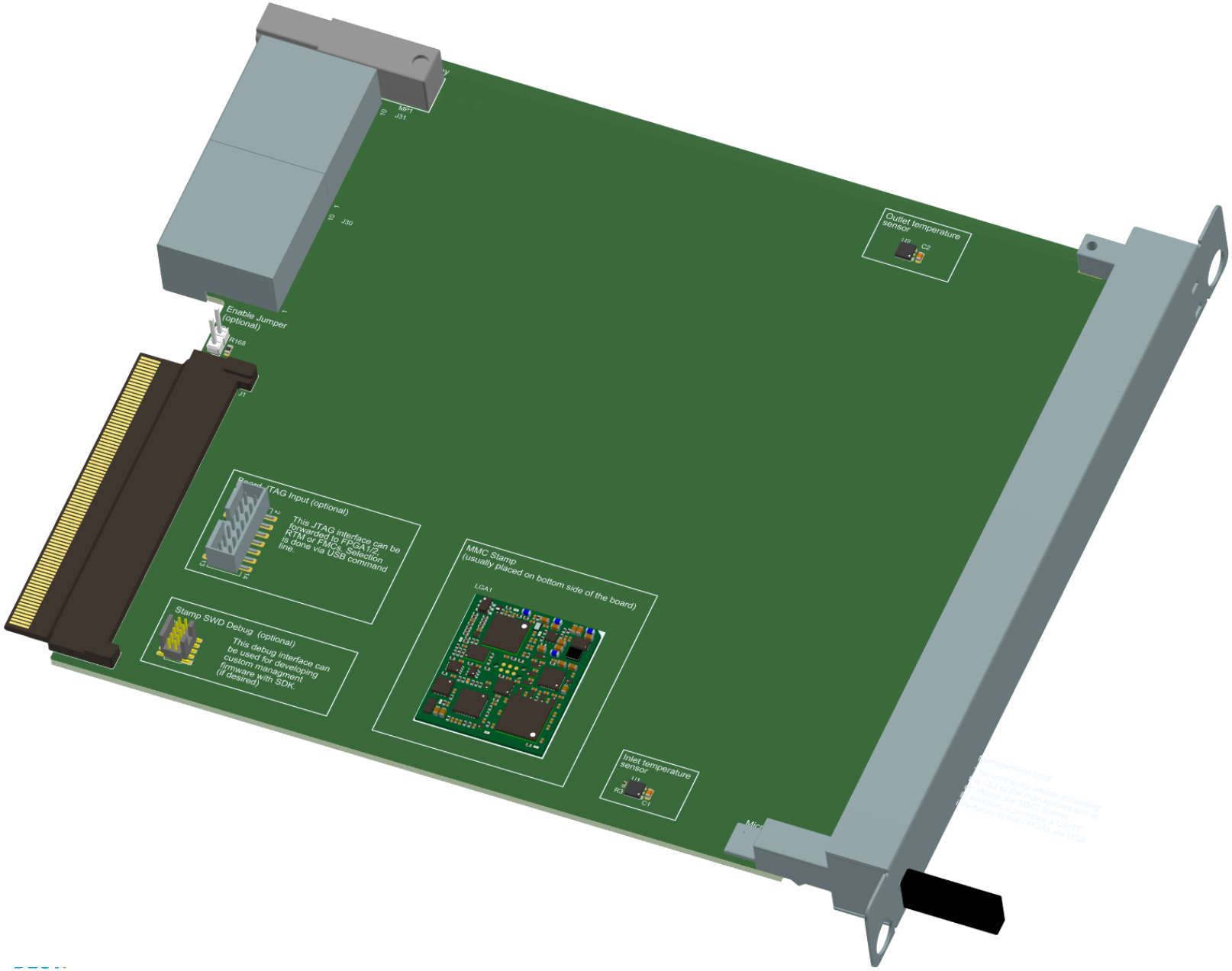
Design Support

AMC Template



- DESY encourages custom HW developments
- We provide a design template
- Includes lots of explanations and hints

AMC Template - Altium™ Designer board



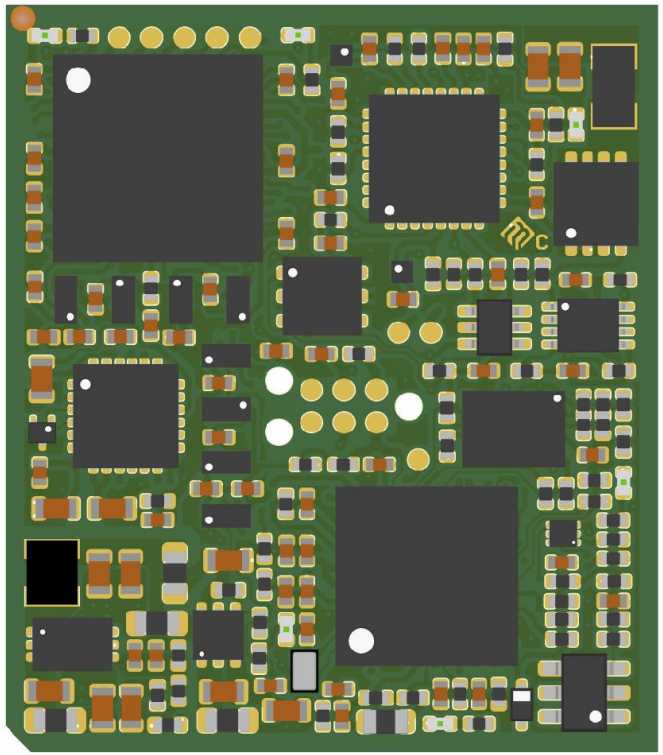
- Schematics and Layout available for free
- Proven mechanical shapes, footprints and symbols
- Jump-Start MicroTCA design
- 3D bodies included

AMC Template - Based on MMC Stamp

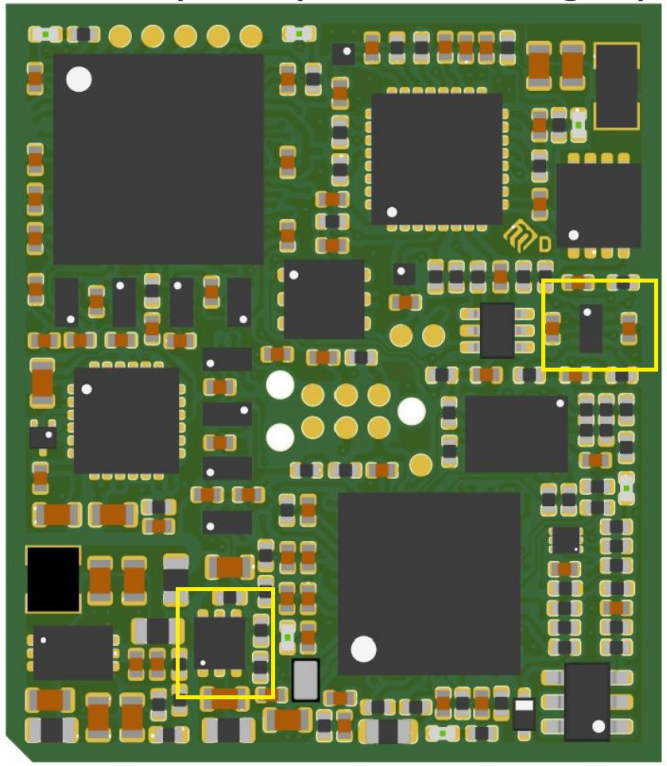
MMC Stamp is available (Obsolescence Management is done by DESY)

- All changes transparent to the user (we take care of firmware)

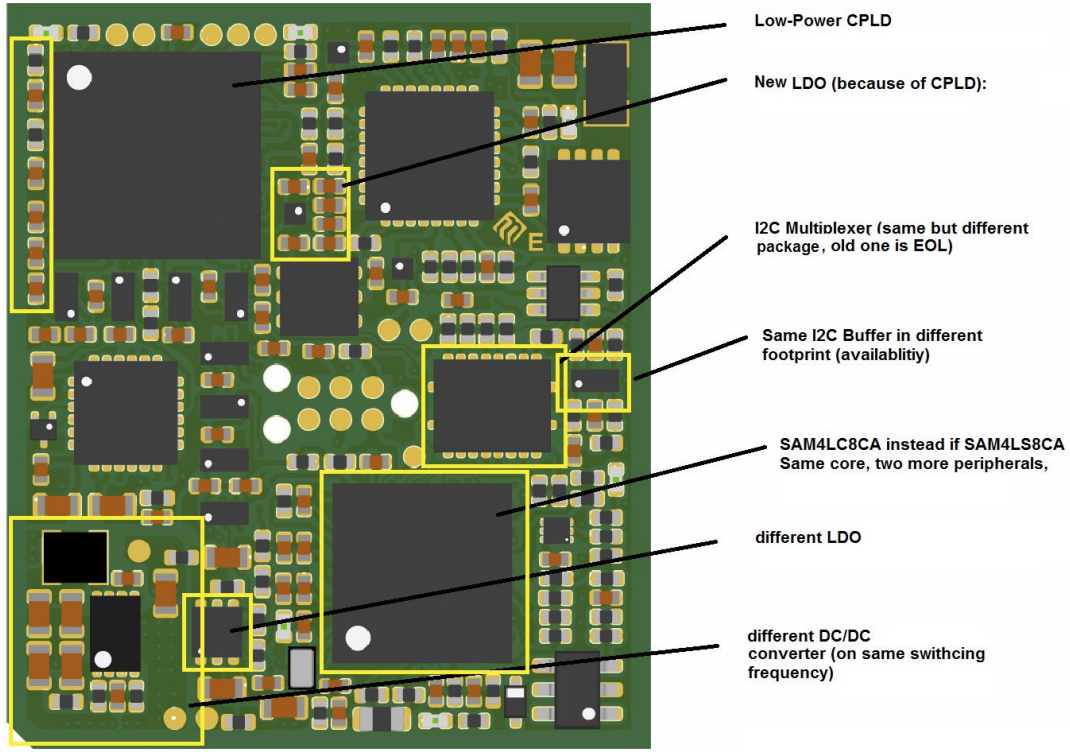
out of stock



current (transparent changes):

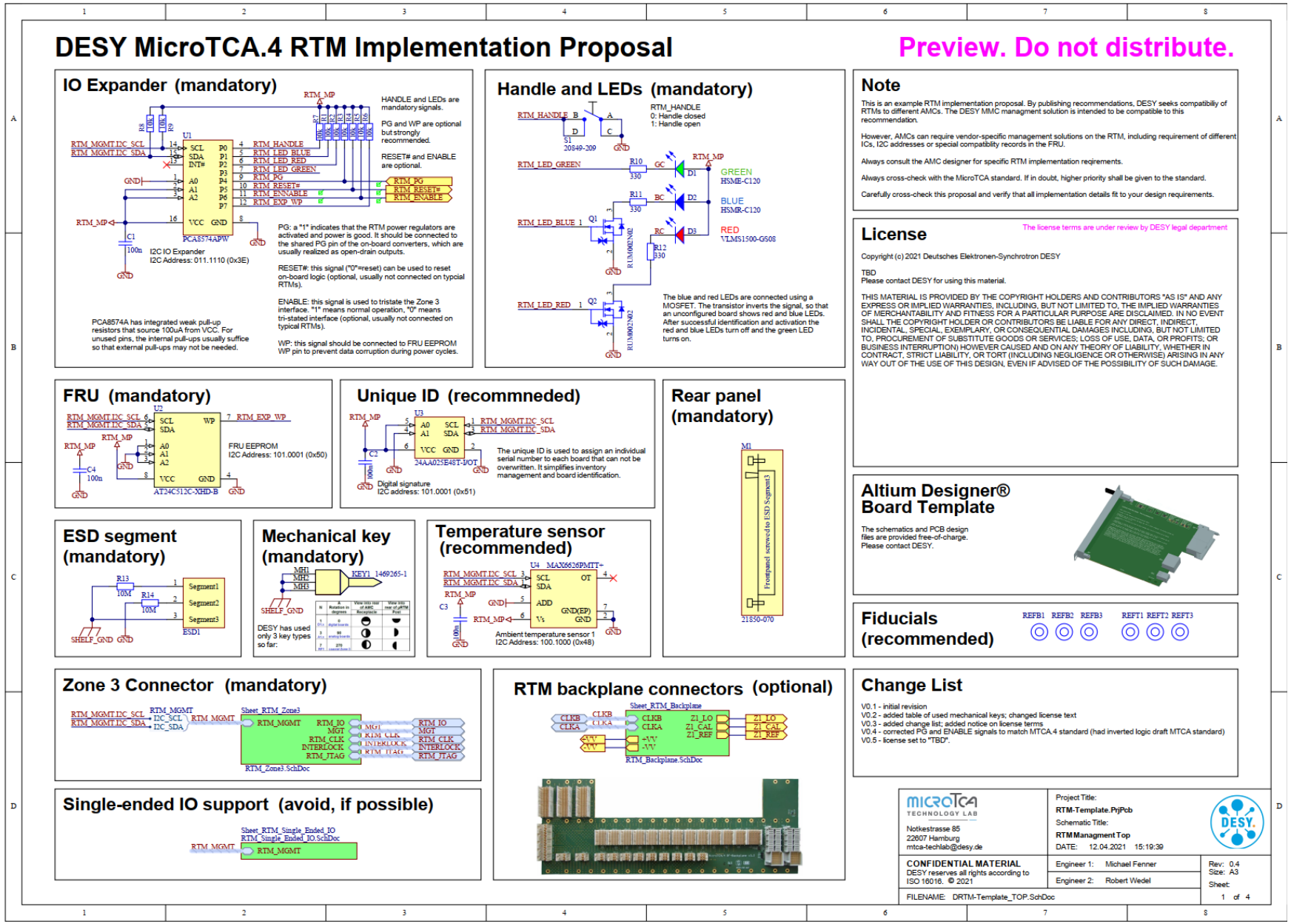


Backup 2022 (under verification):



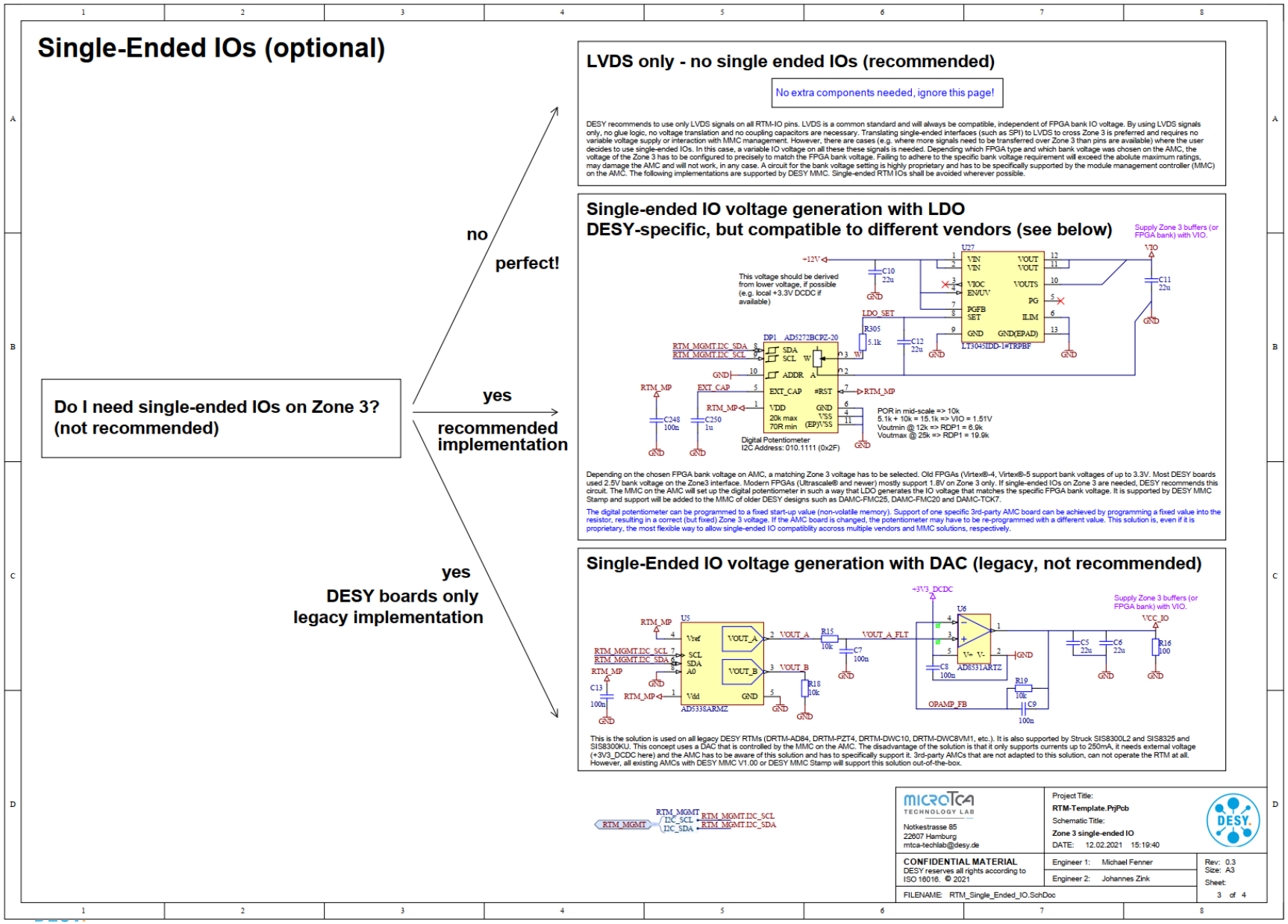
Firmware upwards/backwards compatibility

RTM Template



- Same as for AMC
- Explanations beyond standard
- Collection of best practices

RTM Template



- Provides design hints
- Focus: Proprietary solutions outside standard
- Aims to unify proprietary developments

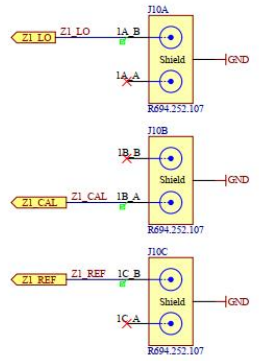
RTM Template

RTM Backplane Connectors (optional)

The MicroTCA specification Revision 4.1 defines an optional RTM backplane. It is used for distribution of high-precision clocks inside the chassis to MicroTCA RTMs. In addition, a clean bipolar supply voltage can be distributed on this backplane. Special eRTMs (without connection to AMC backplane) generate precision clocks and reference signals for the RTMs. A special rear power module can generate a clean supply voltage for the RTMs. Management of the eRTMs and rear power supplies is realised by using a MCH-RTM, which forwards the rear managment signals the front MCH.

A 12-slot chassis with the shown RTM backplane is available from nVent / Schroff GmbH. A modular rear power module and the MCH-RTM are available from N.A.T. GmbH. The DRTM-LOG1300 is available from DESY.

RTM Backplane Zone 1
RF cock input



connetor pinout for slots #4-#12

	A	B
1A	rfu	LO
1B	CAL	rfu
1C	rfu	REF

rfu – pins reserved for future use

RTM Backplane Zone 2
Analog voltage and additional clocks

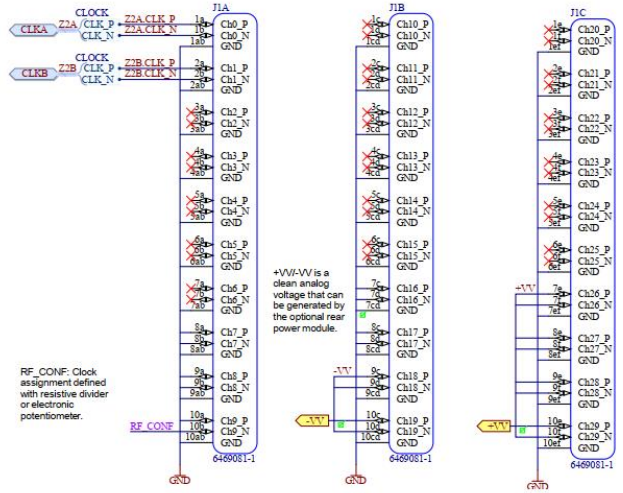


Table 20: J21 connetor pinout for slots #4+#12

	a	b	ab	c	d	cd	e	f	ef
1	CLKxA_P	CLKxA_N	GND	rfu	rfu	GND	rfu	rfu	GND
2	CLKxB_P	CLKxB_N	GND	rfu	rfu	GND	rfu	rfu	GND
3	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
4	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
5	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
6	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
7	rfu	rfu	GND	GND	GND	GND	+VV	+VV	GND
8	GND	GND	GND	GND	GND	GND	+VV	+VV	GND
9	GND	GND	GND	-VV	-VV	GND	+VV	+VV	GND
10	PS1#	RF_CONF	GND	-VV	-VV	GND	+VV	+VV	GND

rfu – pins reserved for future use

RF_CONF Settings

The voltage on RF_CONF is used to request a specific clock assignment on the Zone1 and Zone 2 connectors. A fixed voltage coming from a simple resistor divider can be presented here. Alternatively the voltage can be generated using an electronic potentiometer for maximum flexibility. (5V supply is required for full scale setting.)

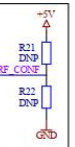
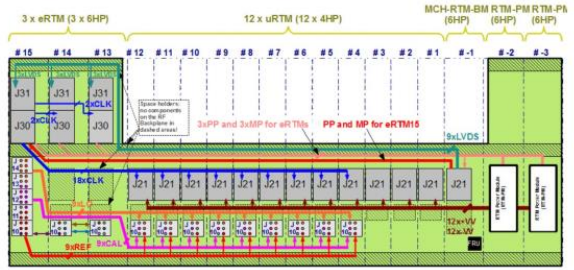


Table 3: RF_CONF signal voltage levels and their assignment

State	CLKs LO CAL REF [1=yes, 0=no]	Required DC level [V]	Lower limit [V]	Upper limit [V]
1	0000	0,4	0,26	0,54
2	0001	0,68	0,54	0,82
3	0010	0,96	0,82	1,1
4	0011	1,24	1,1	1,38
5	0100	1,52	1,38	1,66
6	0101	1,8	1,66	1,94
7	0110	2,08	1,94	2,22
8	0111	2,36	2,22	2,5
9	1000	2,64	2,5	2,78
10	1001	2,92	2,78	3,06
11	1010	3,2	3,06	3,34
12	1011	3,48	3,34	3,62
13	1100	3,76	3,62	3,9
14	1101	4,04	3,9	4,18
15	1110	4,32	4,18	4,46
16	1111	4,6	4,46	4,74

Connectivity of DESY RTM Backplane

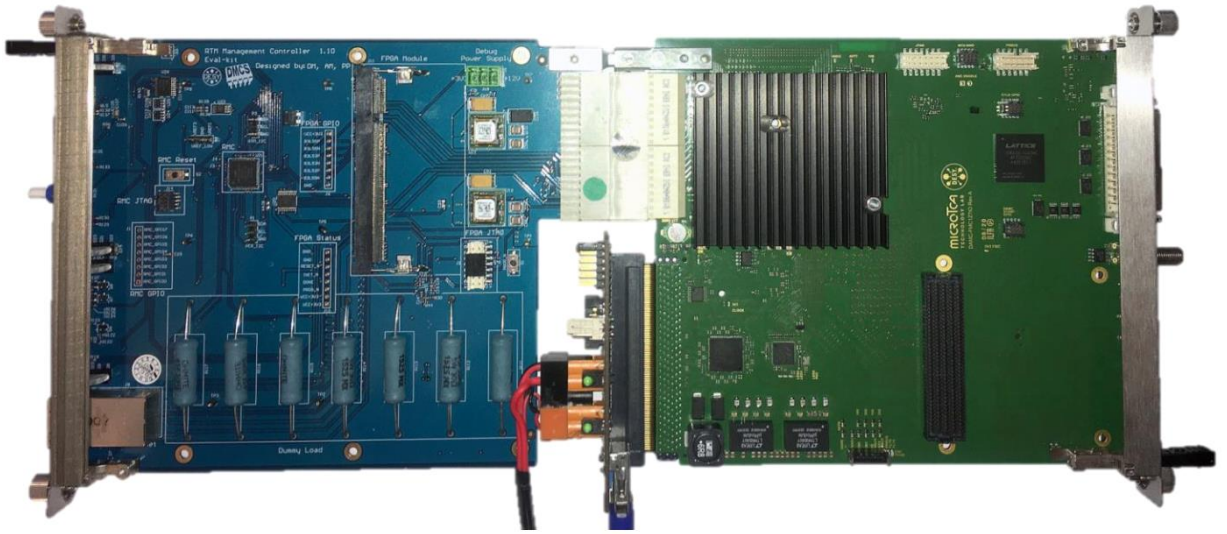


DRTM-LOG1300 - eRTM clock generator

MicroTCA TECHNOLOGY LAB Notkestrasse 85 22607 Hamburg mtca-techlab@desy.de	Project Title: RTM-Template.PrjPcb Schematic Title: RTM Backplane Connectors DATE: 12.02.2021 15:19:40	DESY.
CONFIDENTIAL MATERIAL DESY reserves all rights according to ISO 16016. © 2021	Engineer 1: Michael Fenner Engineer 2: Johannes Zink	Rev: 0.3 Size: A3 Sheet: 4 of 4
FILENAME: RTM_Backplane.SchDoc		

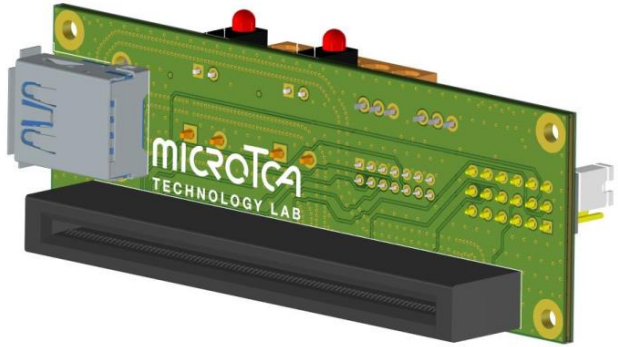
- RTM Backplane design information included

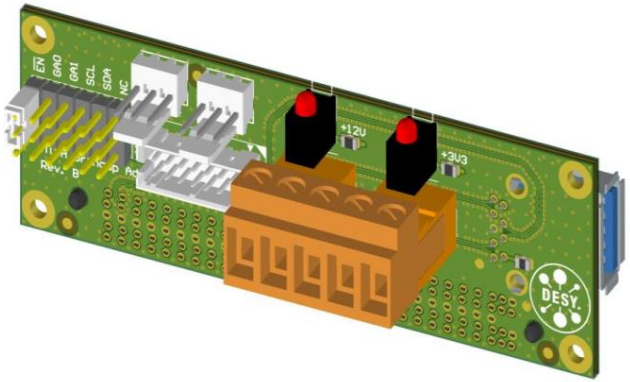
MicroTCA Bring-up adapter



Top view

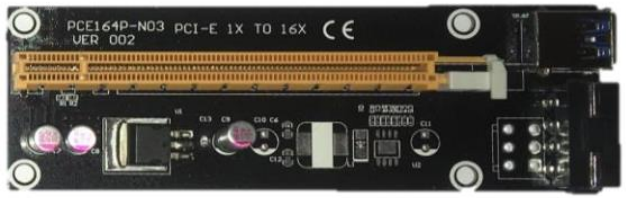
Bottom view



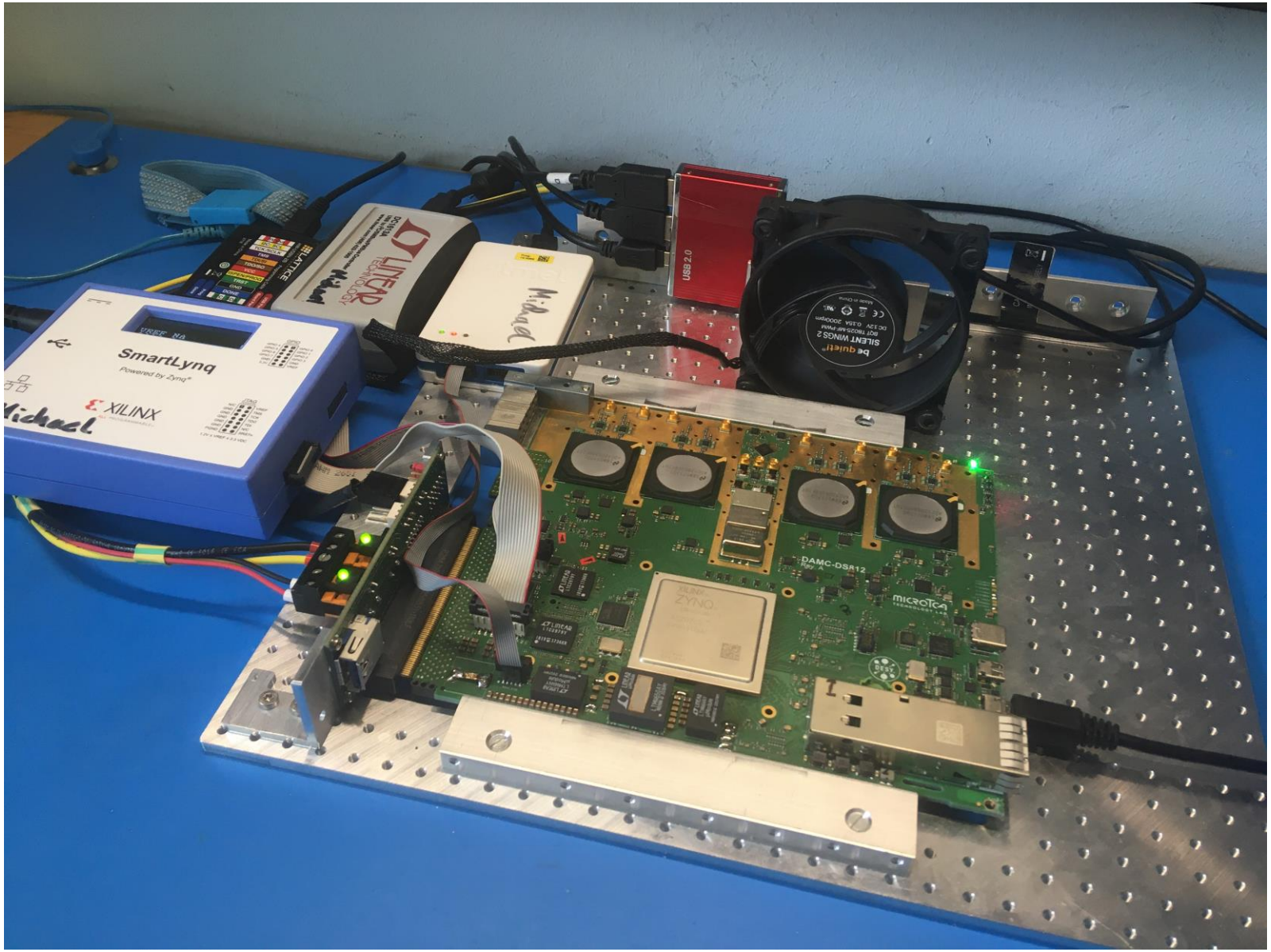


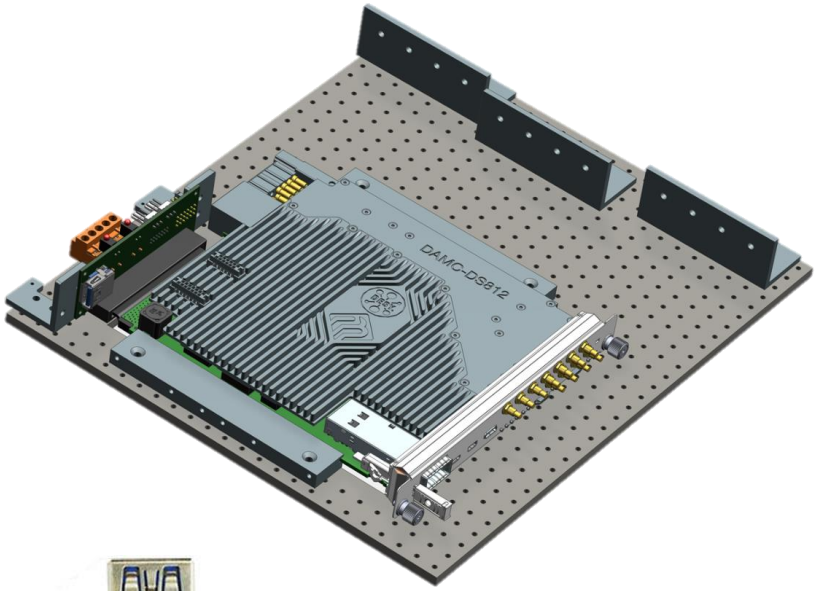
Laboratory bringup tool

DESY provides production files for free



MicroTCA Bring-up adapter





- Mechanical design data can be shared (please contact us)

courtesy of R. Wedel

Thank you!

Acknowledgments: Johannes Zink, Jan Marjanović, Nikola Radaković

Kontakt

DESY. Deutsches Elektronen-Synchrotron

www.desy.de

Michael Fenner
MSK
michael.fenner@desy.de
+49 (0) 40-8998-1885