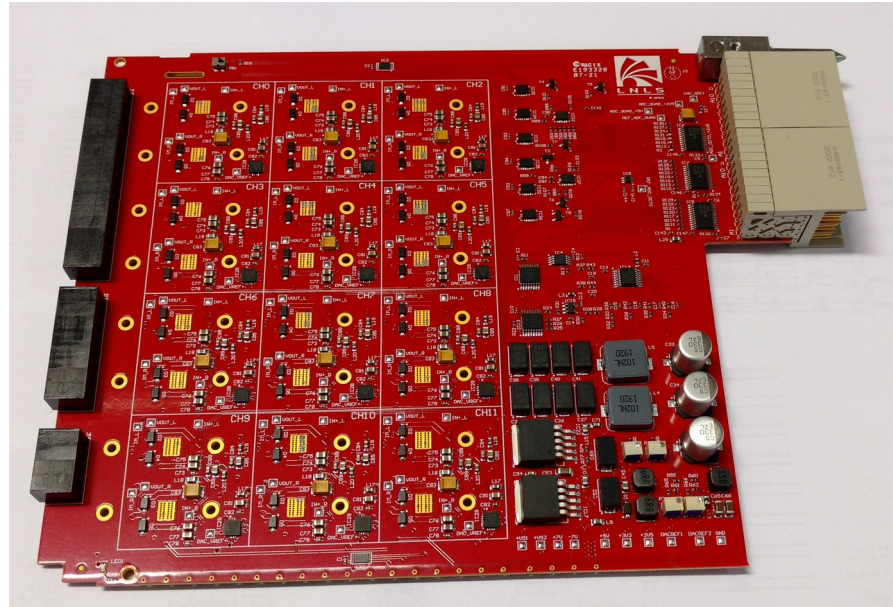# Fast Orbit Corrector Power Supply in MTCA.4 Form Factor for Sirius Light Source

Augusto F. Giachero, Lucas M. Russo, Daniel O. Tavares

MicroTCA Workshop 2021

CNPEM
Centro Nacional de Pesquisa em Energia e Materiais

LNLS
sirius
Brazilian Synchrotron Light Laboratory

# Design Goals

- Correct small electron beam orbit disturbances up to 1 kHz;
- Digital current loop control;
- At least 8 channels for each module;
- Up to ±30 µrad deflection (@ 3 GeV);
- Fit into a MicroTCA RTM slot (mid-size);

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# Requirements

- Small signal bandwidth of 10 kHz;
- Maximum total power consumption of 36 W;
- Current slew rate of 0.5 A/ms;
- Maximum total latency of 5 µS.

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# Requirements

- Load resistance: 1 Ω (max);
- Load inductance: 3.5 mH - 6.2 mH;
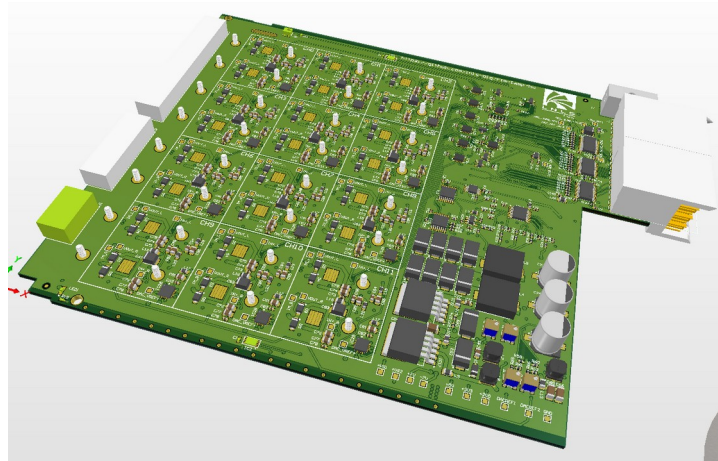- ±1 A output capability per channel;
- Noise Spectral Density:

$$\frac{1.5\,\mu A}{\sqrt{Hz}}\left(f \geq 1\,kHz\right) \qquad \frac{1.5\,\mu A}{\sqrt{Hz}} \times \frac{1\,kHz}{f}\left(f < 1\,kHz\right)$$

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# Electronics Design

- Class AB power amplifier;
- 16 bits DAC, 16 bits* ADC;
- Buck converter (≥90% efficient).
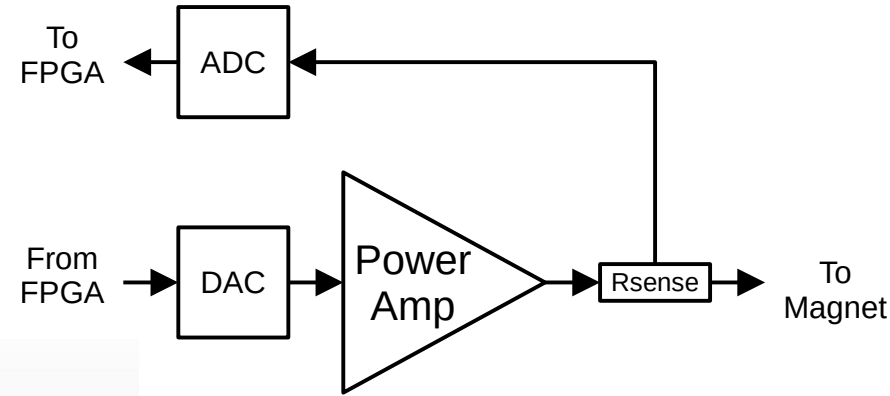
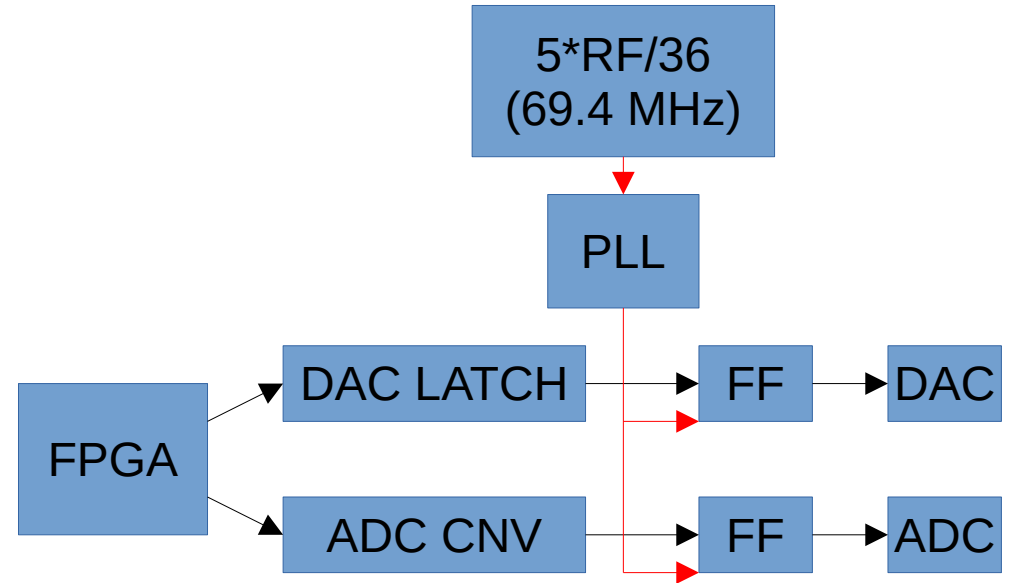\* 16 bit differential input ADC, but only the positive range is used.

# ADC – DAC Synchronization

- D/A and A/D conversions are synced to 2x the beam revolution frequency;

- CNV and LATCH signals are jitter cleaned by retiming them to the RF reference clock.
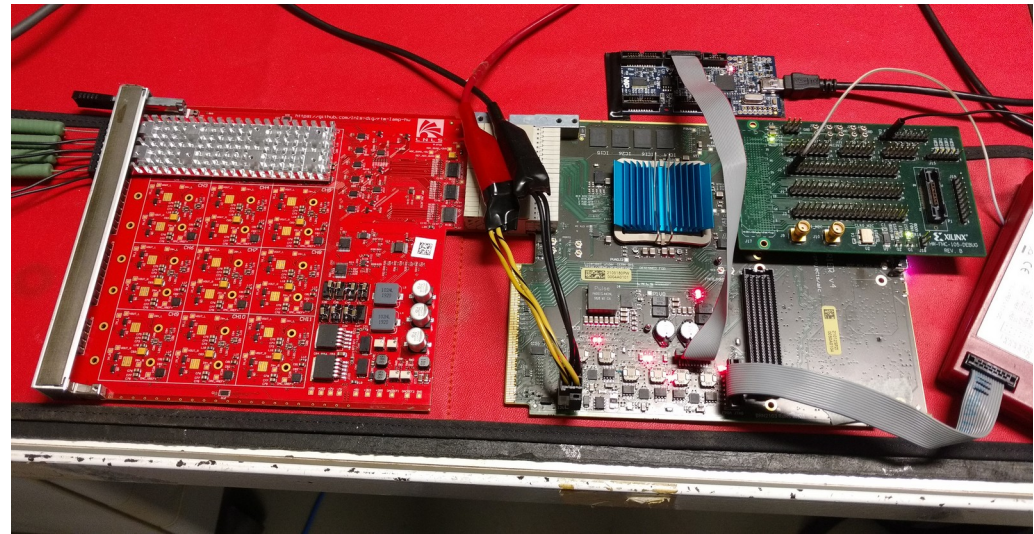
# DC Power Supply Design

- A compromise between efficiency and switching noise;

- All switching converters can be synced with a multiple of the beam revolution frequency.
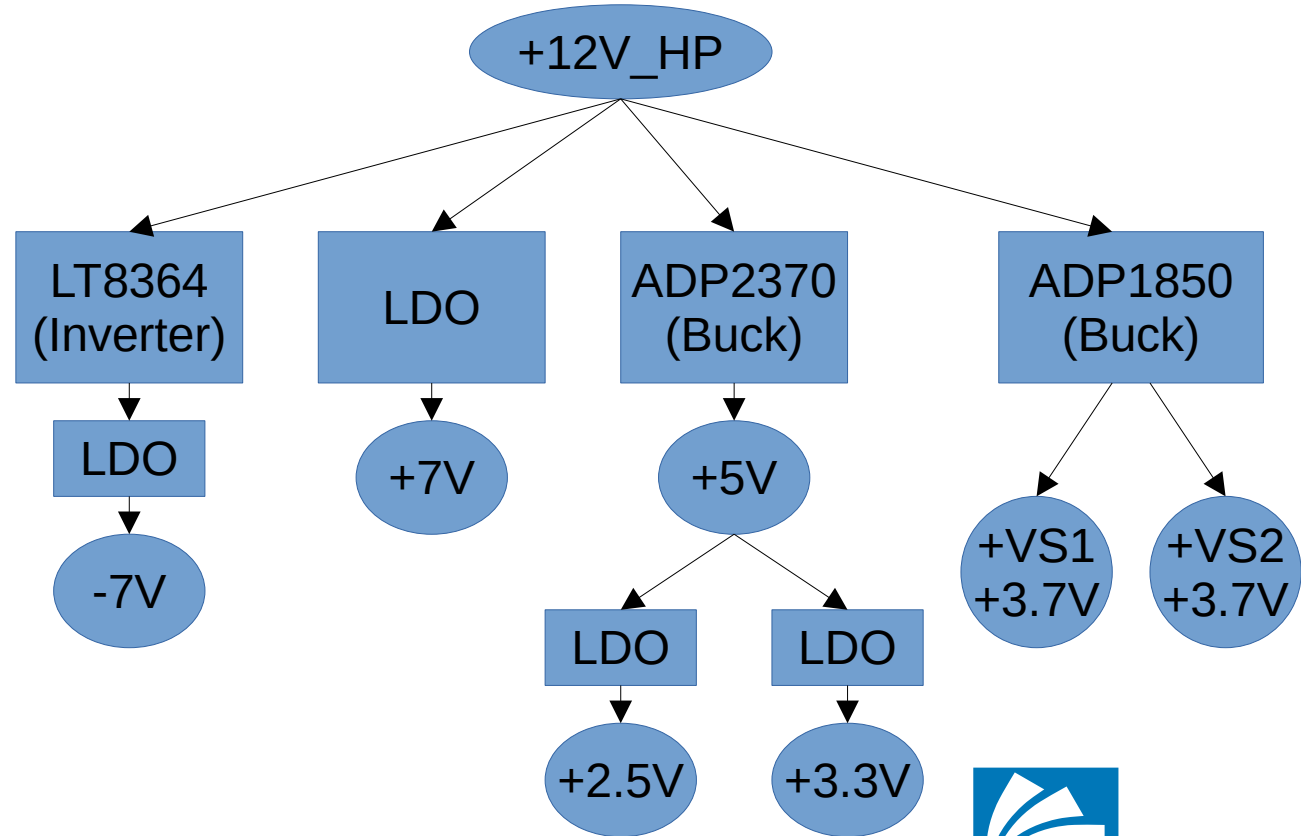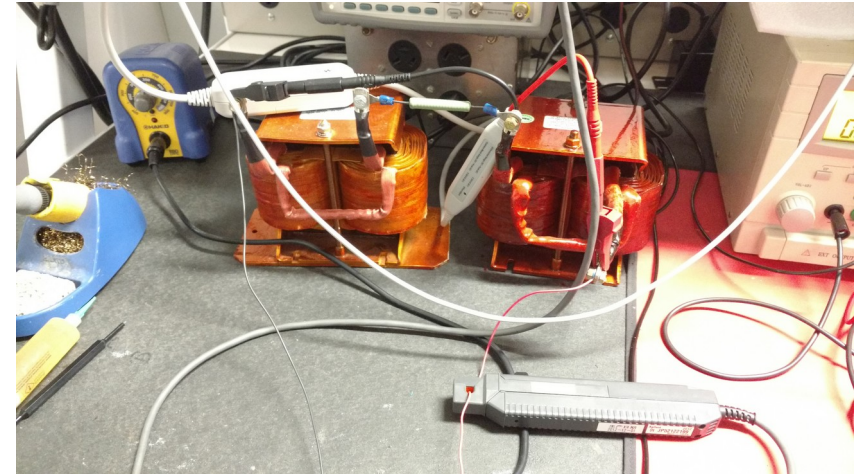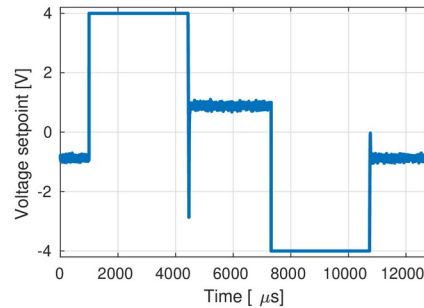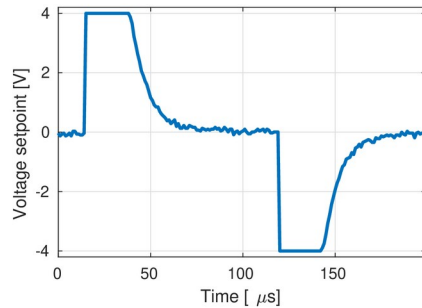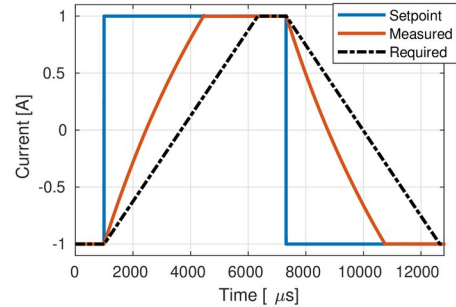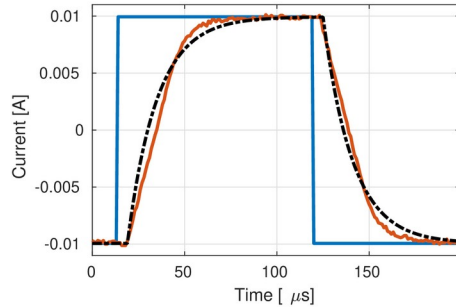
# Prototype Validation

- Buck efficiency measured at 92.5%, 29.6W available to the power amplifiers;
- DAC and ADC digital interfaces tested;
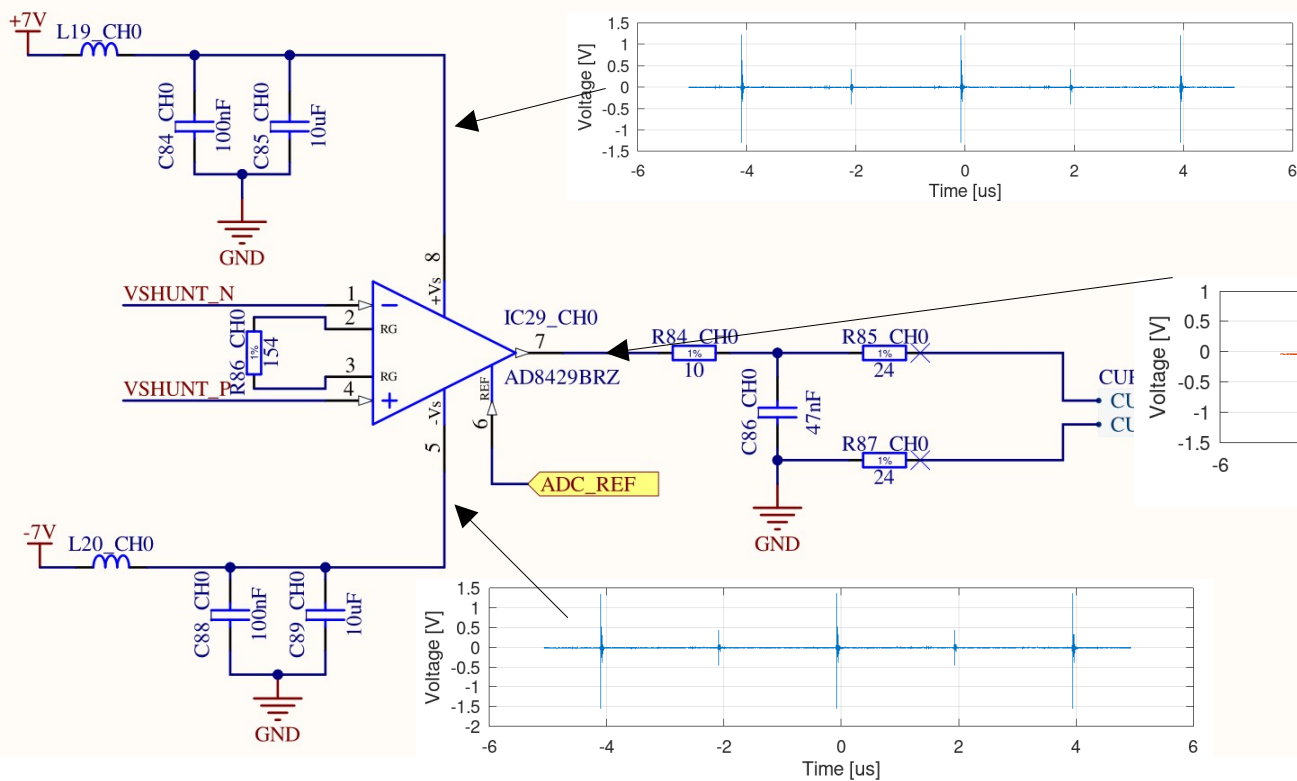- Short circuit protection working.

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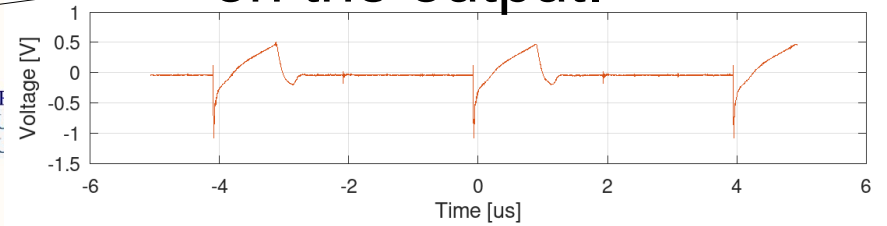
# Prototype Validation (Step Resp.)



1.17Ω 5.9mH load

# DAC to ADC interference



Very short voltage glitches on supply rails results in large glitches on the output.

Turns out it was a grounding issue.

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# openMMC support

- Initial AFC v4 support was recently contributed by Creotech;

- Proof-of-concept code available for the RTM FOFB supply, but it still 'hacky';

- A major code refactoring is planned for improving modularity, removing duplicated code, improve debugging (see https://github.com/lnls-dig/openMMC/issues/110).

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# Next steps

- Validate the second prototype (will arrive soon);
- Order the final production lot;
- Finish the software and FPGA firmware;
- OpenMMC improvements;
- Drive a real corrector magnet.

# Thank you!

IPAC 2021 Paper:
https://accelconf.web.cern.ch/ipac2021/papers/thpab257.pdf

PCB design:
https://github.com/lnls-dig/rtm-lamp-hw
(Licensed under CERN OHL S v2)

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daniel.tavares@lnls.br

open source
hardware

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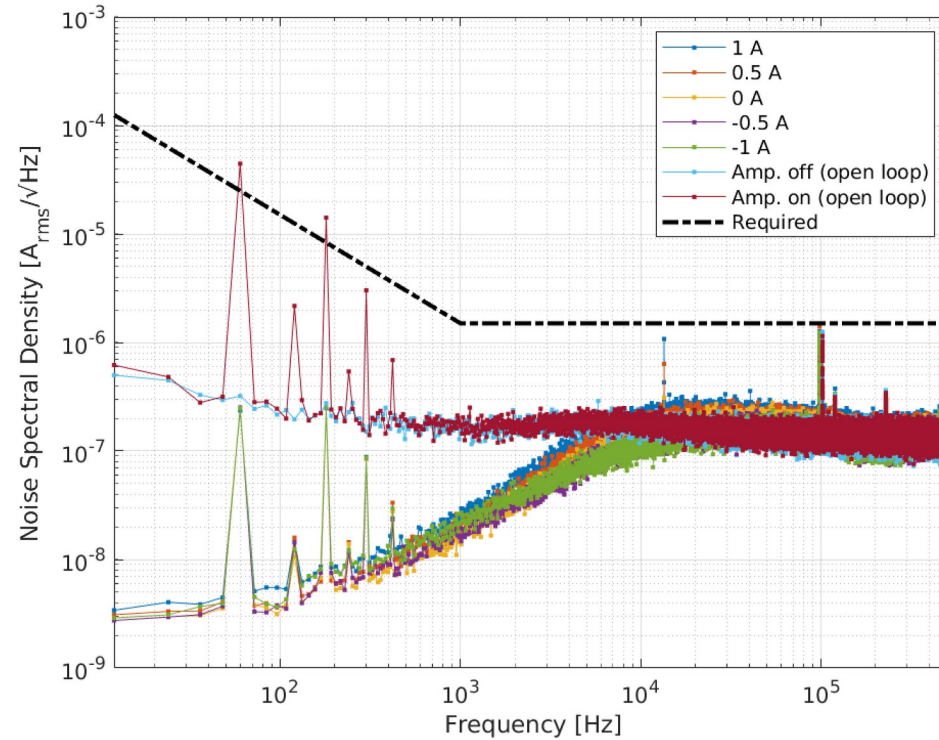Centro Nacional de Pesquisa
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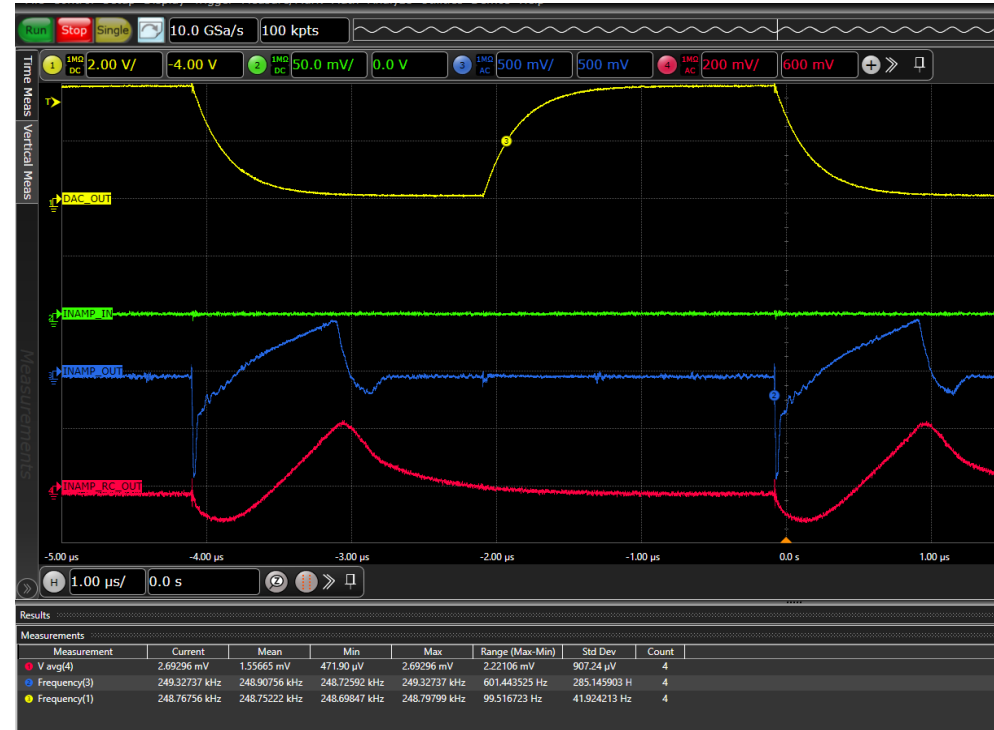Brazilian Synchrotron
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# Backup slides

# Prototype Validation (Noise)

# DAC to ADC interference

- Large signal disturbances coming from the instrumentation amplifier output (channels 0, 2, 3, 5, 6, 8 and 9);
- Correlates with the DAC output transitioning from 4V to 0V.

# DAC to ADC interference

- Careful debugging revealed that it was a grounding issue (only a single via connecting multiple components);
- Workaround: remove decoupling capacitors for +-7V rails.

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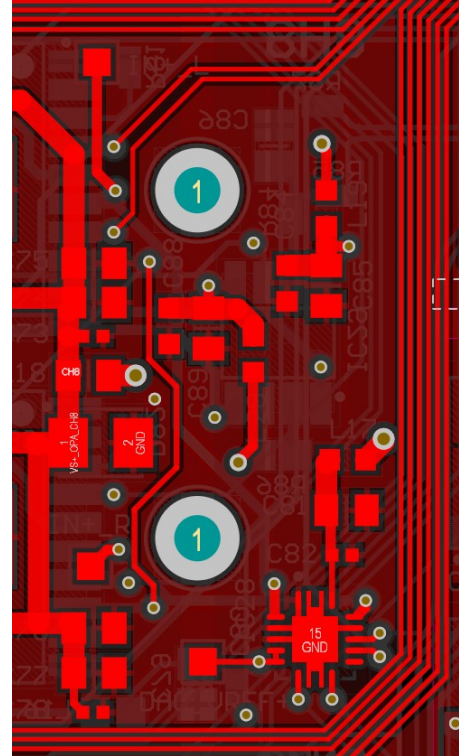
# DAC to ADC interference (solution)

- Connect the DAC GND directly to the ground plane;
- Improve ground impedance between the top layer and ground plane (use the screw mounting holes).
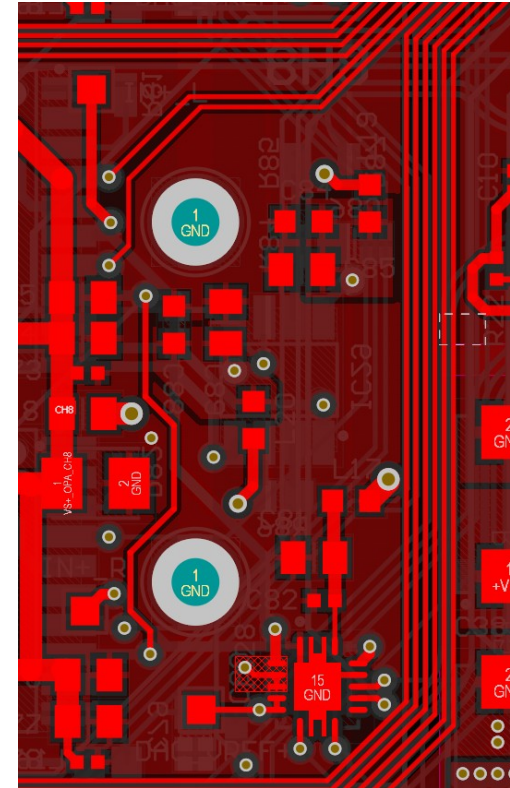
# LTC2320 Low Jitter Clock Timing



Low Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Retiming Flip-Flop