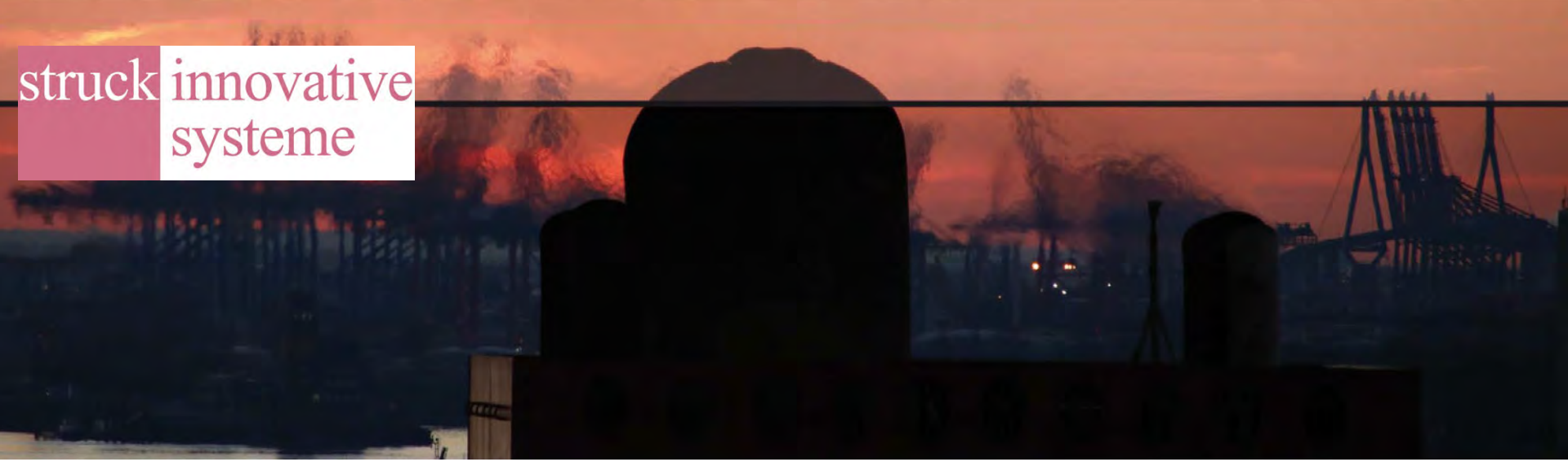


struck innovative systeme

10 Years of Struck MTCA Modules for Beam Instrumentation

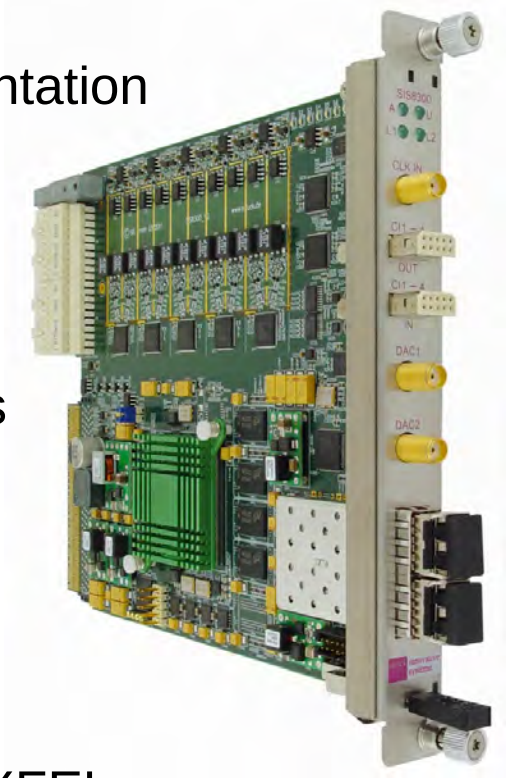
History, Present and Outlook w. Applications

Outline

- First MTCA.4 Digitizer AMC → SIS8300 (2011)
- First MTCA.4 RTM → SIS8900 (2011)
- 125 MSPS Digitizer Evolution
  - SIS8300-V2,
  - SIS8300-L2 (2014)
  - SIS8300-KU (2016)
- SIS8325 250 MSPS Digitizer (2015)
- Sidetrack on Export Control
- Digital I/O AMCs (2015, 2018)
- More Rear Transition Modules
- SIS8160/SFMC01 FMC Carrier/Digitizer FMC (2017)
- Outlook: SIS8172 FMC Carrier (2022)
- Insights on Shipping, Packaging and Component Sourcing

SIS8300-V1/2 Digitizer Properties

- MTCA.4
- 4 lane PCI Express → 640 MB/s readout
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- Two 250 MS/s 16-bit DACs for fast feedback implementation
- High precision, flexible clock distribution logic
- Internal, front panel, RTM and BP clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- Virtex-5 FPGA
- Up to 32 MSample DDR2 Memory per channel
- Additional point to point links over backplane
- In field firmware upgrade

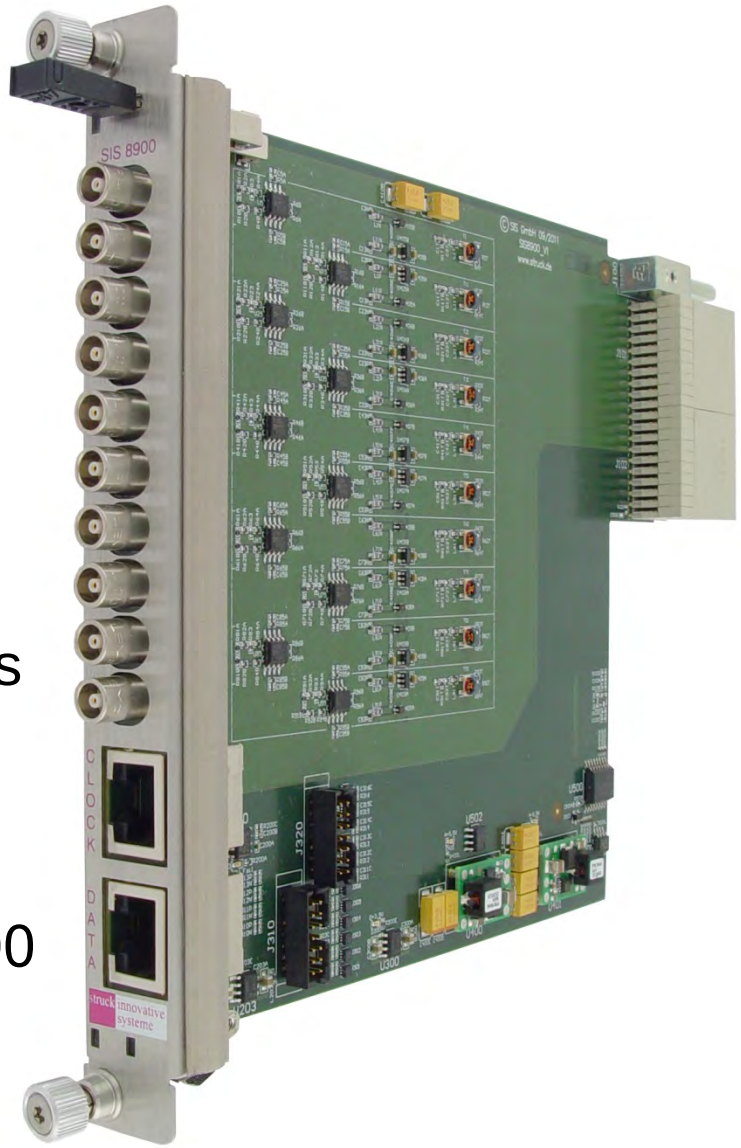


Motivation: Joined DESY-Struck ZIM Project targeted at XFEL

SIS8900 Single Ended Input RTM

- 10 LEMO 00 connectors (FBM option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each

Original Motivation: Test Board for SIS8300



SIS8900 Single Ended Input RTM

- Good Resolution (no variable gain, offset)

Tradeoffs
- fixed input configuration
- no offset capability (symmetric input ranges only)

06397	SIS8900 RTM AC LEMO
06398	SIS8900 RTM DC LEMO +-1V 50 Ohm
06425	SIS8900 RTM 8AC2DC LEMO
06953	SIS8900 RTM 5AC5DC LEMO 3rd
07389	SIS8900 RTM LEMO +-5V 10 KOhm
07490	SIS8900 RTM DC LEMO +-2.5V 1KOhm Sonderv...
07525	SIS8900 RTM DC LEMO +-2.5V 50/1KOhm Sond...
07696	SIS8900 RTM LEMO +-1.5V 10 KOhm Sonderver...

SIS8300-L2 Digitizer Properties

SIS8300 w. new FPGA family
and new IPMI

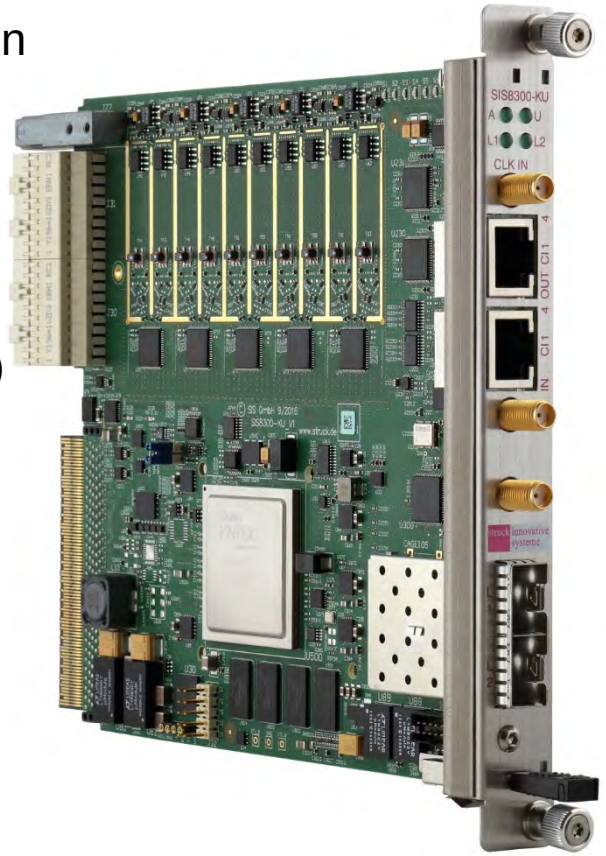
- XC6VLX130T-2FFG1156C FPGA
- DDR3 Memory
- DESY MMC1.0

Central Motivation:
Higher Point to Point Link throughput

→ XFEL Working Horse

SIS8300-KU Properties

- 10 Channels 125 MS/s 16-bit or 250 MS/s 14-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual FPGA Configuration Flash
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Vivado Project for Custom Firmware Development
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible



Central Motivation: ISE → Vivado, FPGA Lifespan, ESS/Lund initiated

SIS8325 Properties (Helmholtz Validation Fund Project)

Basically higher sampling speed version of SIS8300-L2

- 10 Channels 250 MS/s 16-bit ADC

Central Motivation:

- Sampling of shorter pulses,
- Faster availablity of feedback data
- Slightly changed clock distribution scheme (HMC987LP5E replacing 2x AD9510 for improved jitter < 50 fs)

Tradeoff I: Historically still Virtex-6 based

But: SIS8300-KU in 250 MSPS 14-bit has almost the same number of effective bits

Tradeoff II: 16-bit > 180 MS/s → export control

Export Control (Digitizers)

Dual use: Commission delegated regulation (EU) 2020/1749

3A002h h. "Electronic assemblies", modules, or equipment, specified to perform all of the following:
1. Analogue-to-digital conversions meeting any of the following:

	From #Bits	To # Bits	MSPS	Struck Boards
a	≥ 8	<10	> 1300	-
b	≥ 10	< 12	> 1000	SIS3305 (2 x 5 GSPS interleaved, VME)
c	≥ 12	< 14	> 1000	SIS1332 (PCIe)
d	≥ 14	< 16	> 400	SFMC01
e	≥ 16		> 180	SIS8325

General Equal Treatment Act (AGG) No. EU001
Australia, Island, Japan, Canada, New Zealand, Norway, Switzerland including Liechtenstein, UK and the USA

Export Control (FPLDs, FPGAs)

so far of no concern for Struck
to be checked with new products anyway

3A001.a
7. Field programmable logic devices having any of the following:
a. A maximum number of single-ended digital input/outputs of greater than 700; or
b. An ‘aggregate one-way peak serial transceiver data rate’ of 500 Gb/s or greater;

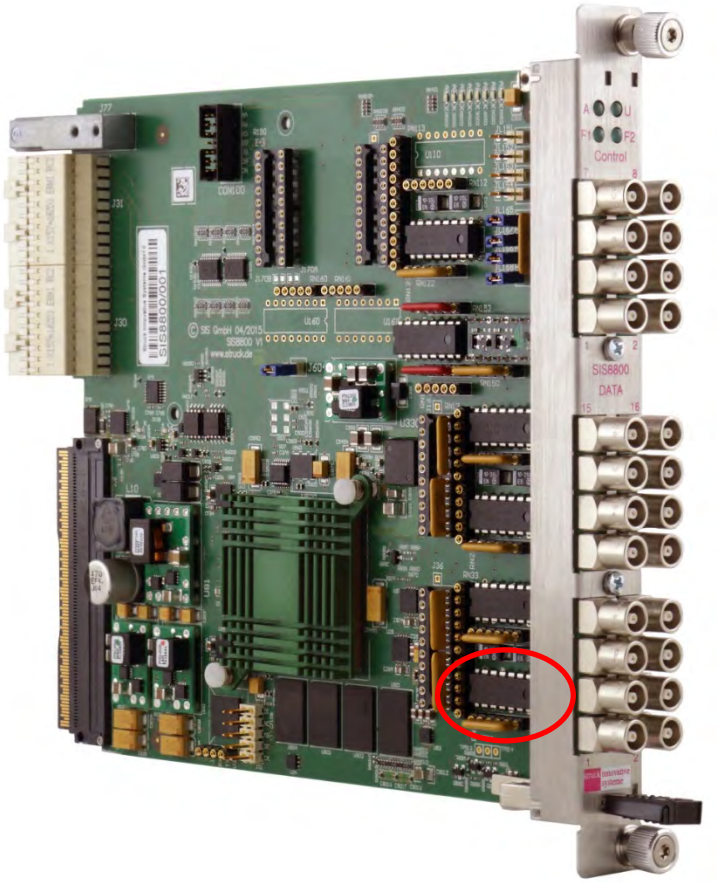
Note: 3A001.a.7. includes: — Complex Programmable Logic Devices (CPLDs) — Field Programmable Gate Arrays (FPGAs) — Field Programmable Logic Arrays (FPLAs) — Field Programmable Interconnects (FPICs) NB: For integrated circuits having field programmable logic devices that are combined with an analogue-to digital converter, see 3A001.a.14.

Note: Encryption and other features may come on top
Keep an eye on: Sanctions Lists, Embargo Countries, Military Goods List, Nuclear Suppliers Group,…

SIS8800 Multi Purpose Scaler

Functionality

- MTCA.4 AMC
- 4 Lane PCI Express connectivity
- XC6VLX130T-2FFG1156C Xilinx
- Dual FPGA Configuration Flash
- Redundant PCIe implementation
- 2 GByte DDR3 memory
- 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
- 200 MHz count rate (NIM/ECL)
- 4 control in-/4 control front outputs
- Zone 3 Class D1.1 compatible
- MMC 1.0 under DESY license LV91



Original motivation for development: FAIR LASSIE BLM System
→ good fit for SRI (Synchrotron Radiation Instrumentation) also

Note: NIM/ECL suffers from discontinuation of MC10H124 and MC10H125

SIS8864 64 channel LVTTL Digital I/O AMC

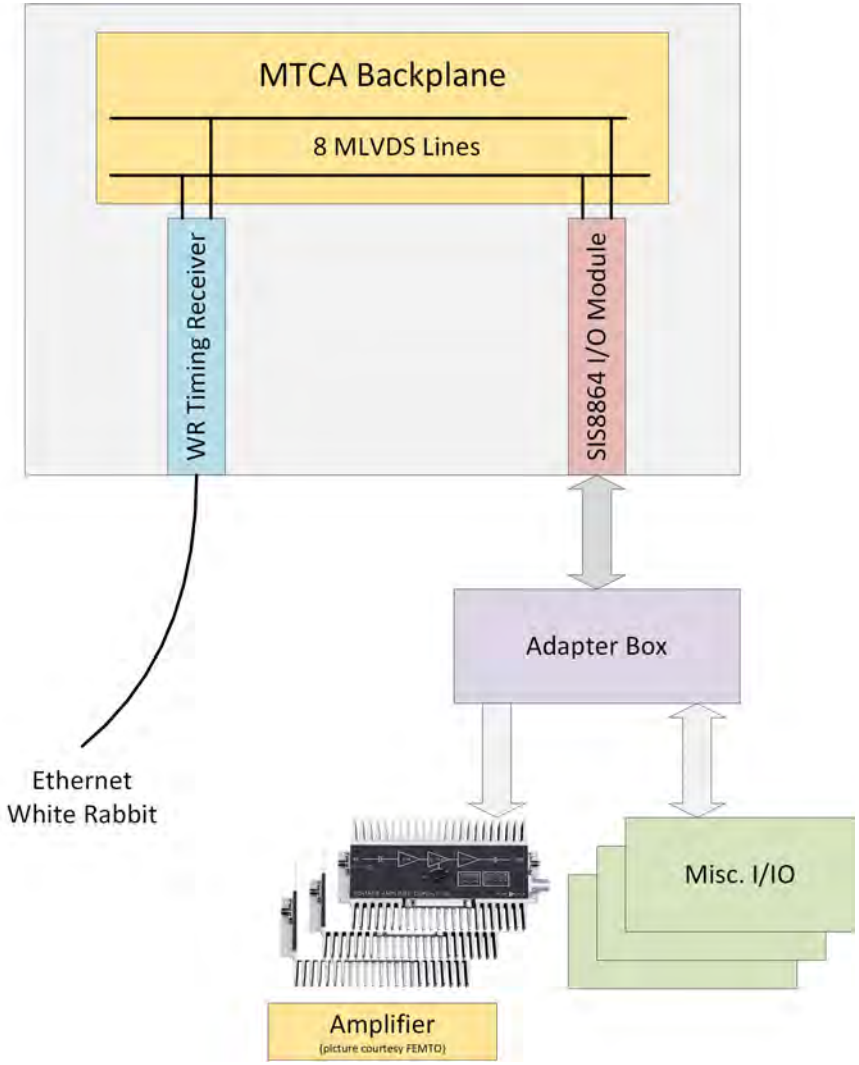
- Machine cycle dependent & generic ouput pattern with digital input
- Alternative to OHWR FMC carrier and two I/O FMC‘s
- Ready to run firmware
- Application specific firmware adaptations

SIS8864 64 channel LVTTL Digital I/O AMC Properties

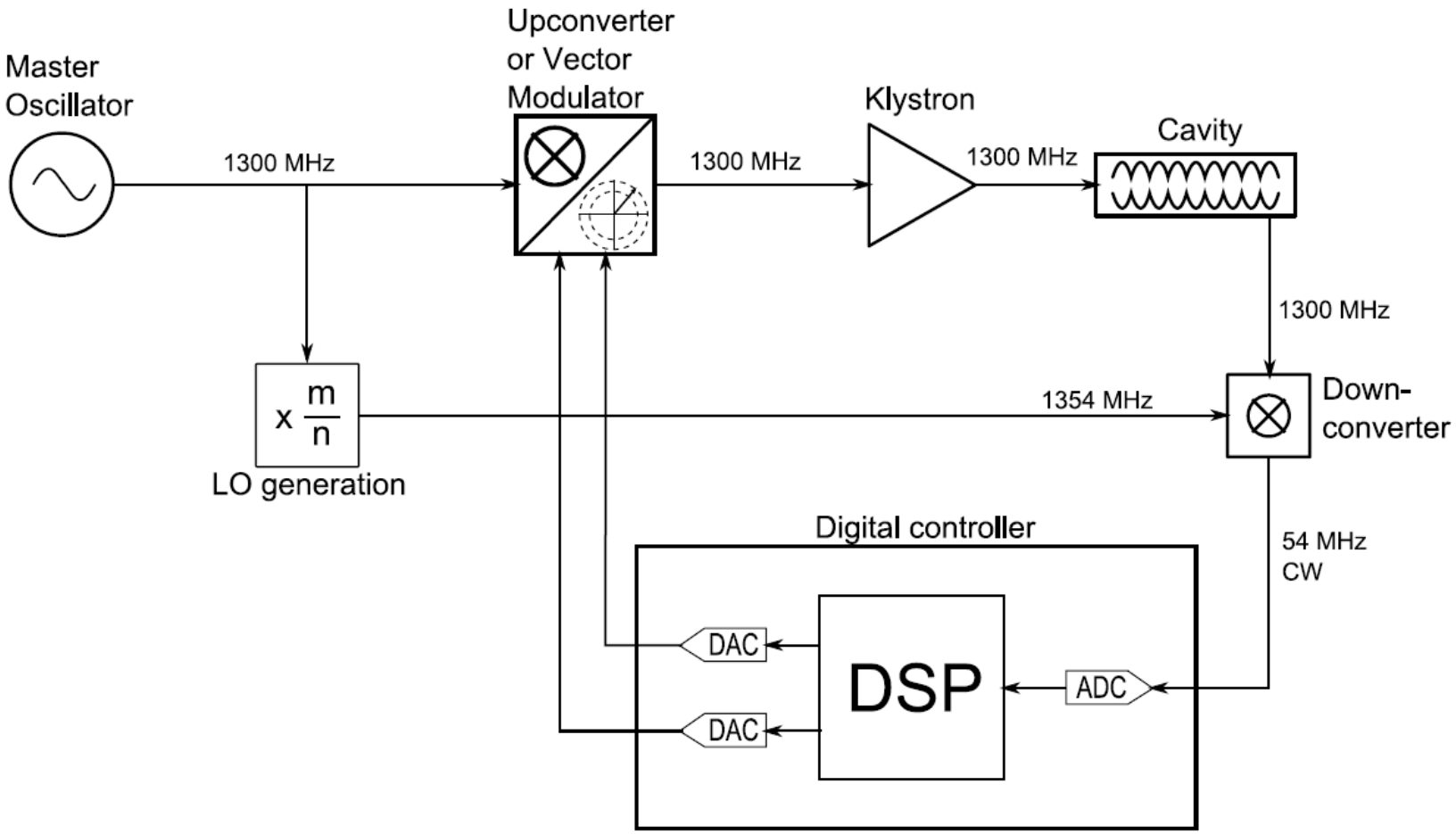
- AMC with Double Width Mid-Size form factor
- Xilinx XC7A15T-2FGG484C Artix-7 FPGA
- Single lane PCI Express Gen2 Interface
- 1 AMC Port GbE
- 2 AMC Ports Point-to-Point Serial Link
- 4 AMC Ports MLVDS (8 MLVDS lines)
- 2 Front panel 32 data I/O: Mini D Ribbon (MDR) (TTL/LVTTL)
- I/O direction programmable in 8-Bit Groups
- 1 Front panel control Input: LEMO (TTL/LVTTL)
- 1 Front panel control Output: LEMO (LVTTL)
- In field firmware upgrade capability
- Module Management Controller ATxmega128A1U, IPMB-L interface
- DESY MMC1.0 (under LV 91)

Note: Firmware for SIS8300-KU digitizer I/O extension over the Point to Point links available (ALBA, Diamond, …)

Typical FAIR SIS8864 Digital I/O Use Case

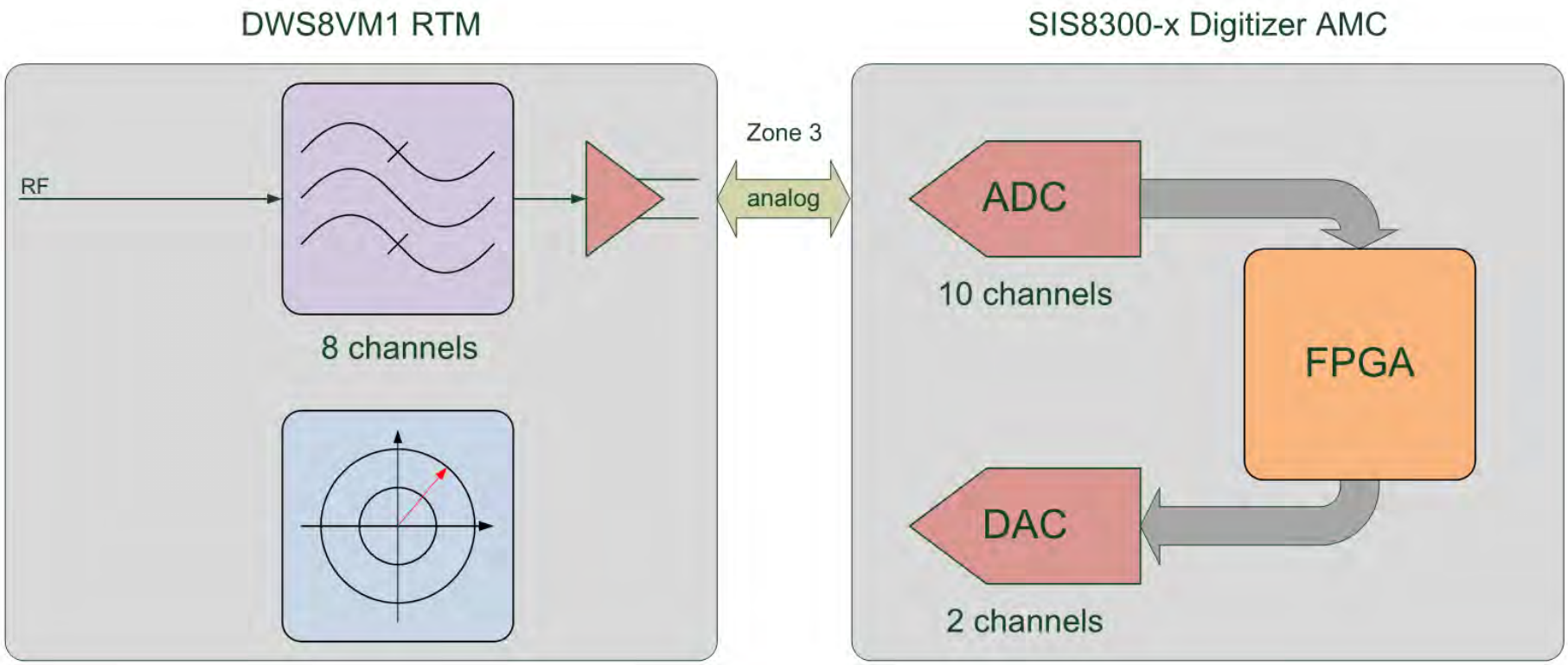


LLRF (Low Level Radio Frequency) IF Sampling Scheme



from thesis Karol Suchecki

SIS8300-x/DWC8VM1 as single cavity LLRF solution covering 350 MHz to 6 GHz



Current combination: SIS8300-KU Kintex-Ultrascale Digitizer and DWC8VM1

DWC8VM1
8 Channel Downconverter
One Channel Vectormodulator*

Model	f_{min} in MHz	f_{max} in MHz
DWC8VM1LF	350	500
DWC8VM1	500	3500
DWC8VM1HF	3500	6000

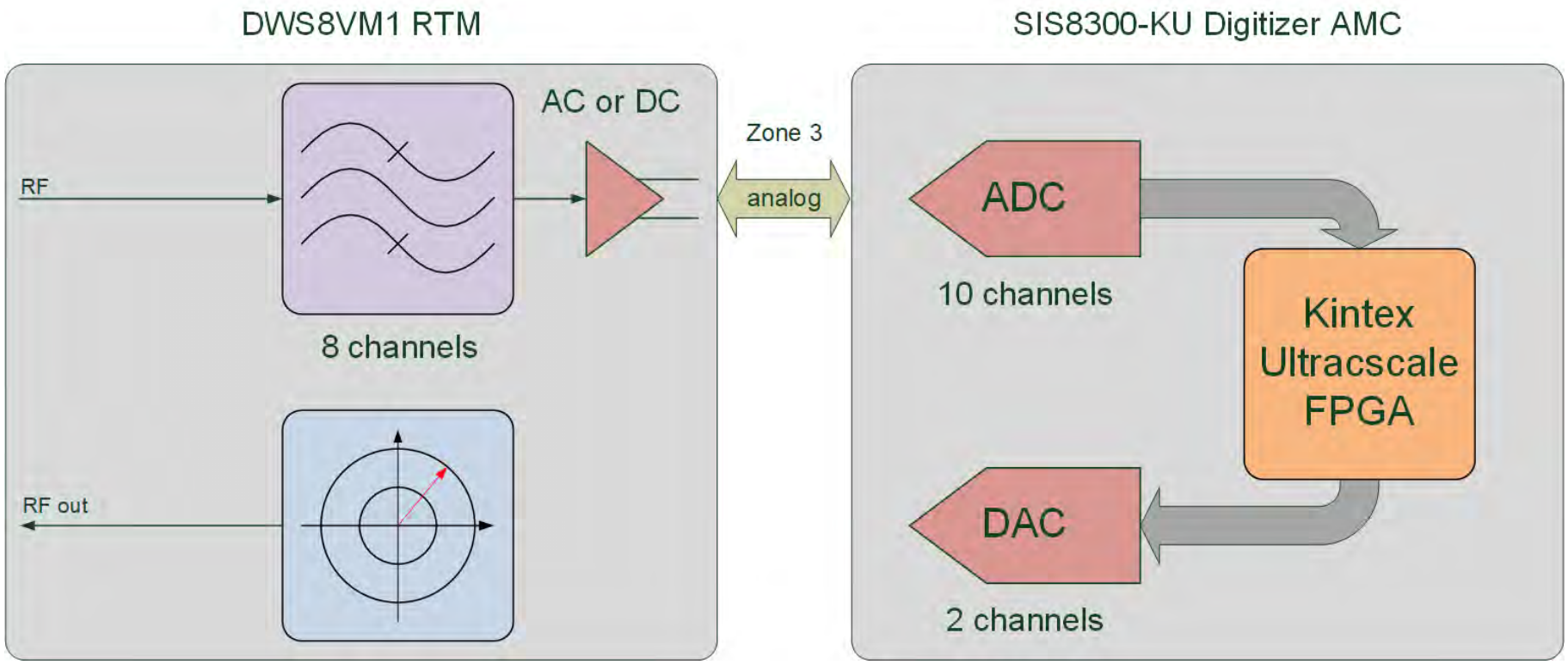
DWC8VM1 Overview Table

*under license from DESY

DWC8VM1 Properties

- MTCA.4 RTM Implementation
- 8 Channels Downconverter
- 350 MHz - 6 GHz (3 different types)
- 8 Channel FBM Multi Coax. Connector (CH1 to CH8)
- 2 Auxilliary Channels
- One Channel Vector Modulator
- VM Output 50 MHz to 6 GHz
- SMA Vector Modulator Output
- Various Intermediate Frequencies
- Switchable Front End Attenuators
- LO Clock From Front Panel or RF Backplane
- LO Power Level Monitor
- Interlock Scheme
- I2C Support
- Zone 3 Class A1.1 compatible

SIS8300-KU/DS8VM1
as single cavity LLRF solution
covering 5 MHz to 500 MHz



DS8VM1
8 Channel Direct Sampling
One channel vectormodulator*

SIS8300-KU/DS8VM1
as single cavity LLRF solution
covering 5 MHz to 500 MHz

Application Examples
UNILAC
NICA
ELBE
CERN PS

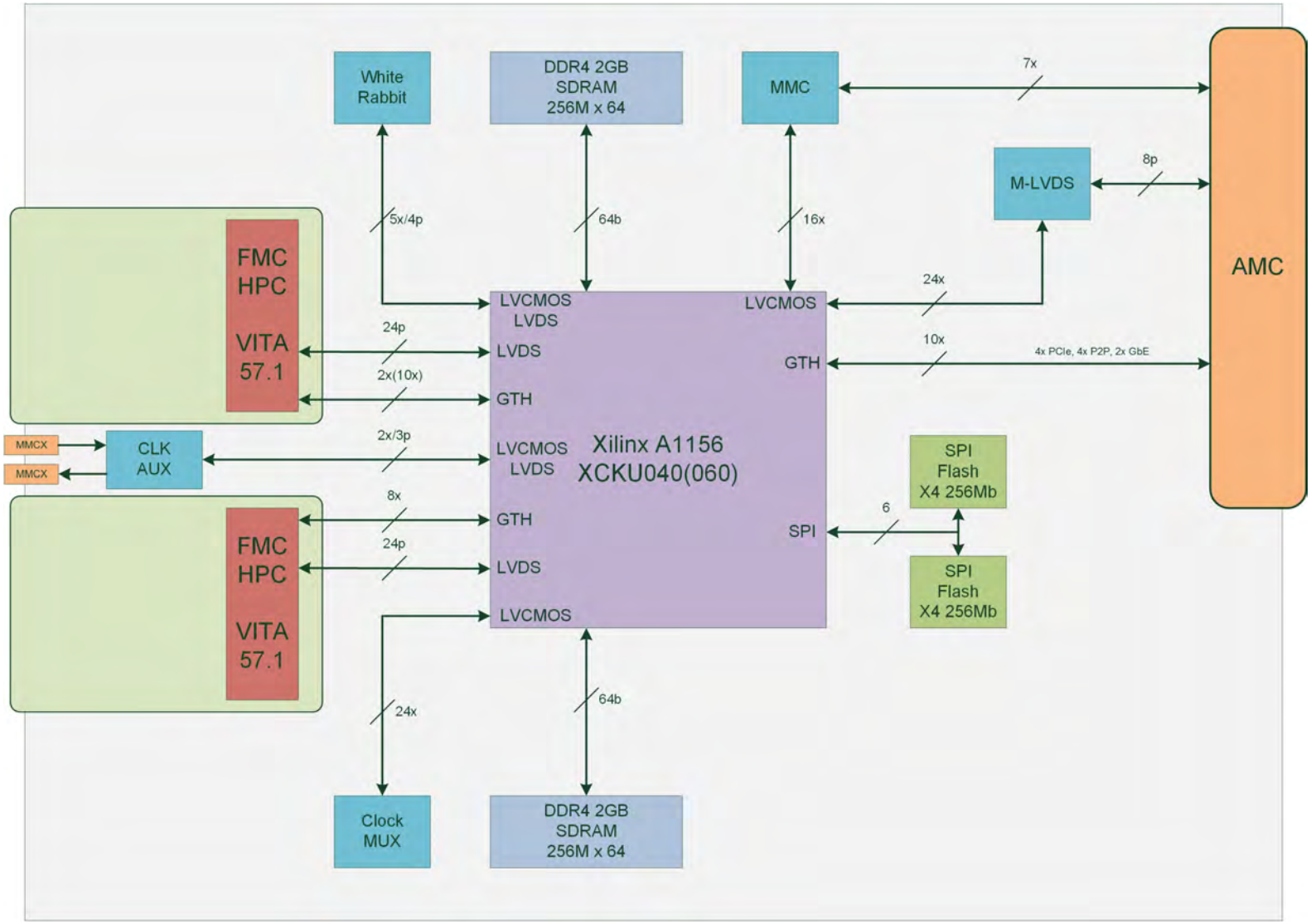
*under license from DESY

System Integration Examples

SIS8160 Dual FMC Carrier AMC

- 4-lane PCI Express Gen3 Connectivity
- Xilinx XCKU40- or XCKU060-1FFVA1156C Kintex Ultrascale FPGA
- Dual Boot
- Front Panel MMCX Clock Input
- Front Panel MMCX Digital In-/Output (HW Configuration)
- Point to Point Links
- 4 MLVDS µTCA Ports (AMC Ports 17-20) → 8 MLVDS lines
- 2 HPC FMC Sites
- Variable FMC VADJ (1,0V - 1,8V)
- Low Jitter Clock Generation and Management
- 2 x 2 GByte DDR4 Memory with two Memory Controllers
- White Rabbit Option (over FMC 2)
- Stand Alone Operation Option
- MMC1.0 under DESY LV91

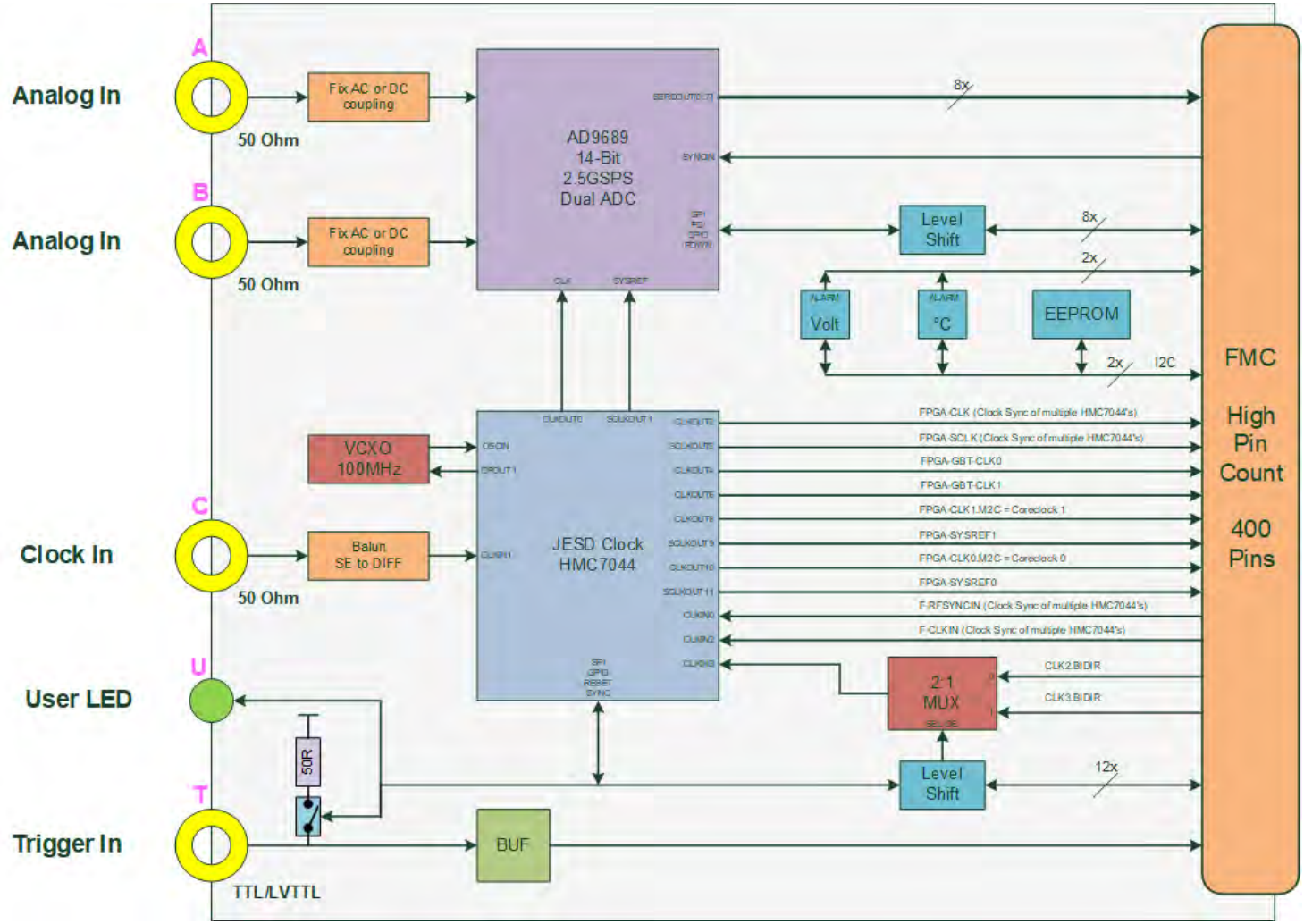
SIS8160 Block Diagram



SFMC01
2 Channel 2.5 GSPS 14-Bit

- Single width, 10mm stacking height, air cooled commercial grade HPC FMC Module
- Analog front-end factory configurable for DC- or AC (Balun) input coupling
- Up to 5 GHz AC Analog BW
- Up to 1 GHz DC Analog BW
- Dual channel 14-Bit, 2.5 GSPS with JESD204B Interface
- 50 Ohm Input Termination
- 4 Front panel SMA Inputs for Analog A/B, Clock and Trigger
- Ultra low phase noise 100 MHz on board clock source
- High performance jitter attenuating frequency generator for JESD204B
- one green Front panel user LED
- System management EEPROM and Temperature Sensor with Thermal Watchdog

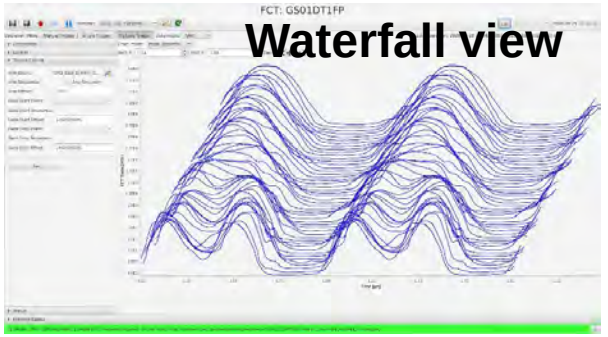
SFMC01
2 Channel 2.5 GSPS 14-Bit

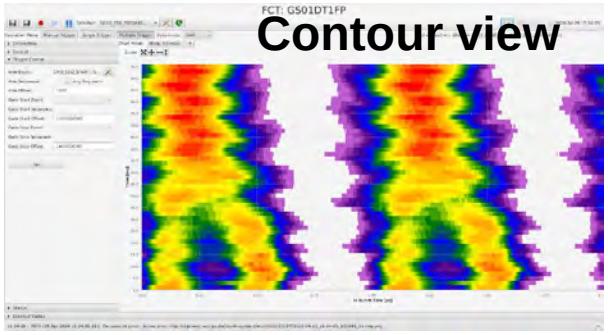


Initial Application: FAIR Fast Current Transformer (FCT) System

Front End Electronics

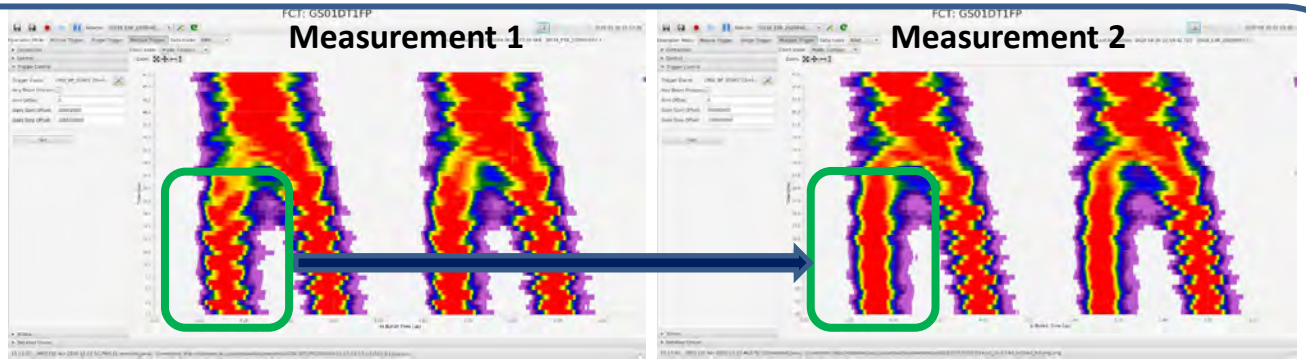
- operational at SIS18 and ESR
- state-of-the-art DAQ based on µTCA
- 2.5 GSa/s, 14-bit ADC
- rf-triggered multi-event acquisition (programmable rate divider for long acqusition times in development by BEA)
- DAQ and operator GUI by BEA





SIS18 FCT

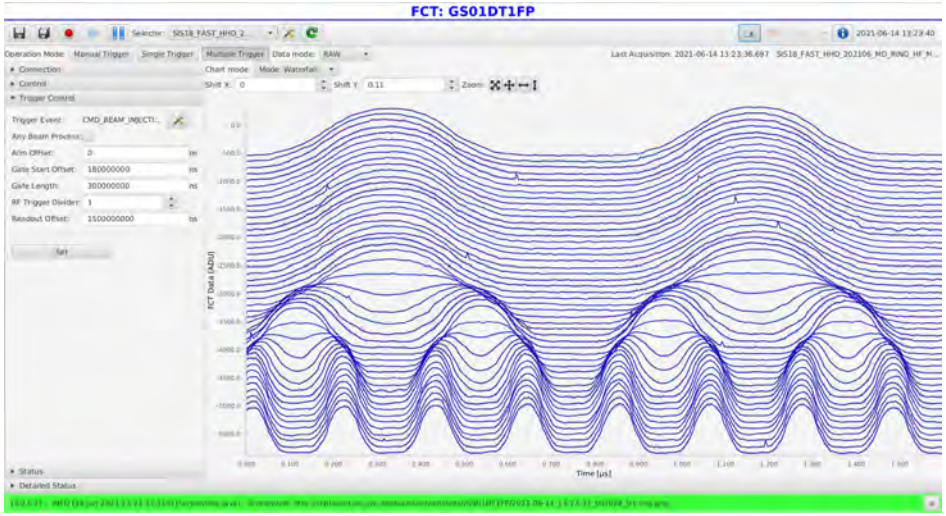
FCT is used for optimization of the „bunch merging 4→2“ process:
cancelling bunch oscillations



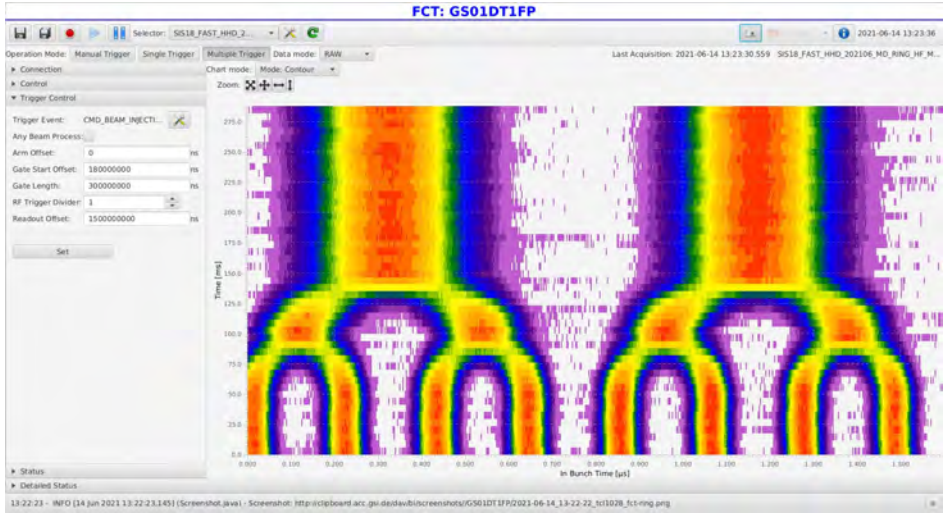
Measurement of fully optimized Multi-step bunch merging procedure:

8 (bunches) → 4 → 2 → 1 (bunch)

Waterfall view



Contour plot view



Courtesy Tobias Hoffmann GSI

SIS8160 Industrial Byproduct Avionics Simulation-/Testbench

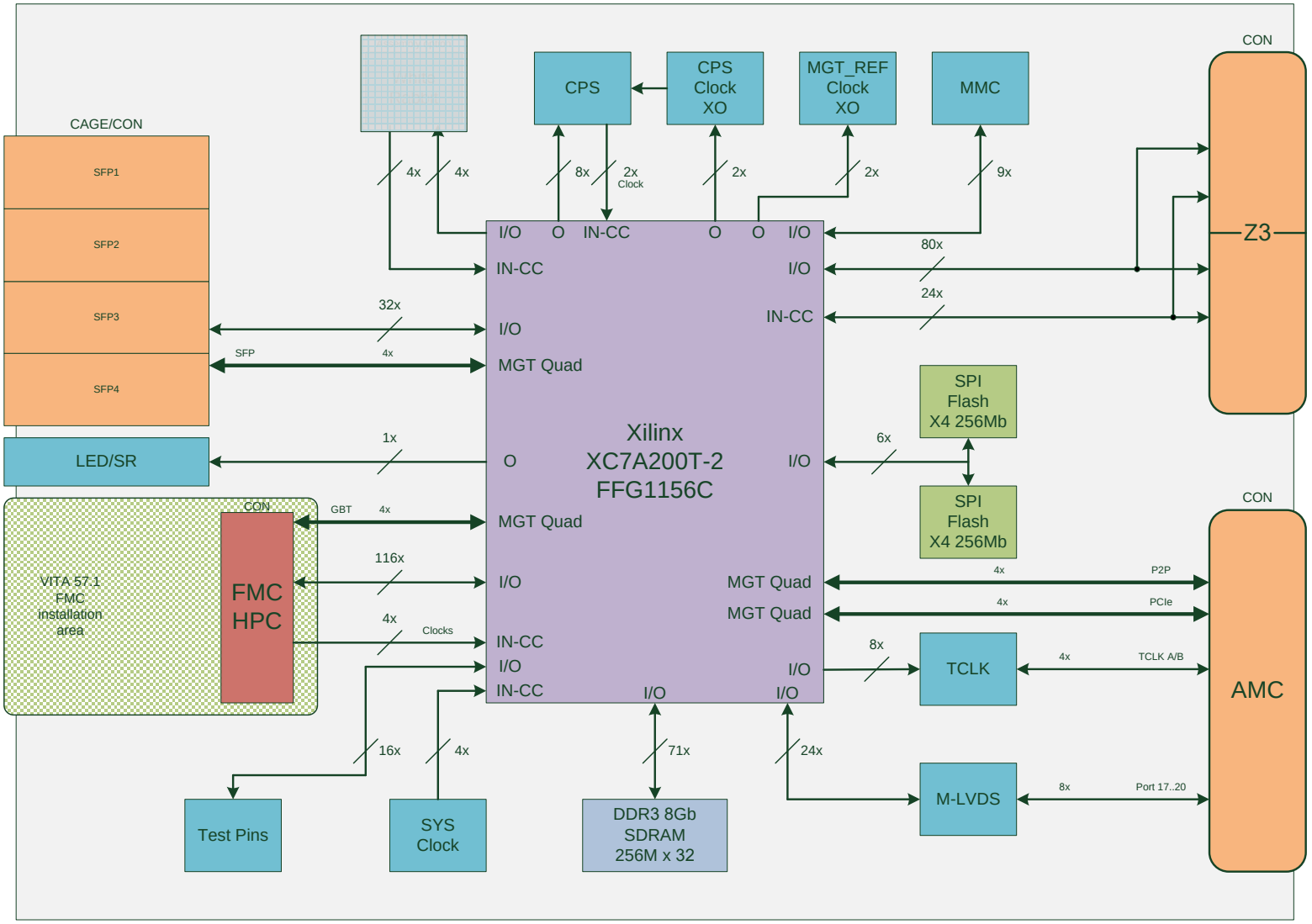
Note:
Monolithic front panel rather than FMC bezel solution (EMI)

SIS8172 Artix-7 Based FMC Carrier Properties

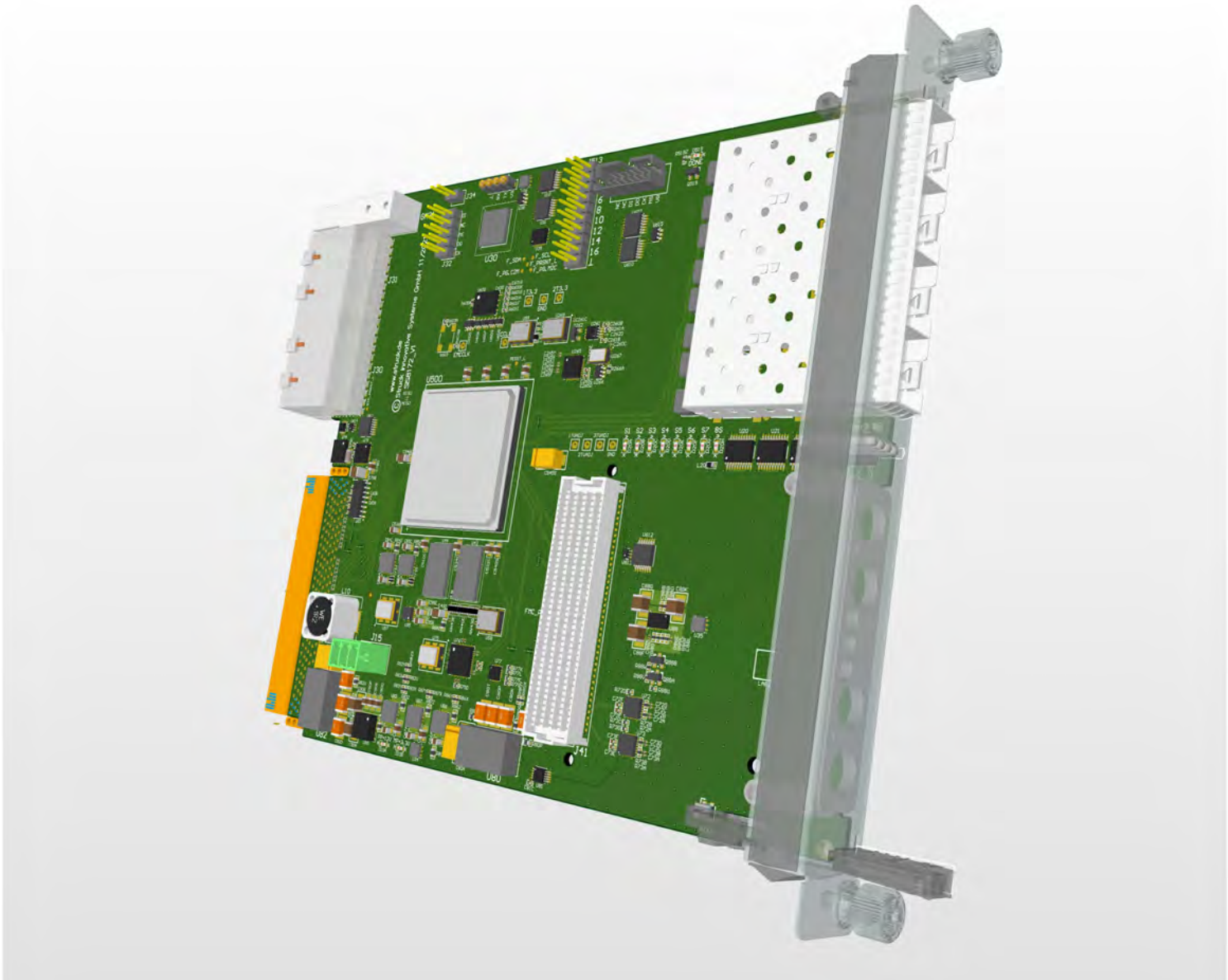
- MTCA.4 AMC with Double Width Mid-Size Form Factor
- Mid cost FPGA (XC7A200T-2FFG1156C)
- 256 M x 32 Bit DDR3 Memory (Artix-7 Limitation)
- 4 Lane PCIe Gen2 (Artix-7 Limitation)
- Dual FPGA Configuration Flash
- Quad SFP+ Cage
- HPC FMC Site
- Zone 3 Class D1.0 Implementation
- 4 Point to Point Link Backplane Interface
- 4 AMC Ports MLVDS (8 MLVDS lines)
- White Rabbit Timing Option
- Module Management Controller ATxmega128A1U, IPMB-L Interface
- DESY MMC1.0 (under LV 91)

Status: Layout in progress

SIS8172 Artix-7 Based FMC Carrier Block Diagram



SIS8172 Artix-7 Based FMC Carrier
Artist‘s View



Possible SIS8172 Target Applications

RTM/Zone 3 Applications

- Beam Loss Monitor (BLM)
- Machine Protection System (MPS)
- PETRA 4 HF Movement Monitor
- PZT4 Piezo Controller (Low Level Radiofrequency)
- …

FMC Applications

- DOSIMON (Dosimetry, XFEL MPS)
- MOTDRV22 (Low Level Radiofrequency)
- Analog Input (Synchrotron Beamline Spectroscopy)
- Digital I/O (Synchrotron Beamline Multiscaler)
- …

In General: AMC for Cost Sensitive Applications

Supply Chain Woes I
Lead Times

XC7A200T-2FFG1156C

XILINX

Enlarge

Mouser No:	217-7A200T-2FFG1156C
Mfr. No:	XC7A200T-2FFG1156C
Mfr.:	Xilinx
Customer No:	Customer No
Description:	FPGA - Field Programmable Gate Array XC7A200T-2FFG1156C
Datasheet:	XC7A200T-2FFG1156C Datasheet (PDF)

Availability

Stock:	0 Notify me when product is in stock. You can still purchase this product for backorder.
On Order:	22 Expected 22/09/2022 77 View Expected Dates
Factory Lead Time:	58 Weeks

Long lead time reported on this product.

Some Xilinx FPGA families will likely not ship at all in 2022 (Spartan-6, Virtex-6)

Manufacturer Part Number	Manufacturer	Customer Part Number	Price (EUR)	Quantity	Inventory	Pipeline/Quantity	Lead Time	RoHS	Additional Info
TPS82140SILT Module DC-DC 12VIN 1-OUT 0.9V to 6V 2A 8-Pin uSIP SMD EP T/R	Texas Instruments	Customer Part: None	250+ €2.42937 750+ €2.26491 Arrow Purchasing Currency: USD	Min. Qty 250 ADD TO CART	Public 0 Buffer 0 Multiple 250 SPQ 250	2023-02-15 - 6750	64 Weeks		

Supply-chain problems will last through 2023, Intel chief says

https://www.livemint.com/technology/tech-news/supplychain-problems...

Vor 20 Stunden · **Supply-chain** problems will last through **2023**, Intel chief says Premium Intel intends to continue doing most of its chip making at its own plants (Photo: AFP) 2 min read....

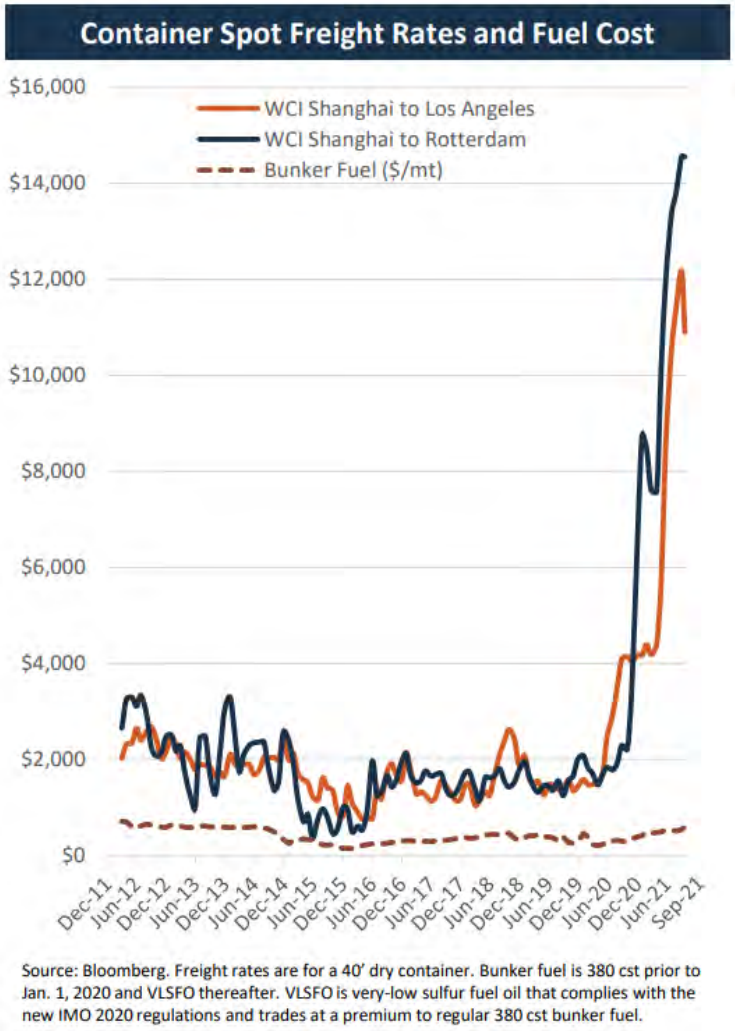
→ Expect a tough ride in 2022 (what is not on order yet may be hard to ship)

Supply Chain Woes II
Pricing

- Xilinx +20% (November 2021)
- Analog Devices +10,…,+40% (Nov/Dec 2021)
- Texas Instruments unclear > 10% (TPS82140SIL e.g.)
- Schroff +3,5% (Jan ´21) + 4-6%(Sep ´21)
- Skyworks/SiLabs +30% (November 2021)
- Harting +6,8% (February 2022)
- EMS house +11% (November 2021)

→ Grey Market risk paired with 10-fold price not unusual

Supply Chain Woes III
Freight Rates+Packaging



Source: Bloomberg. Freight rates are for a 40' dry container. Bunker fuel is 380 cst prior to Jan. 1, 2020 and VLSFO thereafter. VLSFO is very-low sulfur fuel oil that complies with the new IMO 2020 regulations and trades at a premium to regular 380 cst bunker fuel.

Source SCA Q3/2021 presentation
→ Impact on wooden shipping boxes and packaging materials in general

Questions/Discussion