Readout Electronics for Silicon Photomultipliers

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Outline

- General Readout Requirements of SiPMs
  - electrical
  - others
- Existing chips & motivation for new design
- Application Specified Designs
  - high energy physics
  - medical application

Readout Requirements of SiPMs

- ✓ Electrical

  relative low noise : O(10^5) , pixel size dependent

  large dynamic range : 40fC (pixel charge) – 200pC (pixel number)

  $\log_2$(max/min) 13 – 14 bits

  fast rise time : ~2ns , ToF capable

  bias tune : all devices same gain , gain propotional to overvoltage

  (SiPM $V_{bias} = V_{power} - V_{chip}$, V_{chip} is tunable)

- ✓ Other

  limited power consumption :

  cooling free large system (calorimeter)

Motivation of New SiPM r/o chip design

Trip-t *for MPPC in T2K neutrino experiment*
J. Estrada, *et al.*, MCM II and the Trip Chip, D0 Note 4009 (2002).
Originally designed for D0
drawbacks : no bias tune, limited dynamic range

BASIC
F. Corsi et al. BASIC: An 8-channel front-end ASIC for Silicon Photomultiplier detectors , IEEE NSS Record 2009
drawbacks :dynamic range (< 100pC) , power

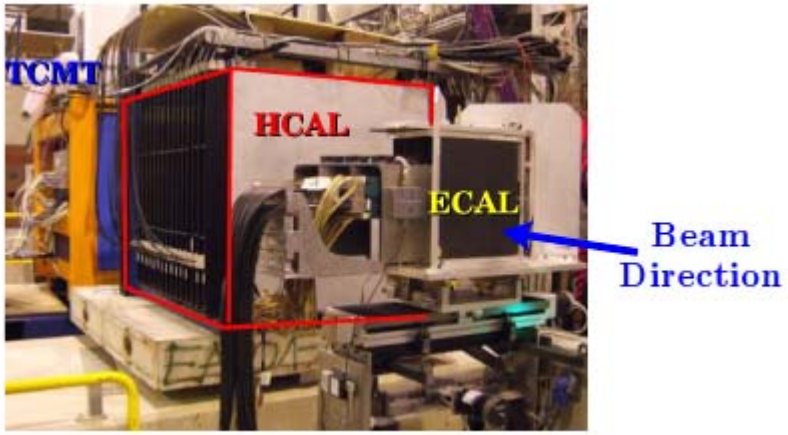
SPIROC *for CALICE AHCAL*
S. Callier et al. Silicon Photomultiplier integrated readout chip (SPIROC) for the ILC: Measurements and possible further development , IEEE NSS Record 2009
drawbacks : S/N for low gain SiPM , timing

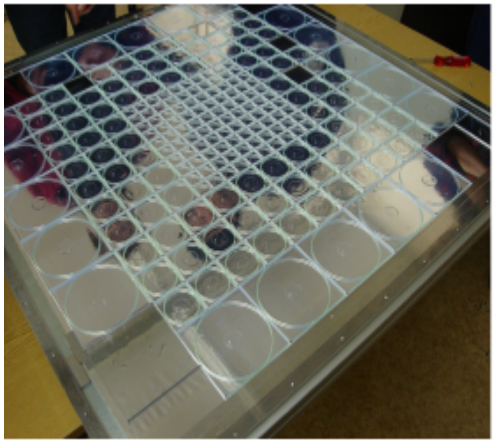
NINO *for ALICE MRPC (used for Timing)*
Anghinolfi et al , NINO: an ultrafast low-power front-end amplifier discriminator for the time-of-flight detector in the ALICE experiment , IEEE Transanctions on Nuclear Science, Vol 51
drawbacks : power , bias tune

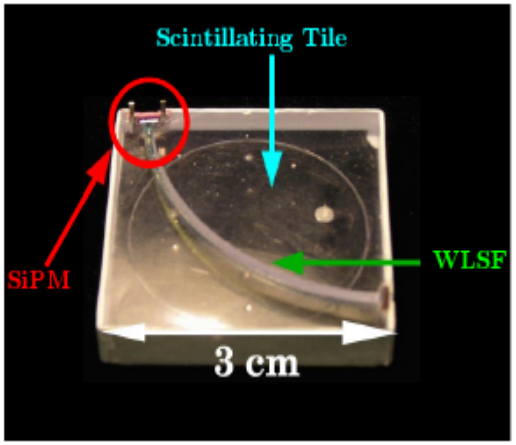
New design needs bias tune, large dynamic range, high S/N , timing , power

Special Applications - i

- High granularity Power limited Readout

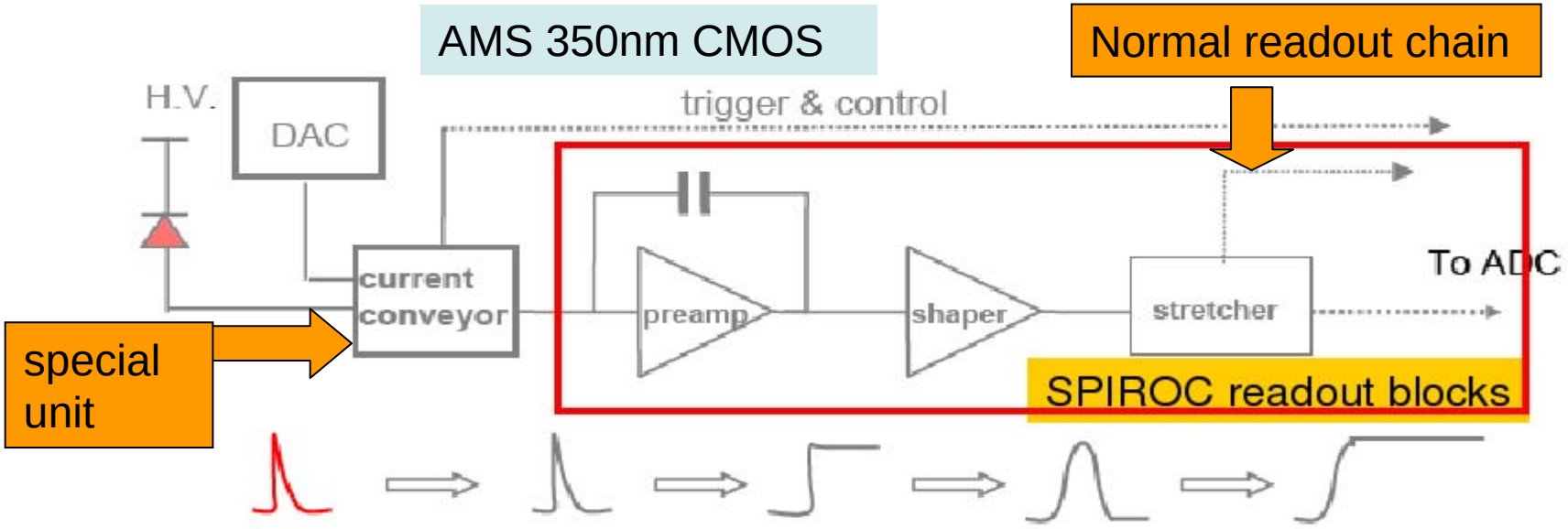






- **relative low noise (resolve pixel spectrum)**
- **large dynamic range (factor 5000 , ~13 bits)**
- **bias tune (SiPM breakdown variation 2-5 V)**
- **power pulsing , 1% duty cycle (explain later)**

KLauS - Kanäle für Ladungsauslese von SiPM



Measured feature :

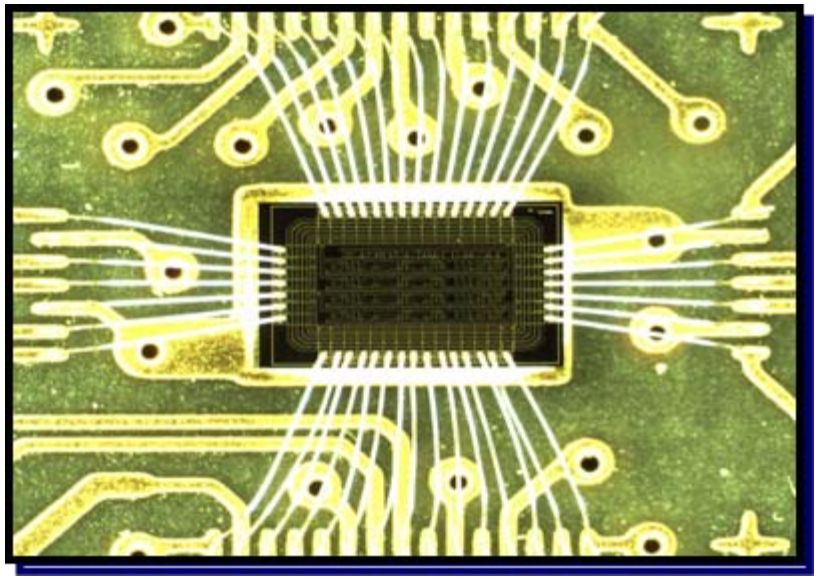
2V bias tuning capability

dynamic range up to 150pC

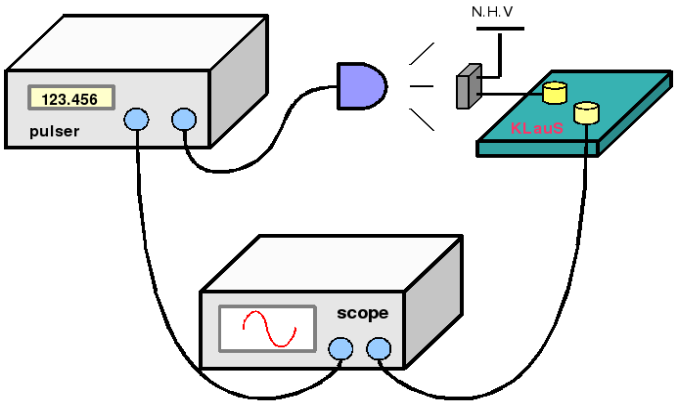
S/N > 10 for 2.5 x 10^5 gain

pixel timing 260ps

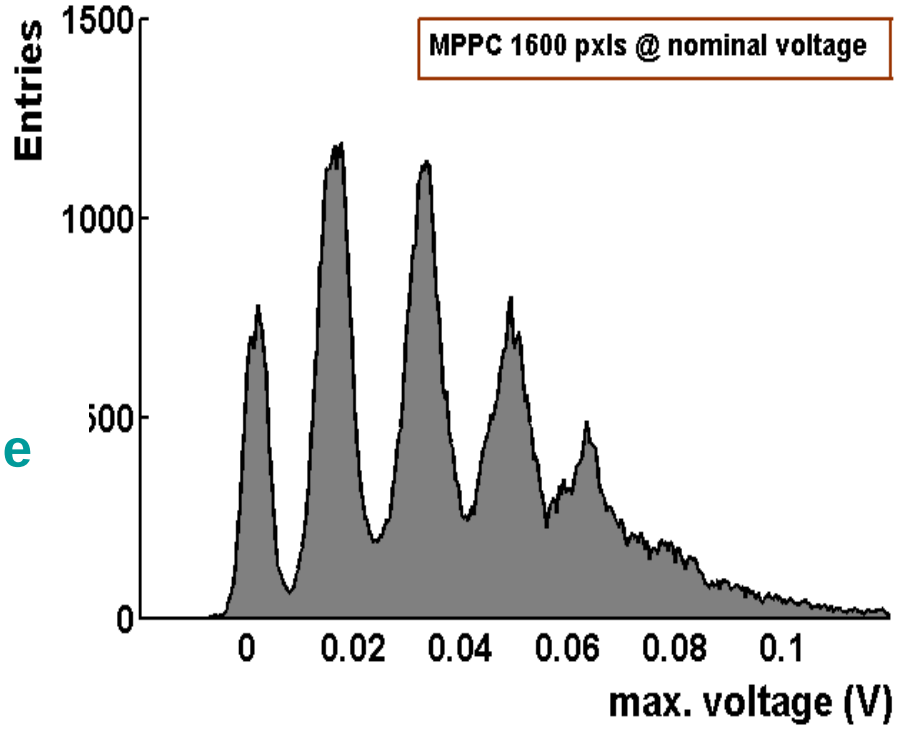
Plan to Replace SPIROC analog part



Results of KLauS – i



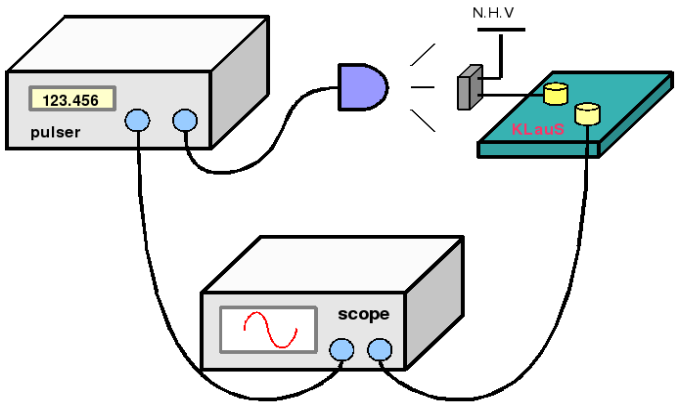
Test setup with LED
Measurement with Visible Photon



sgl. photon spectrum

max voltage proportional to charge

Results of KLauS – ii



LED tuned to fire only few pixels

Pixel timing jitter much smaller than walk

$$\sigma_{MIP} = \sigma_{pxl} / N_{fired}$$ (N > 10 for M.I.P.)

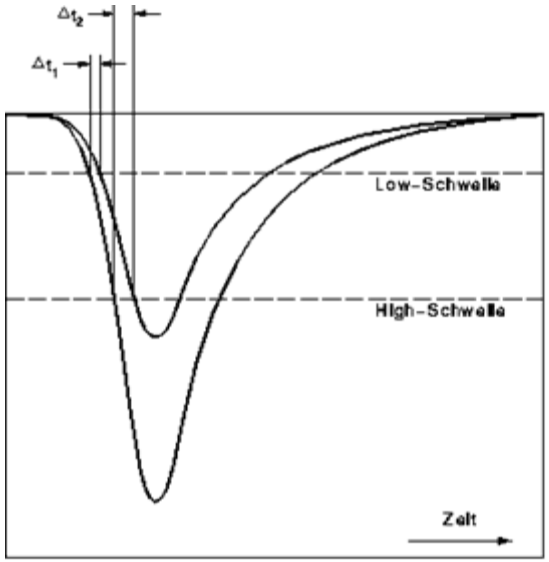
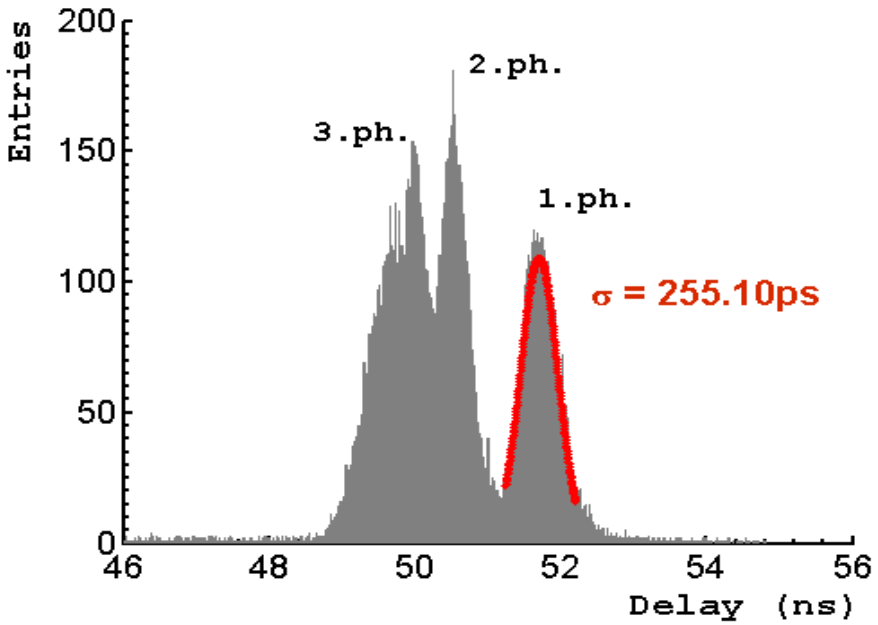
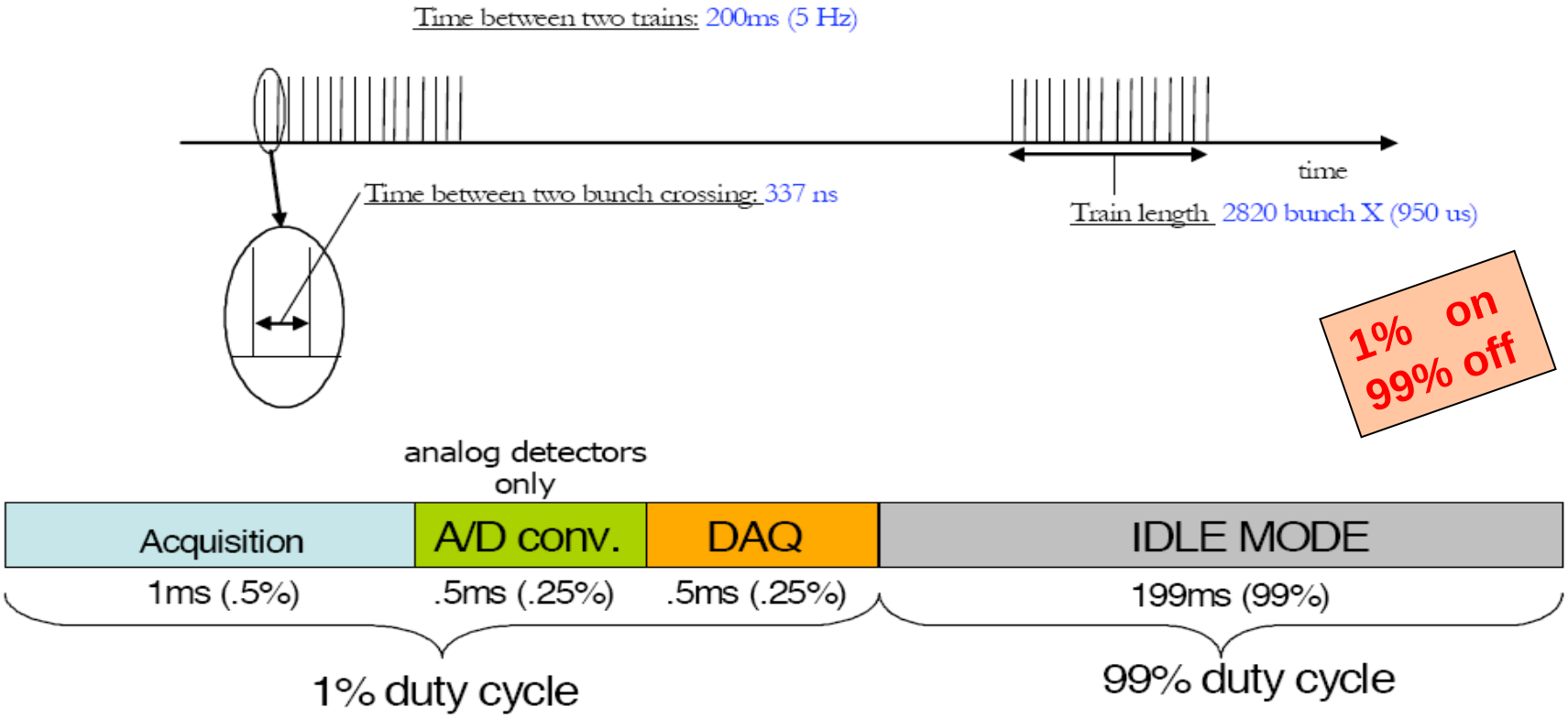


Abb. 15: Abhängigkeit des Time-Walk von der Diskriminatorschwelle



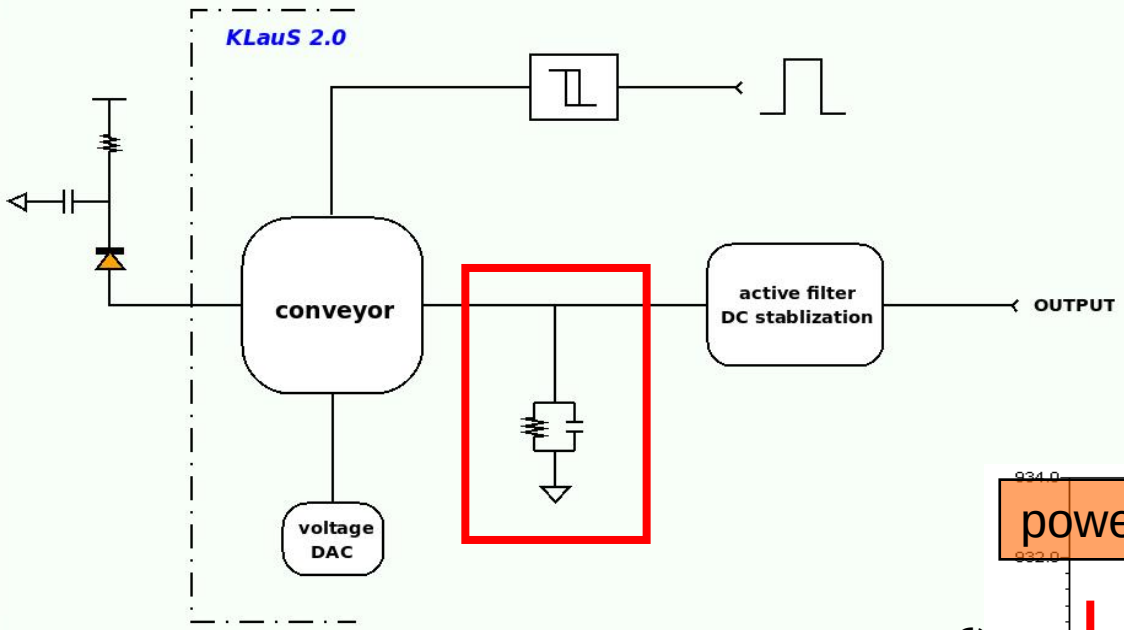
ILC beam structure & Power Pulsing



switch down electronics :

meanwhile keep the SiPM bias voltage at all times

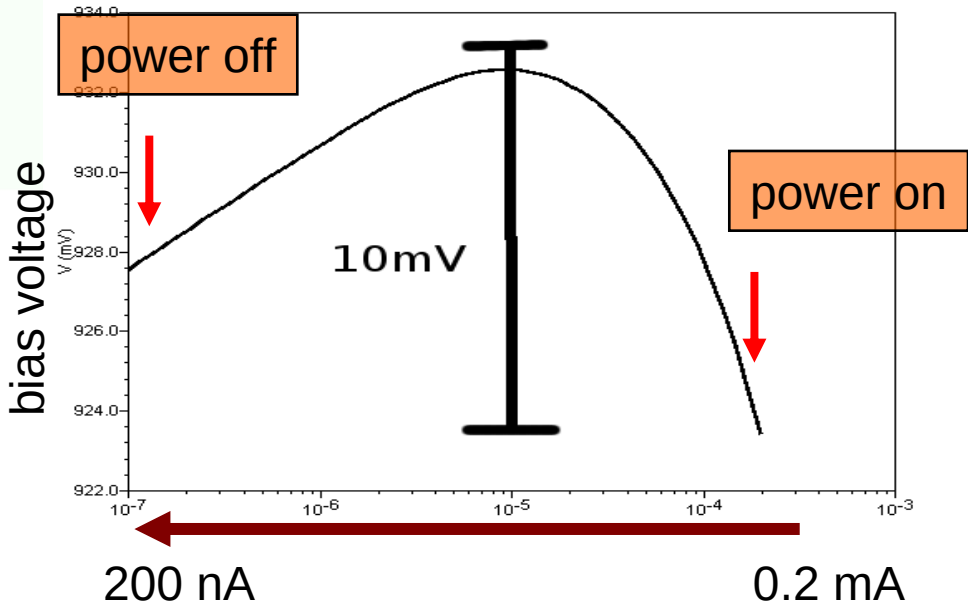
Upgrade - KLauS 2.0



channel with low power feature

- **leave out preamplifier**
- **power pulsing < 25 µ W / ch**

  power on ~ 1.5mW / ch



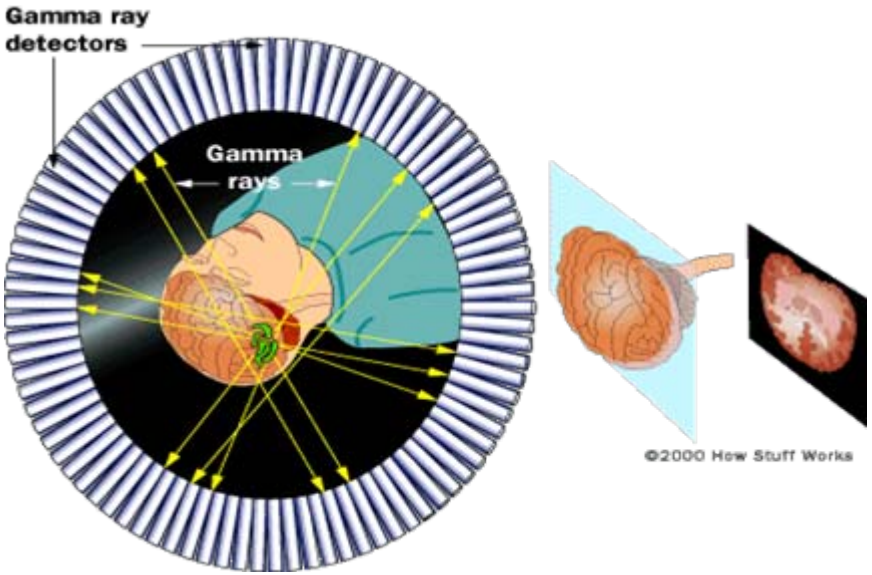
from " on " to " off "

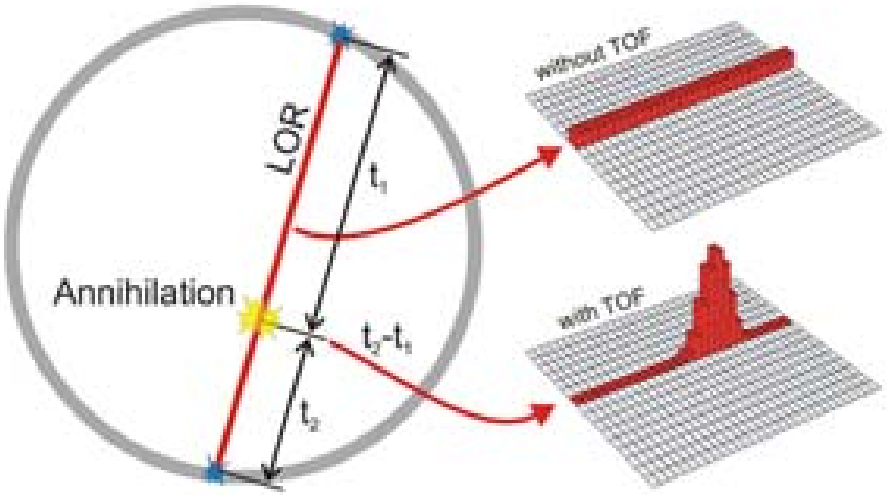
bias voltage 10 mV change

submission in Nov. @ 2010

Special Applications - ii

- High Timing Resolution



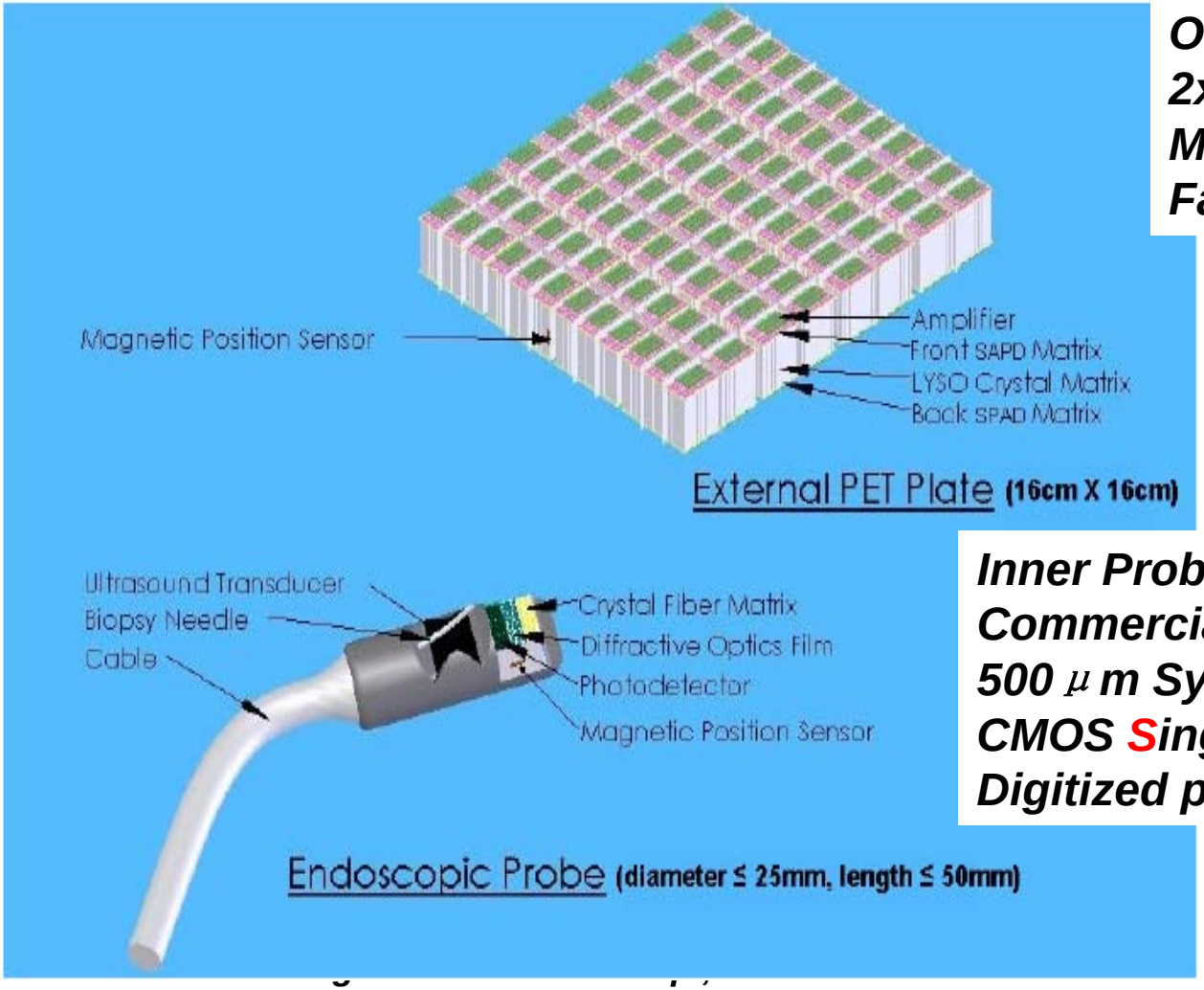


ToF PET to improve spacial resolution

SiPM in EndoToF PET project

Ultra-Sound Endoscope + ToF PET

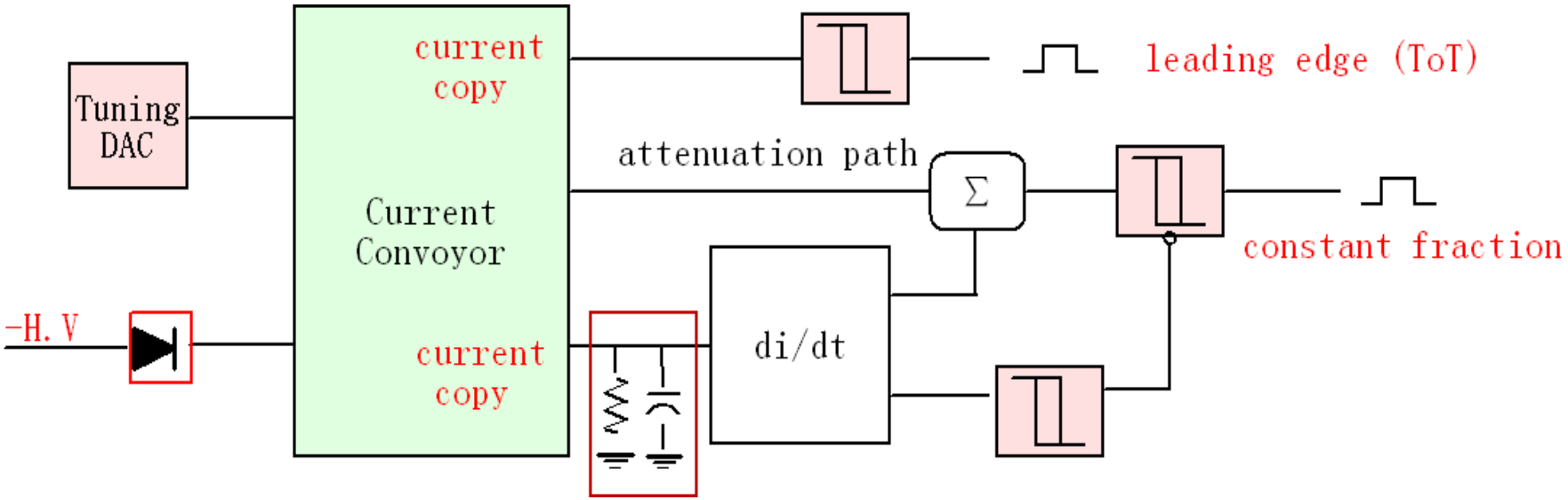
200 ps resolution, 3cm spatial resolution



Outer Plate :
2x2x20mm Crystal
MPPC 50 μm pixel
Fast Discrimination + TDC

Inner Probe :
Commercial Ultra Sound Probe
500 μm Syntillation Fiber
CMOS Single Photon Avalanche Diode
Digitized photon counting signal

STiC - SiPM Timing Chip

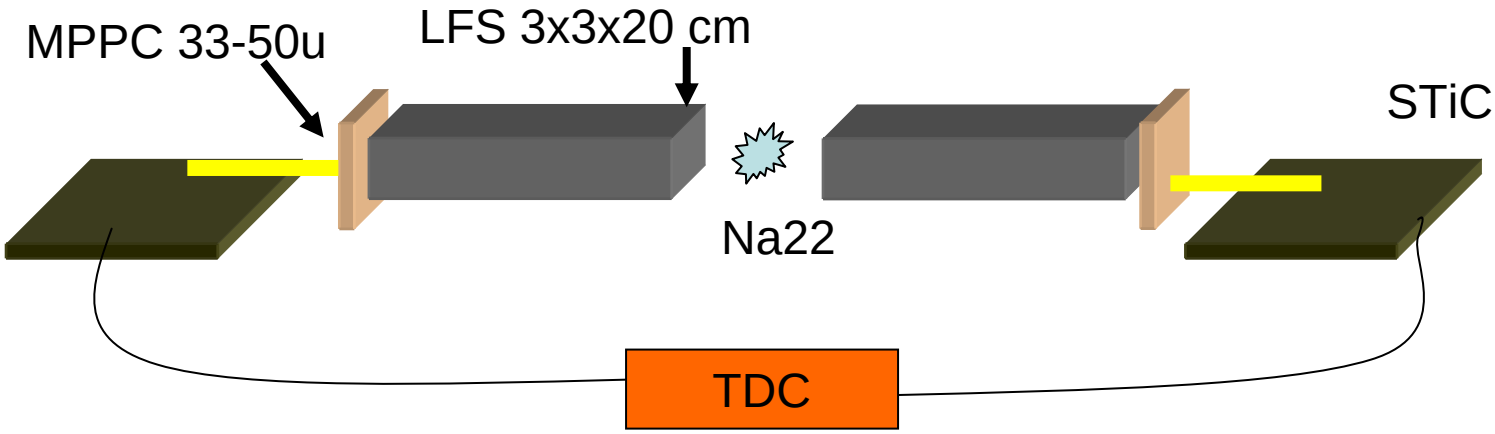


AMS 350nm CMOS prototype

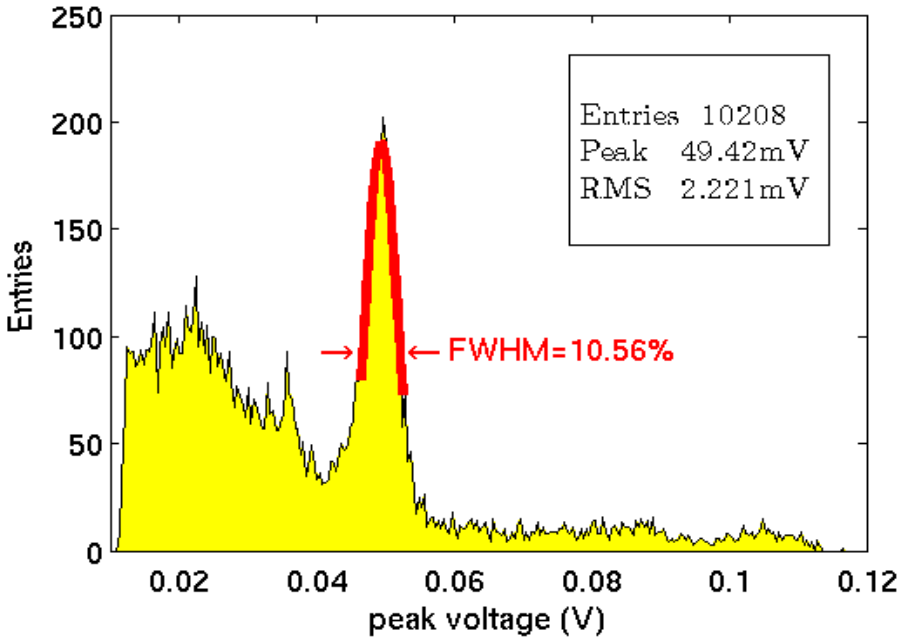
Leading Edge and Constant Fraction timing method

charge measurement compatible with components highlighted

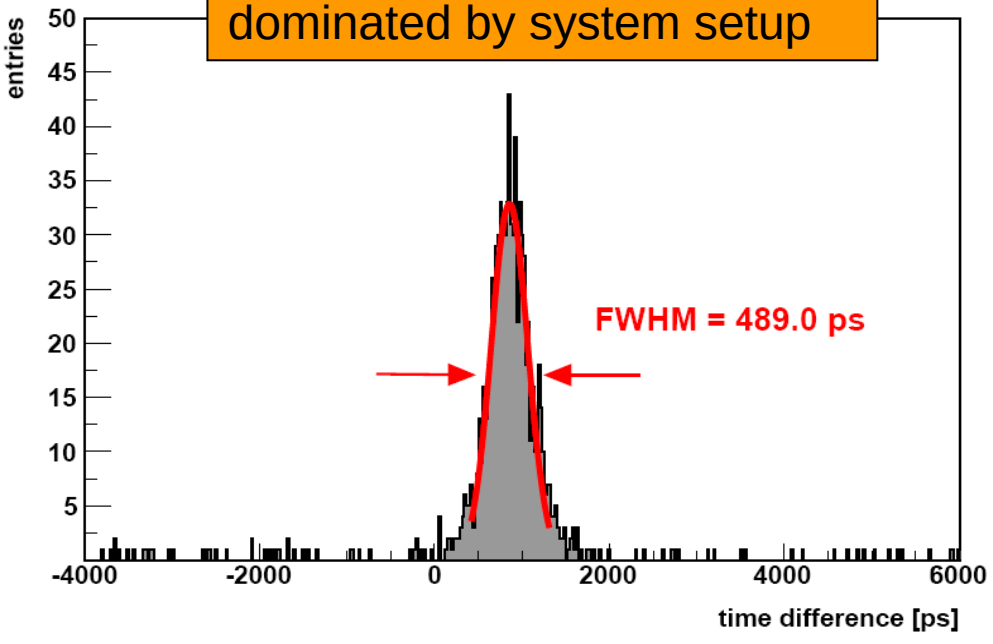
Results of STiC



Energy resolution 11%



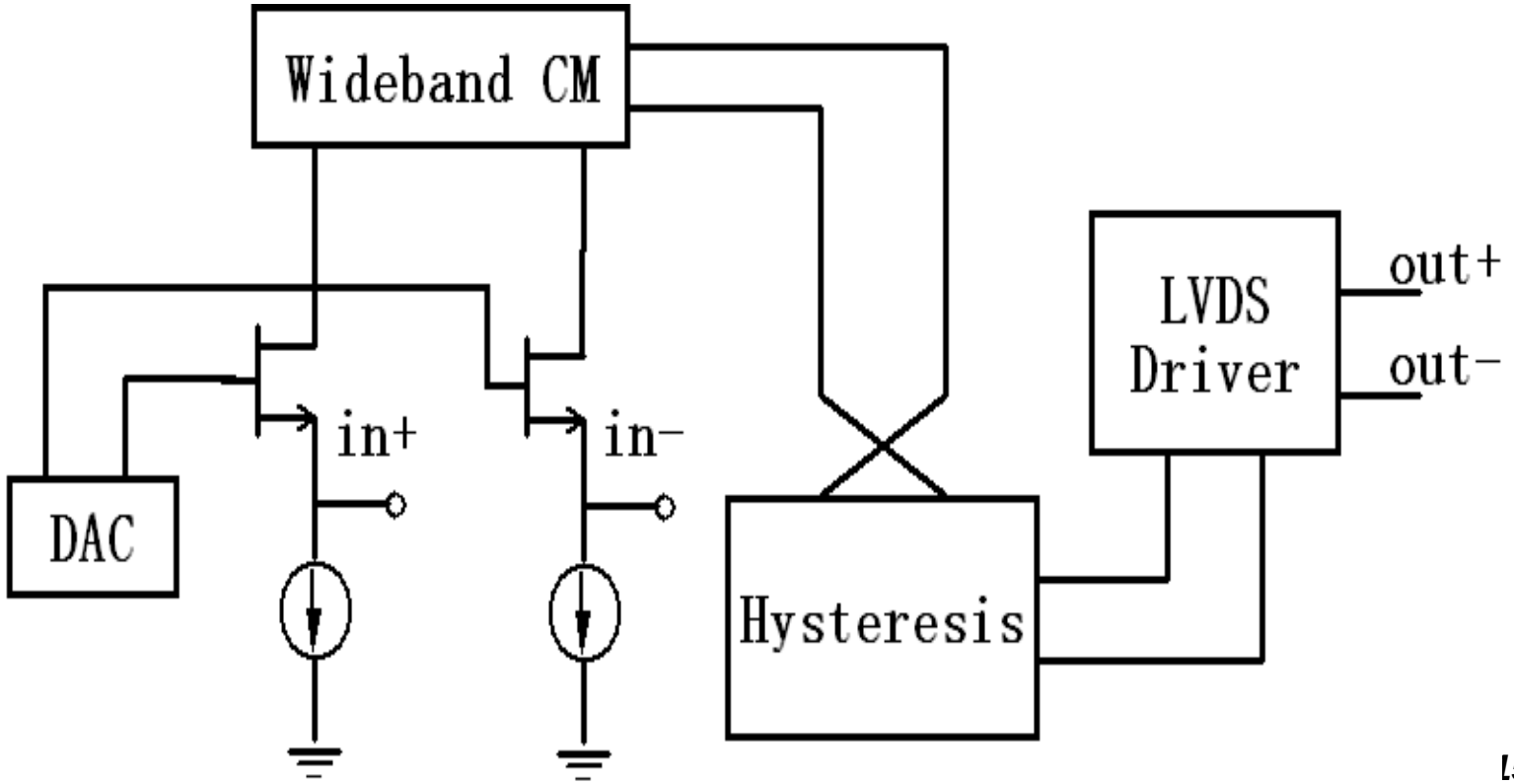
Coincidence resolution 490ps
dominated by system setup



STiC 2.0

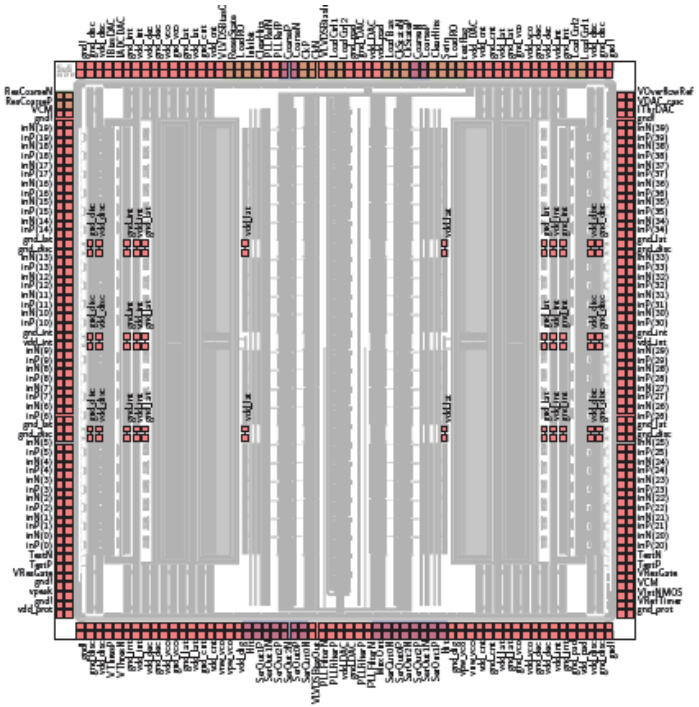
- **LSO + MPPC 3x3 50 μ m + NINO – 350ps**
  pros of NINO: low impedance, differential
  cons of NINO: no bias tune, large power

STiC upgrade, differential fast discrimination with much less power



The PETA ASICs (Position-Energy-Time-ASIC)

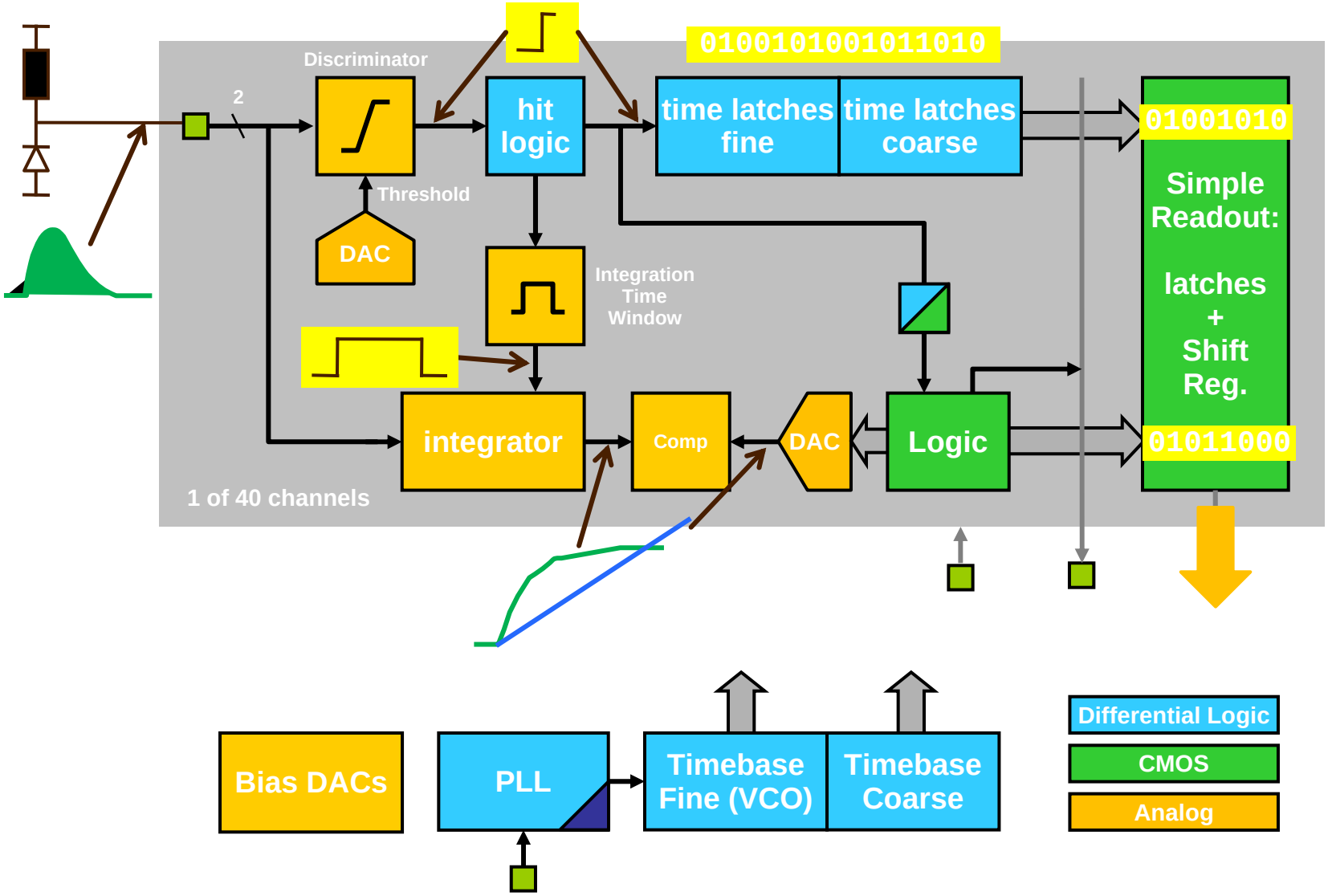
- Is a complete 40 channel SiPM readout system on one chip:
- Amplification (differential voltage amp.)
- Discrimination (per channel threshold trim)
- Time Stamping (50ps bins)
- Integration (self gated, program. int. time)
- Digitization (~8 Bit resolution)
- All digital readout (LVDS handshake)
- Self triggered, asynchronous operation



@ZITI / Uni Heidelberg

- Developed by the group of circuit design, Heidelberg / Mannheim
- (P. Fischer, I. Peric, M. Ritzert) within FP7 EU Project ‘Hyperimage’

PETA Operation



PETA Details

Size: 5 x 5 mm^2

Technology: UMC 180nm CMOS

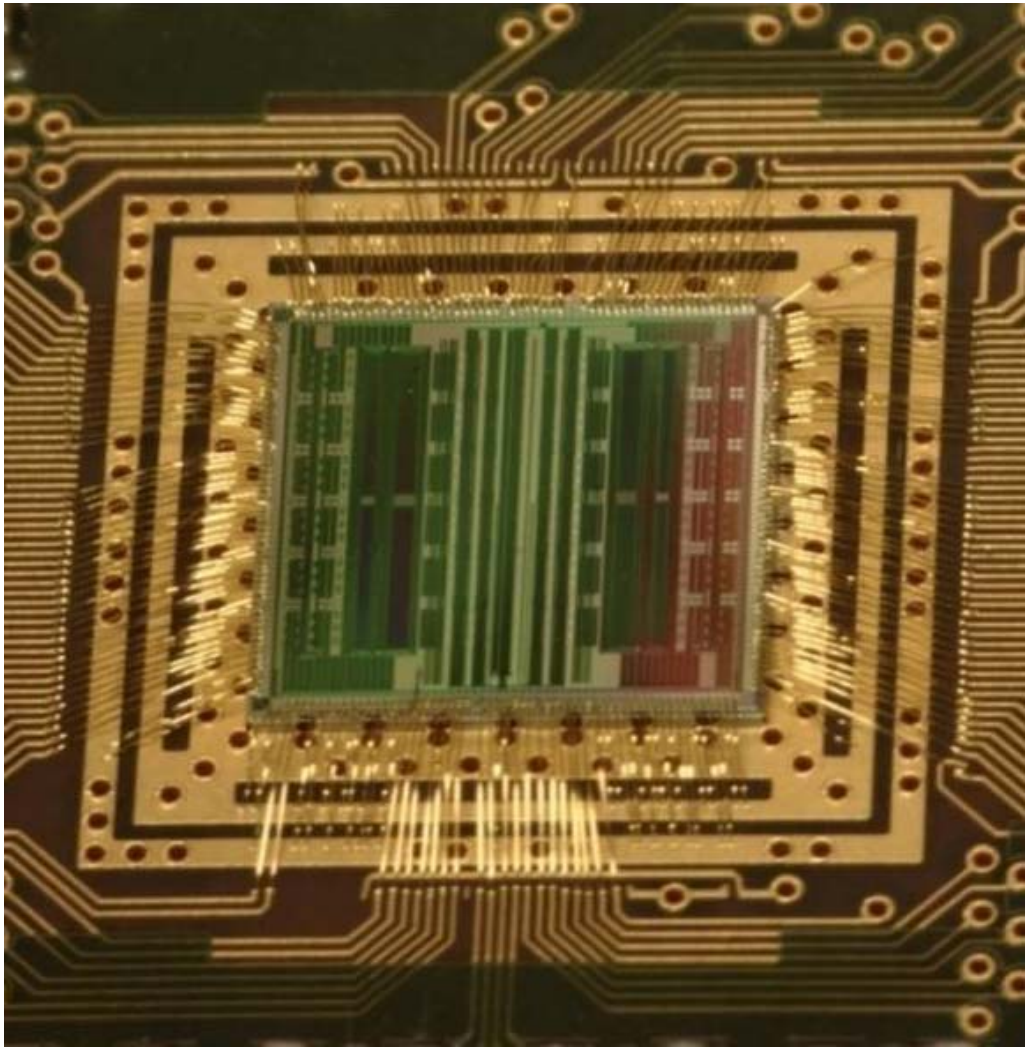
TDC:

- 625 MHz Ref clock for PLL
- σ_t < 20ps (1ch, on-chip)
- σ_t ~ 30ps (ch-ch, chip-chip)

Discriminator:

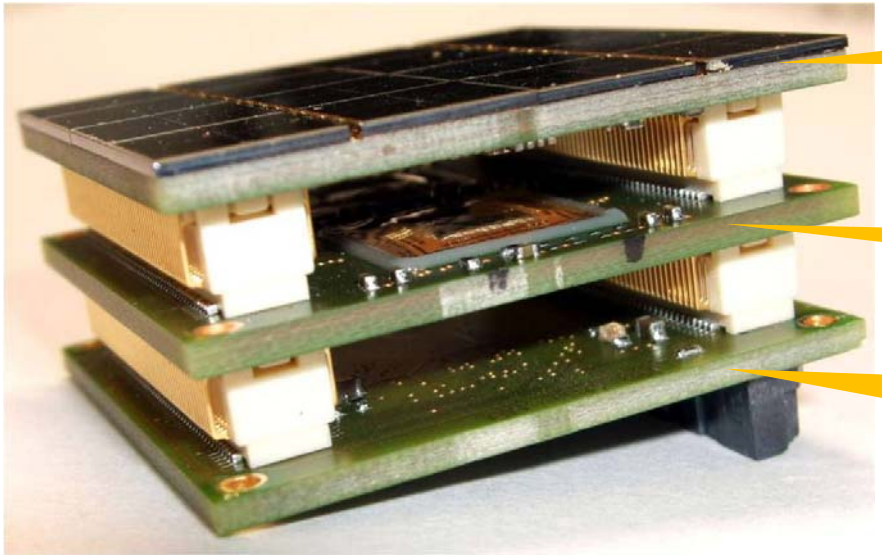
- Voltage noise σ < 200µV
- Thresholds <2mV (lab)

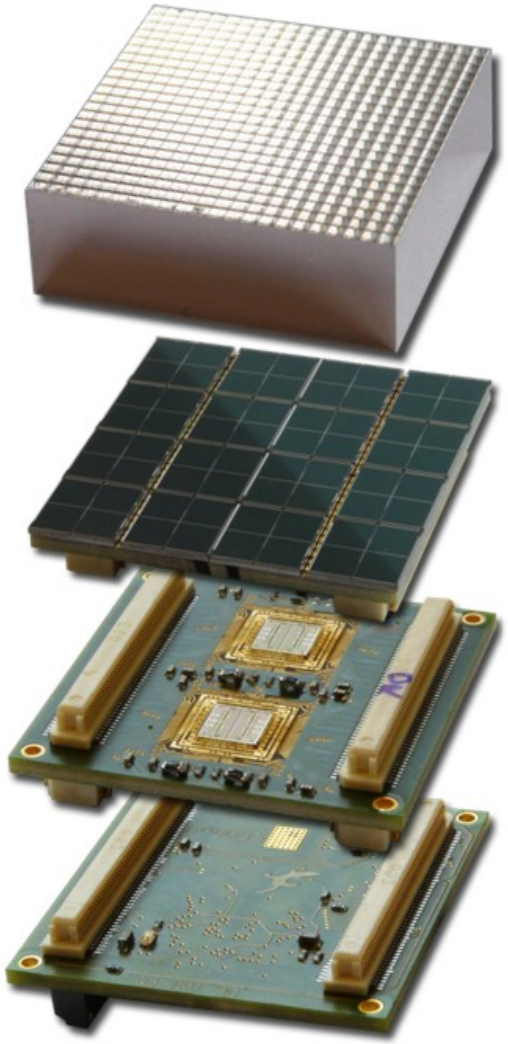
Power: < 30mW / channel



The Hyperimage γ Detection Unit

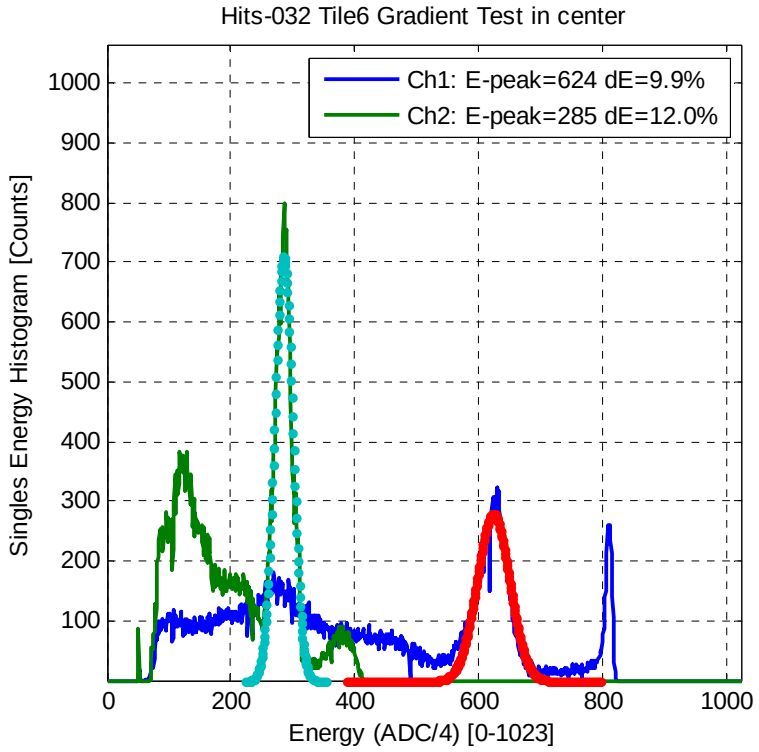
- Crystals + SiPM array + Electronics
- Very compact Multi Channel Design
- 3×3 cm2 active area, very small edge
- 8×8 SiPMs + electronic channels
- Modular design with 3 PCB ‘Tiles’



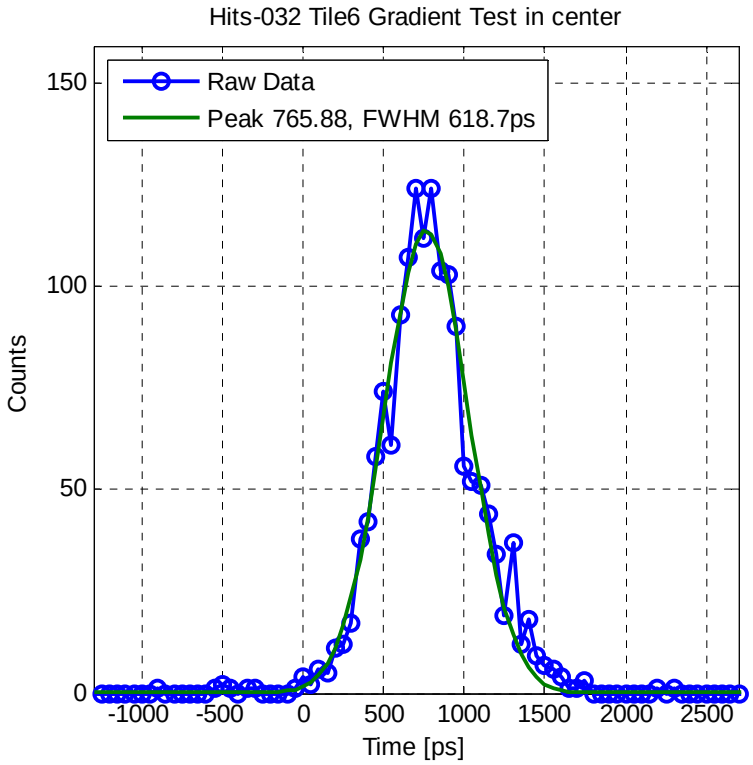


Stack PET Operation (inside RUNNING MRI Scanner)

Module has been successfully operated in MRI



Energy Resolution ~12% (uncorrected)



Timing Resolution ~600 ps (FWHM coinc.)

Single channel elec. jitter 20 ps
coinc. Dominated by system setup

Summary

- **Special requirements for SiPMs**

  large dynamic range
  fast timing
  low power

- **Electronic development to meet SiPM requirements active field**

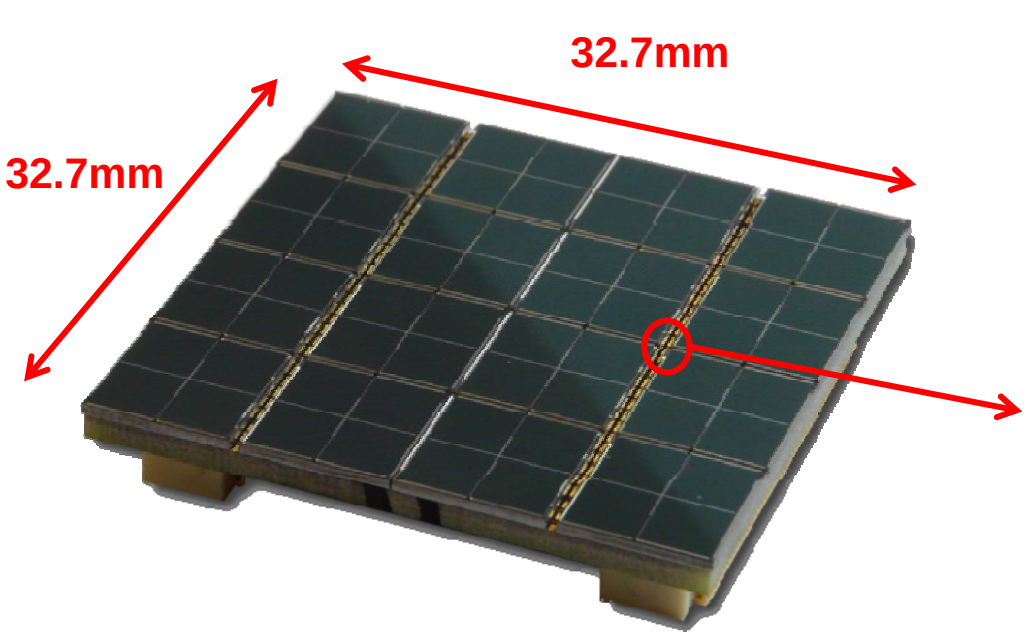
  KLauS (Calorimeter)
  STiC & PETA (Positron Emission Tomography)

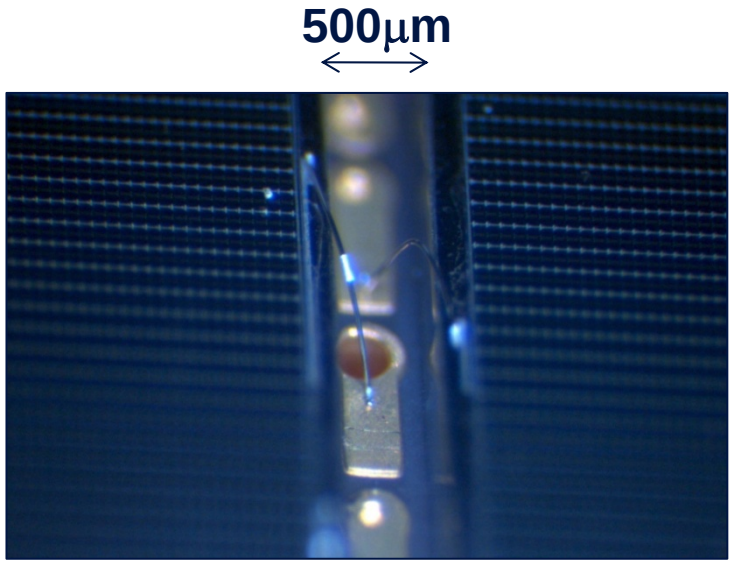
Back up slides

The SiPM Tile Design

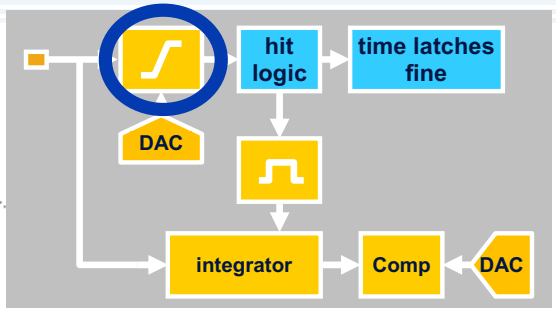
SiPMs by FBK. ‘Quads’: 4 x (4x4mm^2), 50µm^2 cell size

Geometrical fill factor ~ 84% (not including SiPM ff)

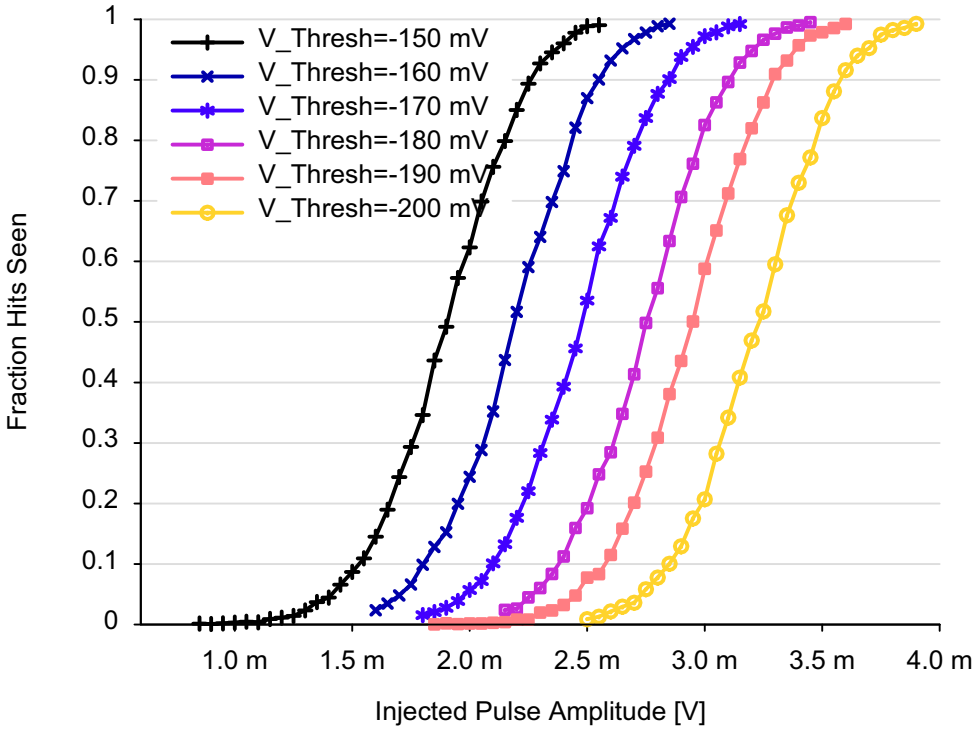




Measurement: Discriminator

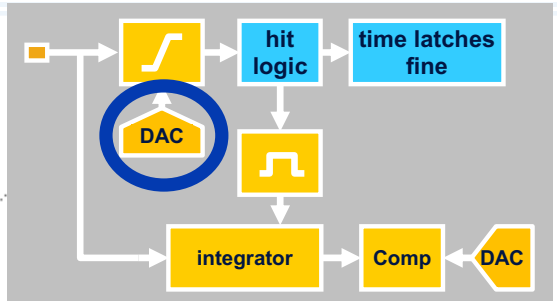


Inject (small) pulses with increasing amplitude.
Channel fires with 50% probability at threshold.



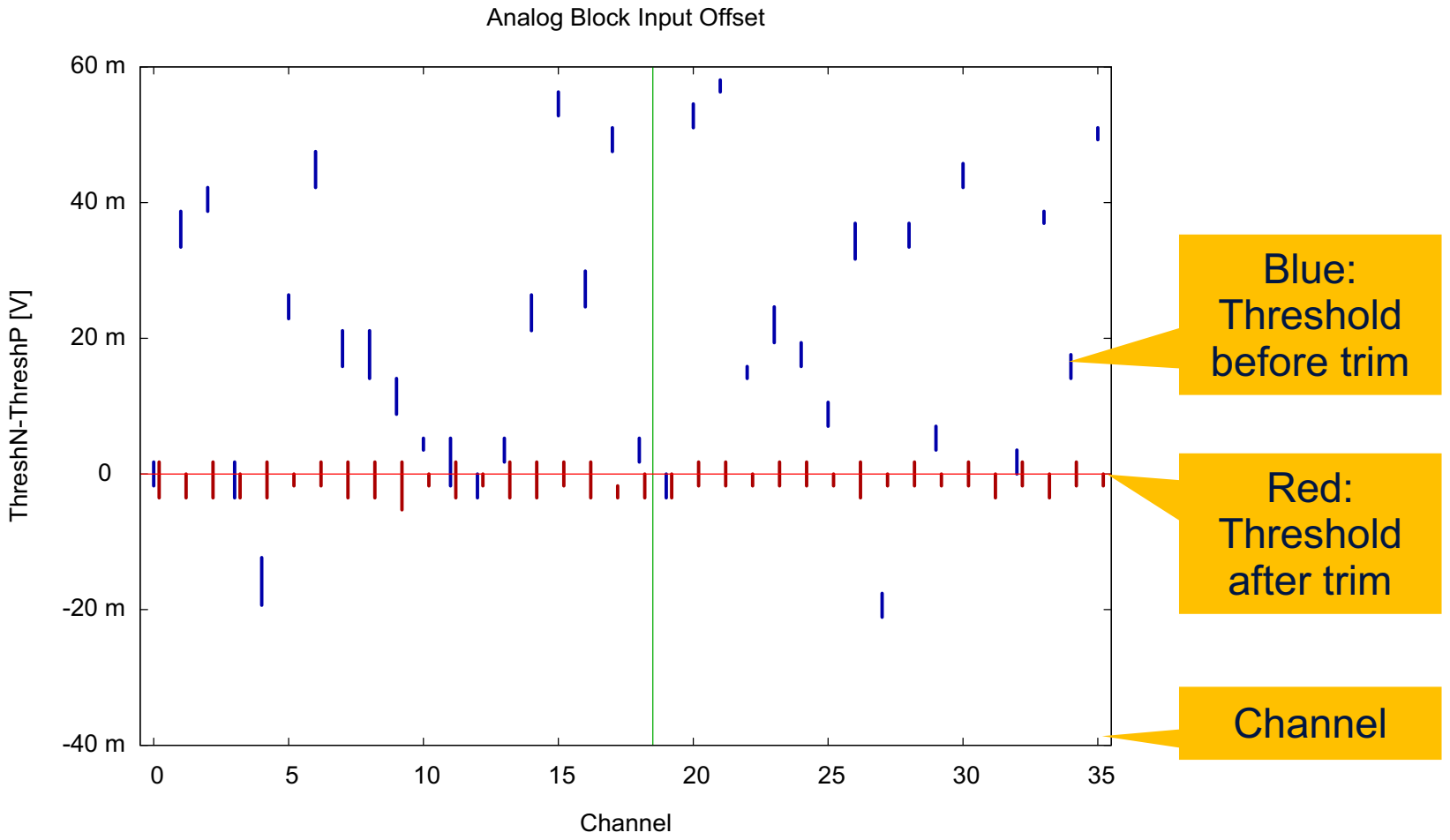
Thresholds as low as 2mV are possible, noise is ~200µV (rms)
Adjustment (Thres. vs. ext. setting) is very linear!

Measurement: Threshold Trim

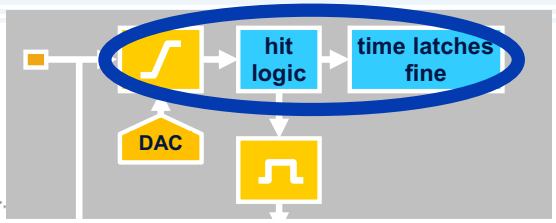


Observed large threshold dispersion in PETA1

Fixed by new trimming scheme in PETA2



Measurement: Time Resolution

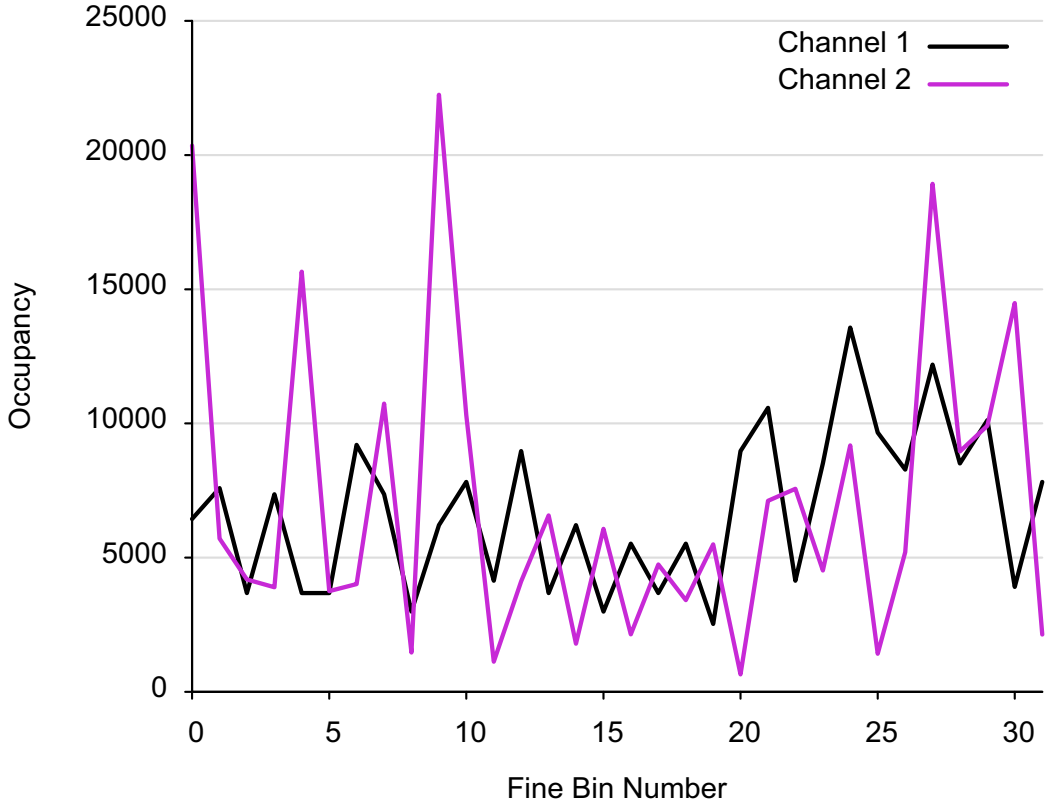


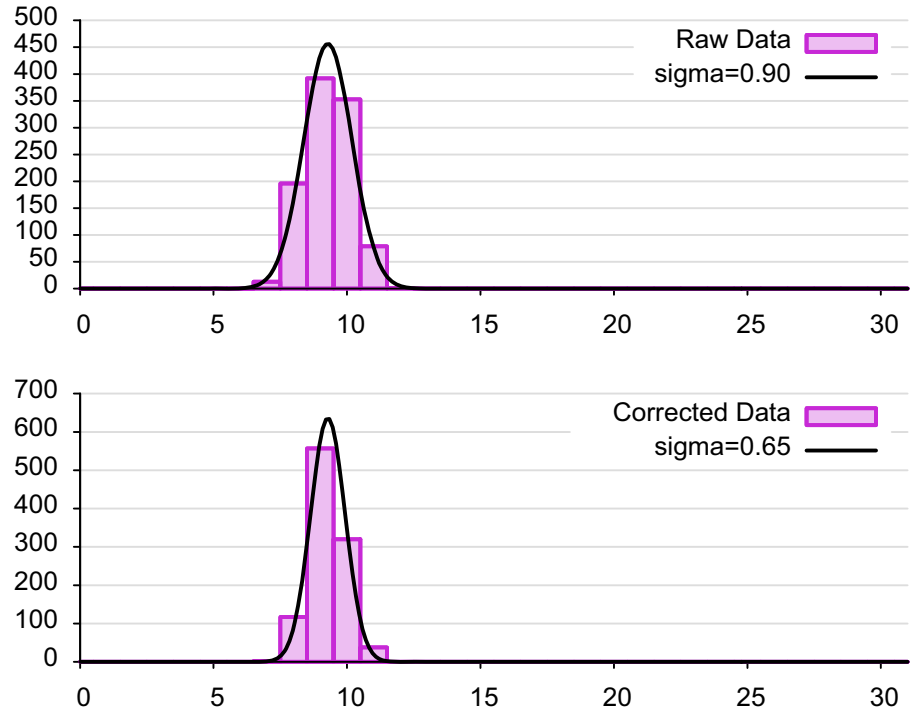
Delay mismatch in VCO leads to unequal hit time distribution

- this is constant over time and characteristic for a chip – 'Fingerprint'

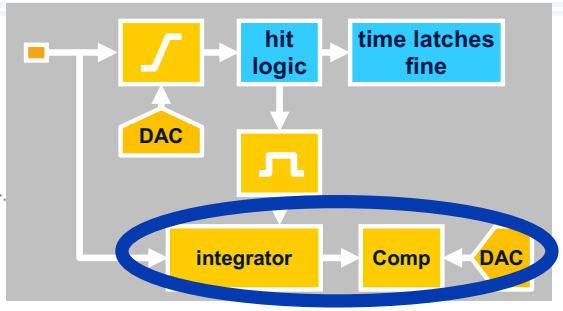
Can be corrected for → improved time resolution

Achieve σ~20ps (single channel). MUCH better than LYSO crystals!





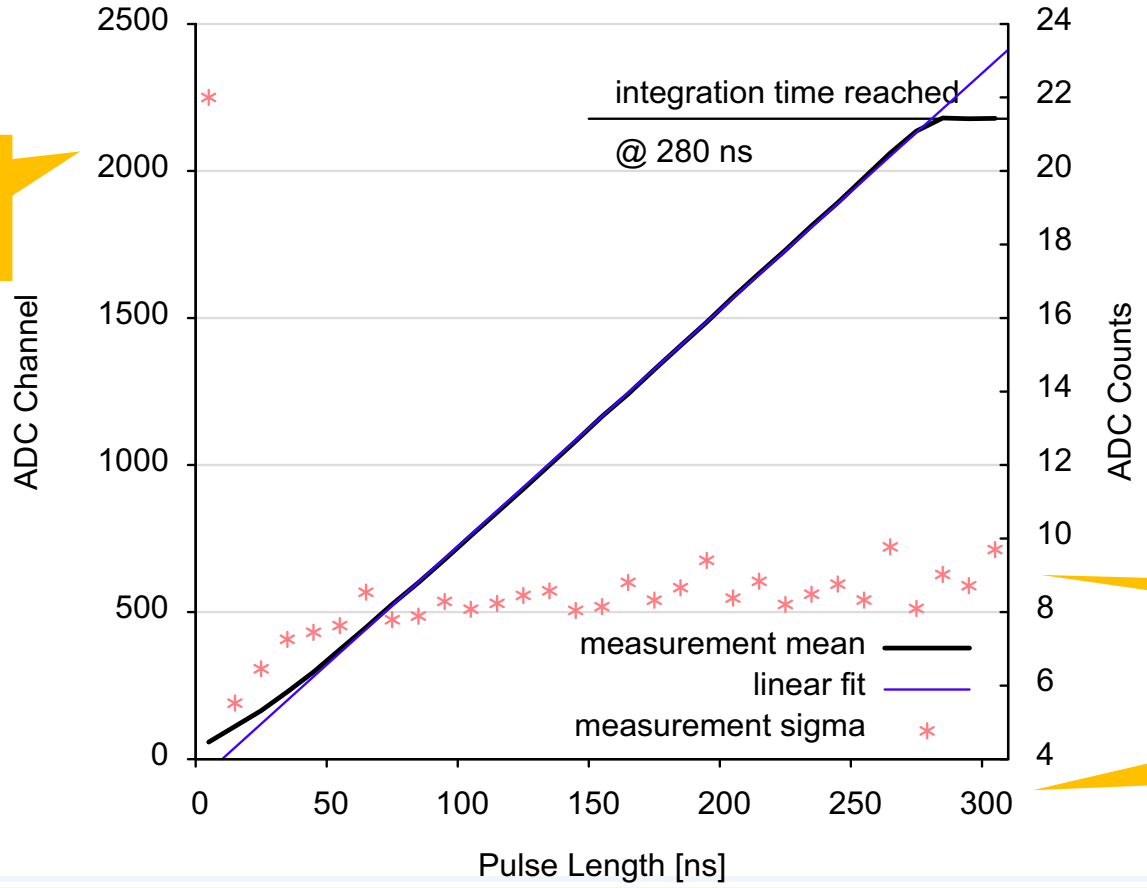
Measurement: Integrator / ADC



Chip performs **true integral** of input pulse (area under pulse)

Resolution ~ 8 Bit. Much better than 15% res. of 511keV!

ADC digital output



σ ~ 9 counts

Input pulse width