Development of CoRDIA: An Imaging Detector for next-generation Synchrotron Rings and Free Electron Lasers

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Outline

- Future sources and detector requirements
- ASIC design
- Signal chain
- Development roadmap
- Outlook

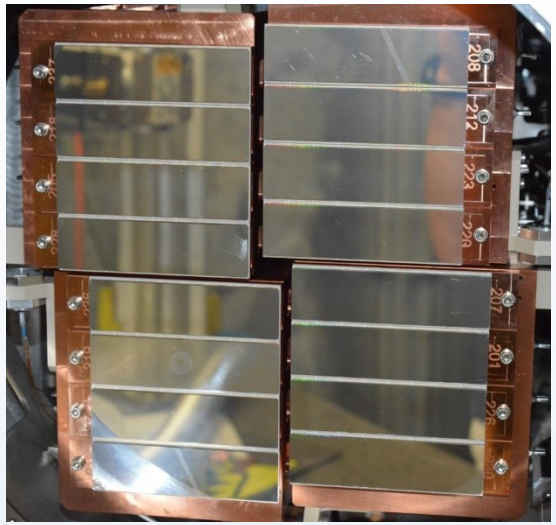
Current Imagers

Imager example for PETRA: **LAMBDA**

- Up to 10 megapixel (55 µm pixel size)
- 2 kHz frame rate (continuous)
- Photon counting up to

  250,000 photons/pixel/s

Imager example for Eu.XFEL: **AGIPD**



- 1 megapixel (200 µm pixels),

  4 megapixel in development
- 4.5 MHz burst imaging

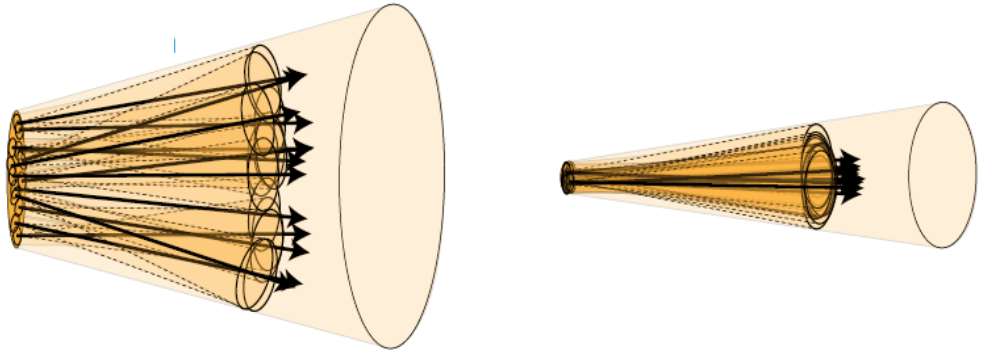
  (internal storage: 352 images)
- Dynamic range – single photon

  to 10^4 photons /pixel/image

Future Source Upgrades

PETRA-IV: Upgrade to diffraction limited ring (2028)

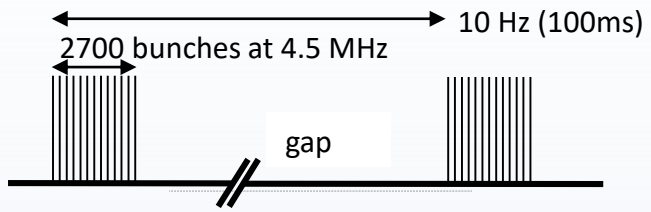
PETRA-III electron bunch PETRA-IV electron bunch



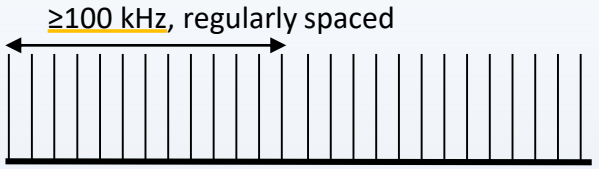
- 100-1000 fold improvement in brilliance and coherent flux
- Frame rate requirements in some experiments increase from kHz to >100 kHz (continuous) readout

European XFEL: CW mode operation (20??)

Current Eu.XFEL burst mode



Future CW operation



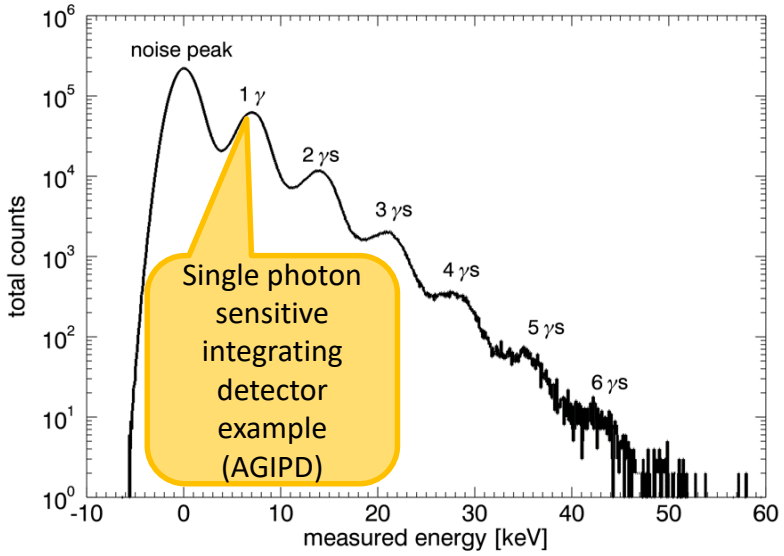
- many more [O(1)] bunches per second
- no gap for burst-readout of internal storage

Common need for:
- continuous readout
- > 100kHz frame rate

CoRDIA – Continuous Readout Digitising Imager Array

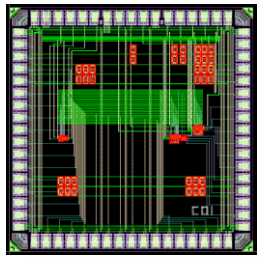
CoRDIA – Design Goals

- Pixel size 100µm × 100µm
- Continuous Frame Rate f_{FR} ≈ 150kHz (≥100kHz)
- Dead-time free pipelined operation
- Single-photon sensitive (@ ≤12keV)
- ≥ 10k photon Dynamic Range
- Little or no dead area



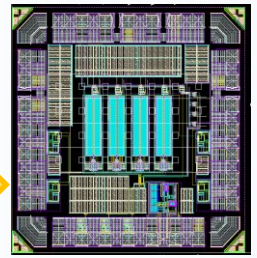
CoRDIA – Implementation

- Hybrid pixel detector
- Charge integrating
- Dynamic gain switching (à la AGIPD)
- Electron-collecting to be compatible with various sensors:
  - Si for hard (12keV X-Rays)
  - High-Z materials for E > 15keV
  - Active (LGAD) sensors for low E
- On-chip digitisation @ ≥ 10 bit
- Multi-Gbit data transmission (based on Timepix4 implementation)
- TSMC 65 nm technology

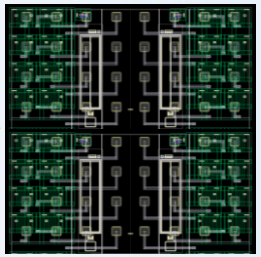


CoRDIA 0.1 (analogue FE) &

HSI_ADC01 (SAR ADC) test chips



CoRDIA 02
4x (16pix+ADC)
test chip
Nov. 2022 MPW

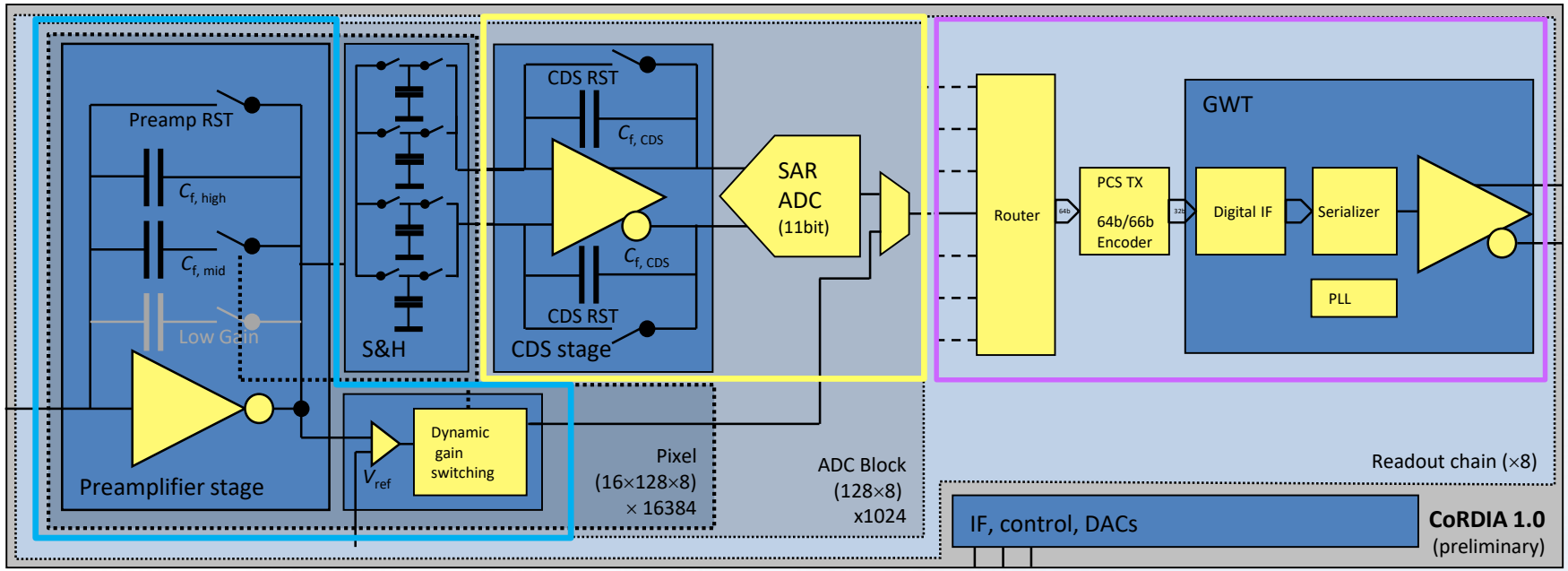


Collaboration of Bonn University & DESY

universitätbonn

DESY.

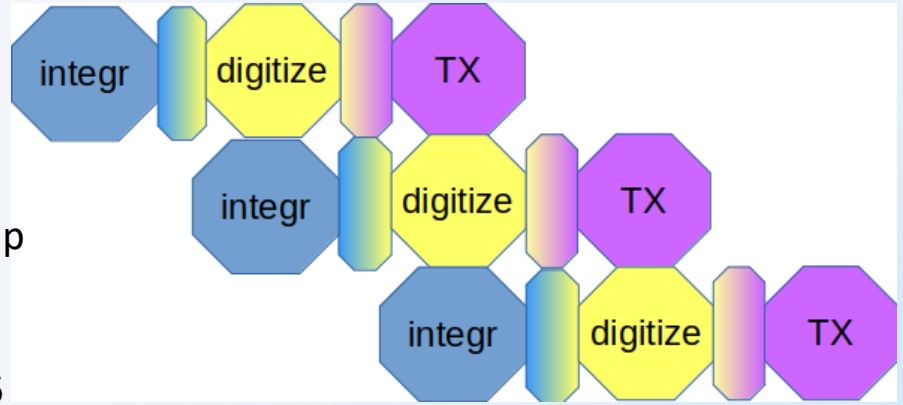
CoRDIA – Architecture & Signal Path



CoRDIA Architecture

- CW (continuous wave) operation
- Pipelined
- Small dead time due to reset of integrating preamp
- Size of individual ASIC chip still under discussion:

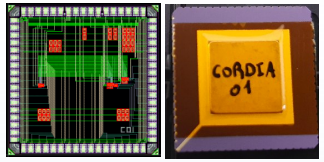
  128 x 128, 128 x 192, 256 x 192, 256 x 256

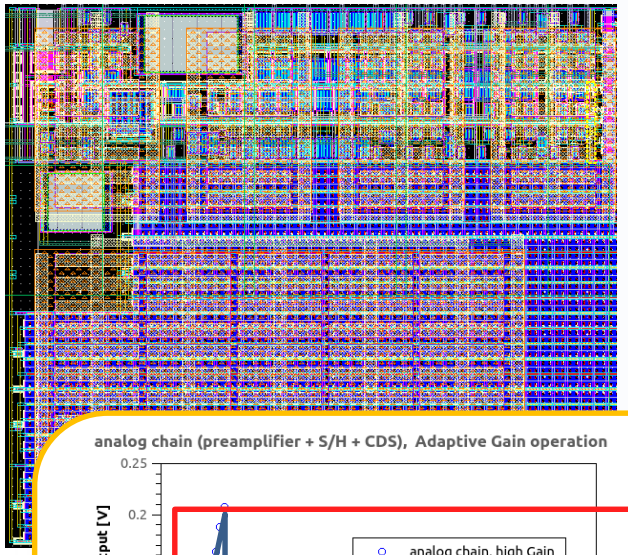


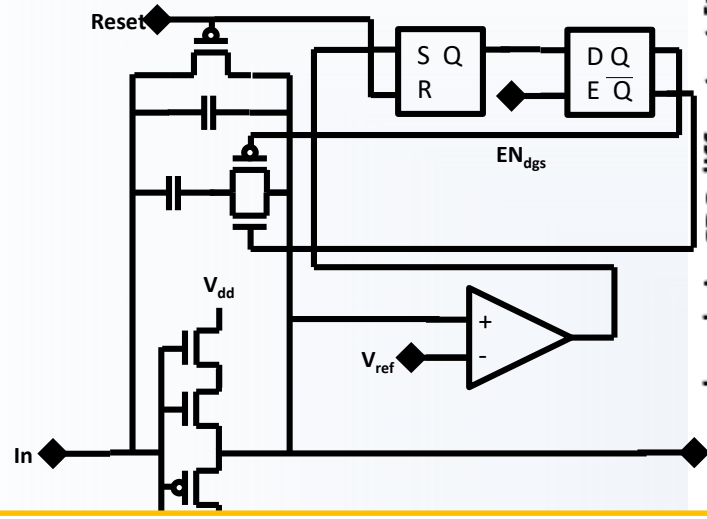
Preamp

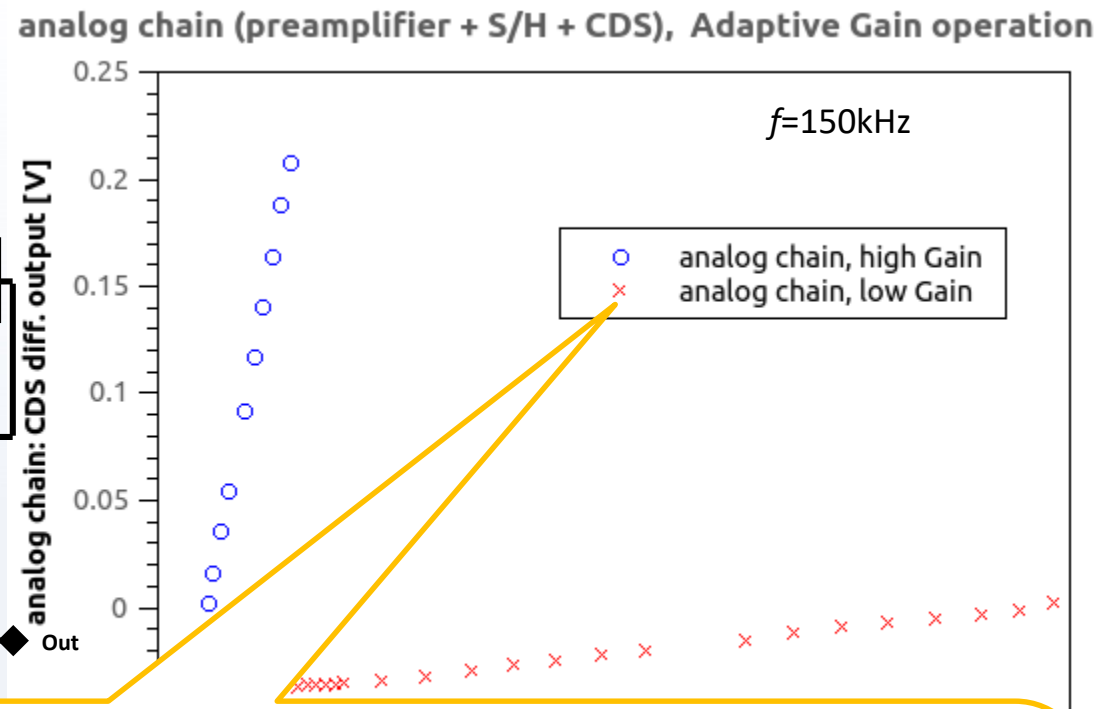
Adaptive gain architecture based on AGIPD

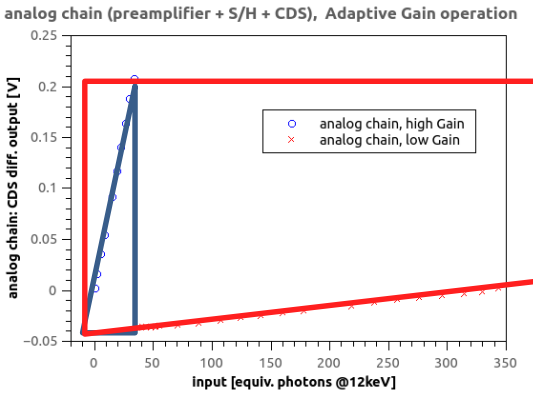
- 2 gains
- Core based on inverter stage
- ‘Std. cell grid’ layout









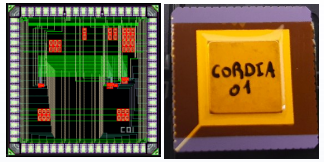


Extrapolation:
~3000 photons

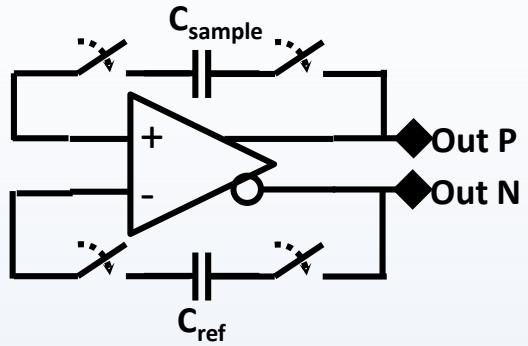
CDS – Correlated Double Sampling Stage

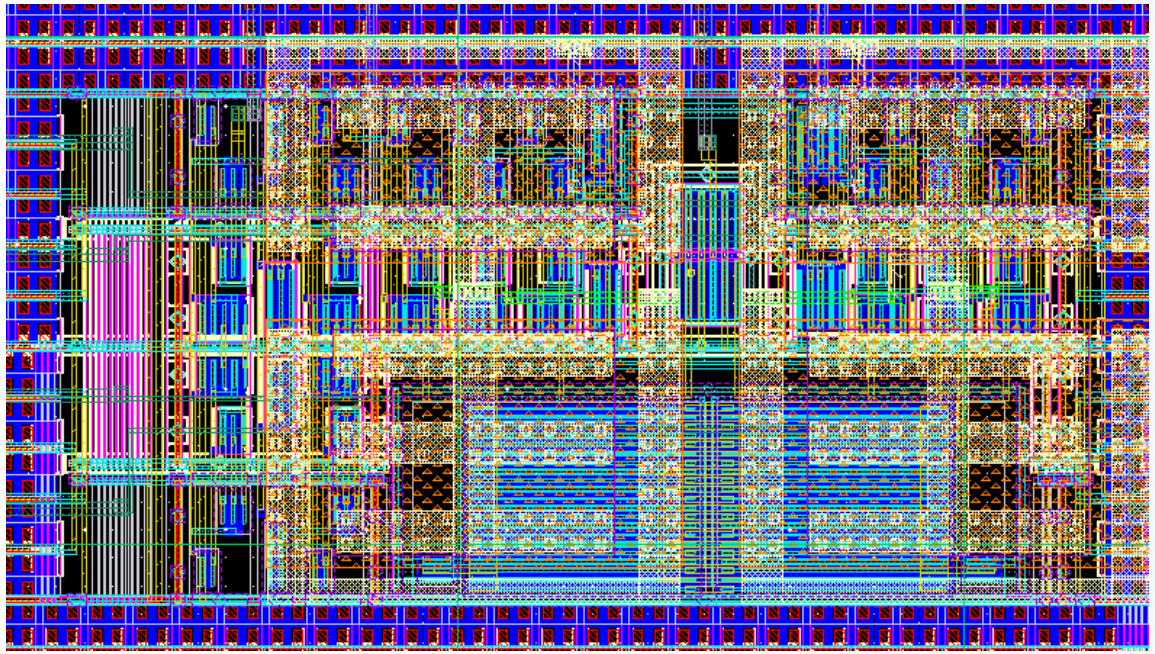
Based on a fully differential amplifier

- Differential pair with simple CM feedback
- SC or continuous sampling (CS) mode
- 2 gains (in CS mode)
- ‘Std. cell grid’ layout

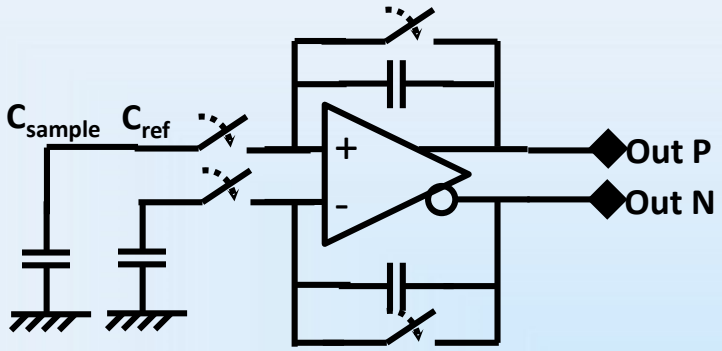


Switched Capacitor mode





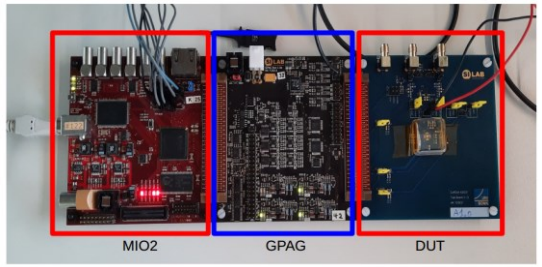
Continuous Sampling mode

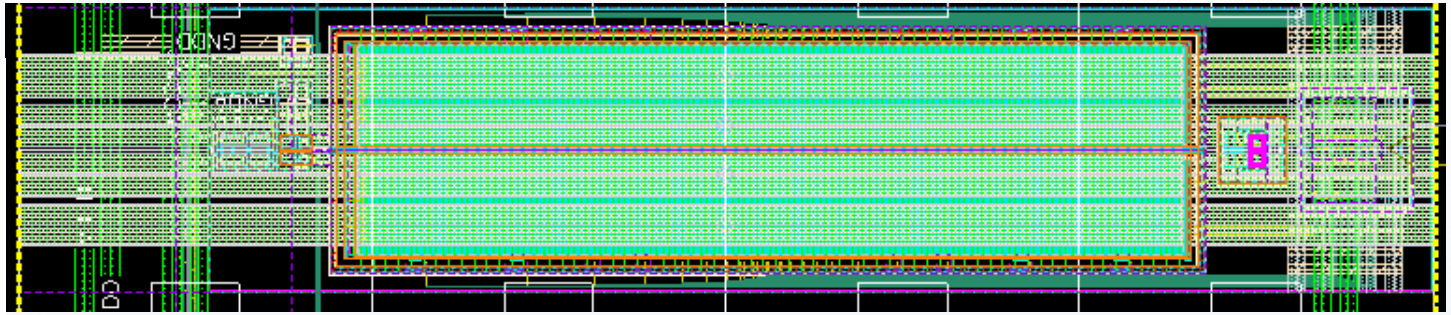


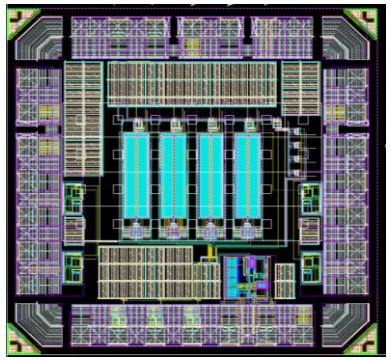
SAR ADC

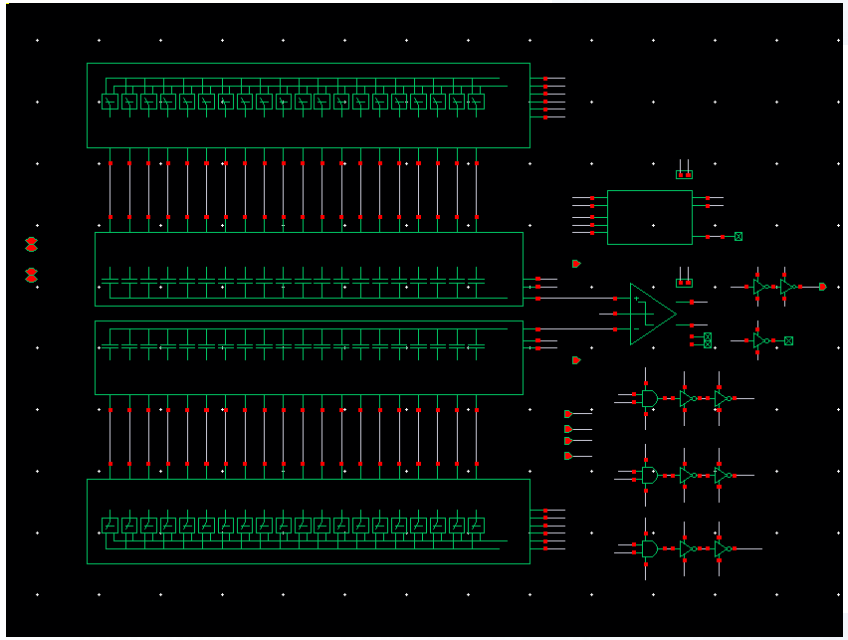
HSI_ADC01 contains 4 successive approximation register (SAR) ADCs

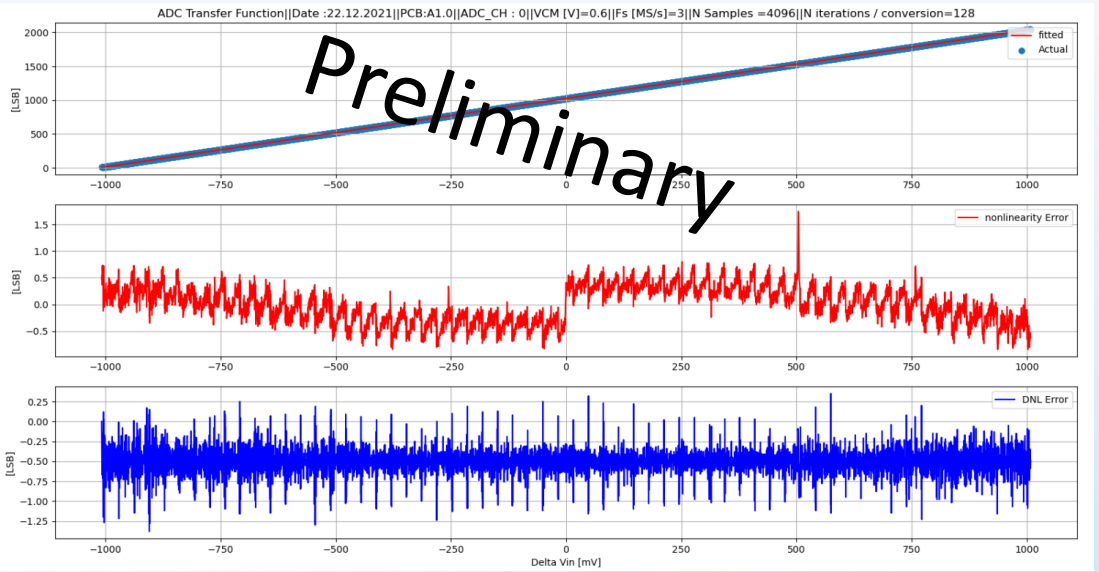
- 11 bit
- ≥2.5 MSamples/s
- Serial data output
- ~10 ENOBs (best one)











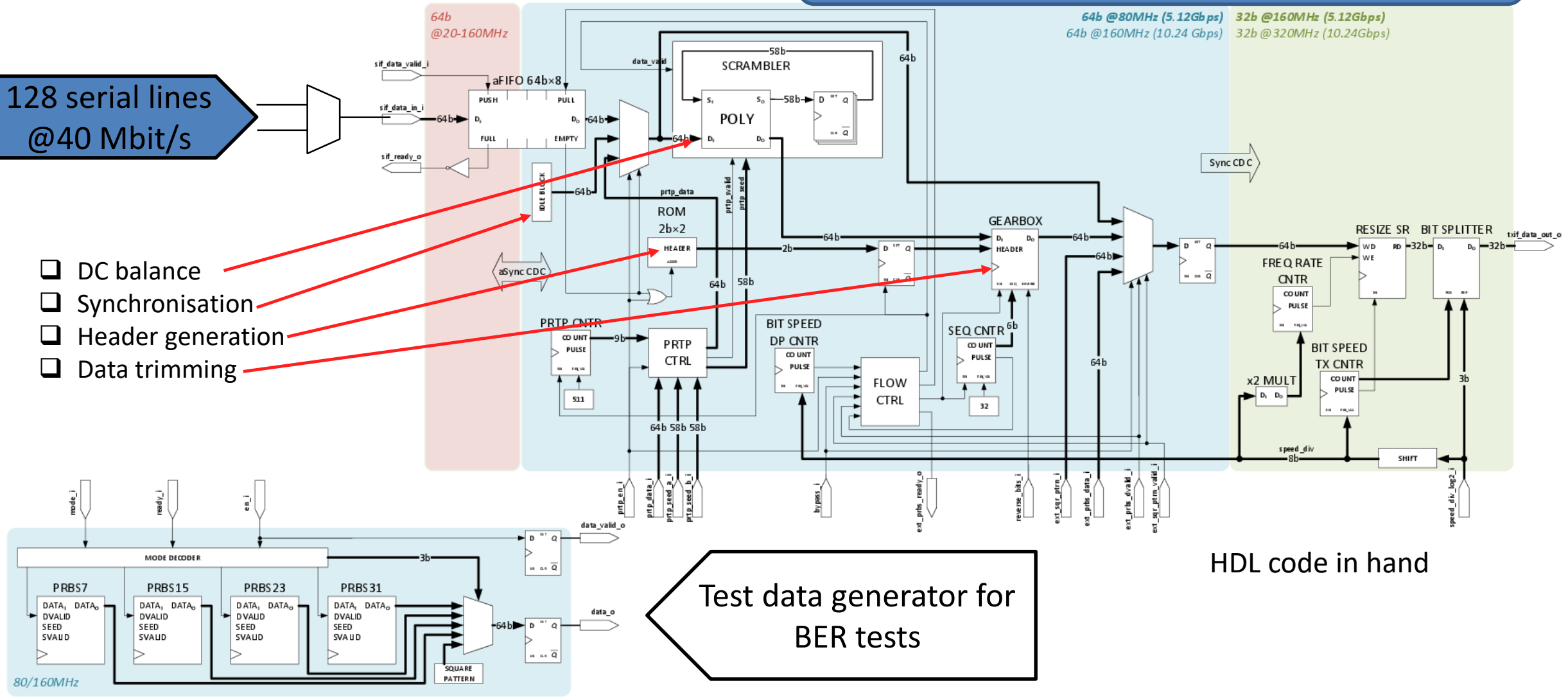
Nonlinearity (INL & DNL) ≤1 LSB => ~10 ENOBs

PCS TX: BLOCK DIAGRAM

Physical Coding Sublayer

128 serial lines @40 Mbit/s

- DC balance
- Synchronisation
- Header generation
- Data trimming



HDL code in hand

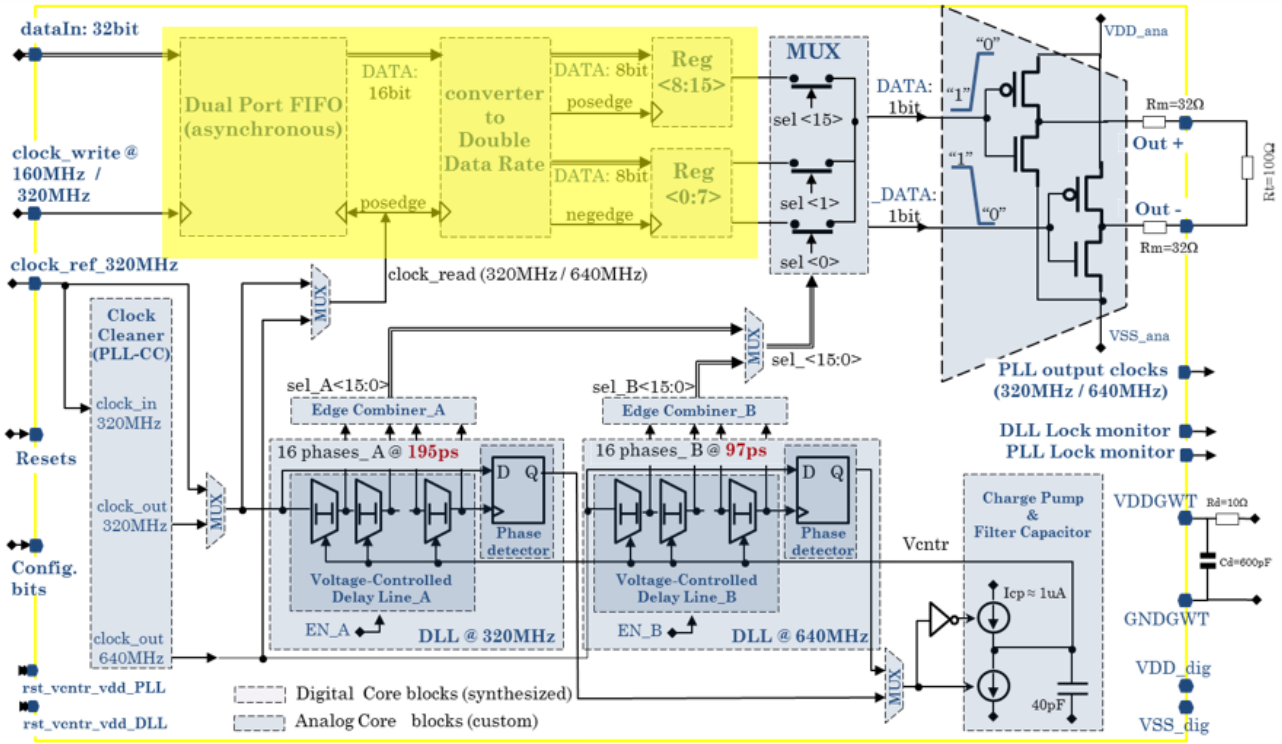
Test data generator for BER tests

GWT – Gigabit Wire Transmitter

Consists of a PLL & a 32 to 1 serializer/mux

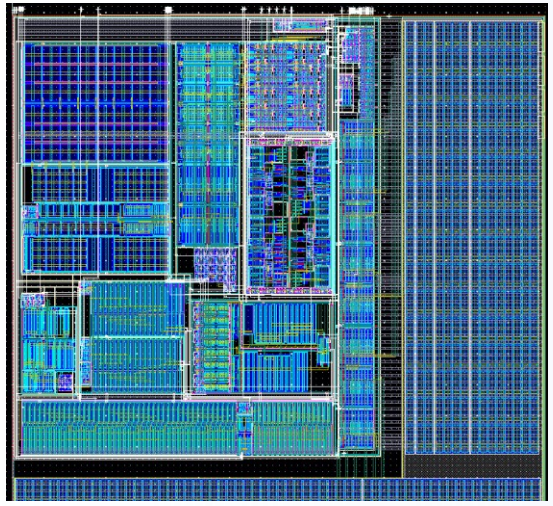
- PLL
- 320MHz or 640MHz
- 86 µm x 120 µm
- Serializer/mux
- 5.12 Gbit/s or 10.24 Gbit/s
- Individual DLLs for either speed
- Differential (100 Ω) off-chip driver
- 86 µm x 67 µm

Developed by
Vladimir Gromov (NIKHEF)

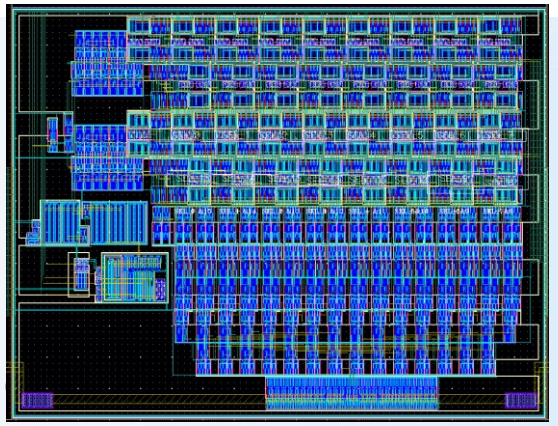


Schematics by Vladimir Gromov (NIKHEF)

PLL

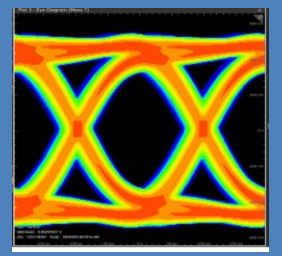


Serializer

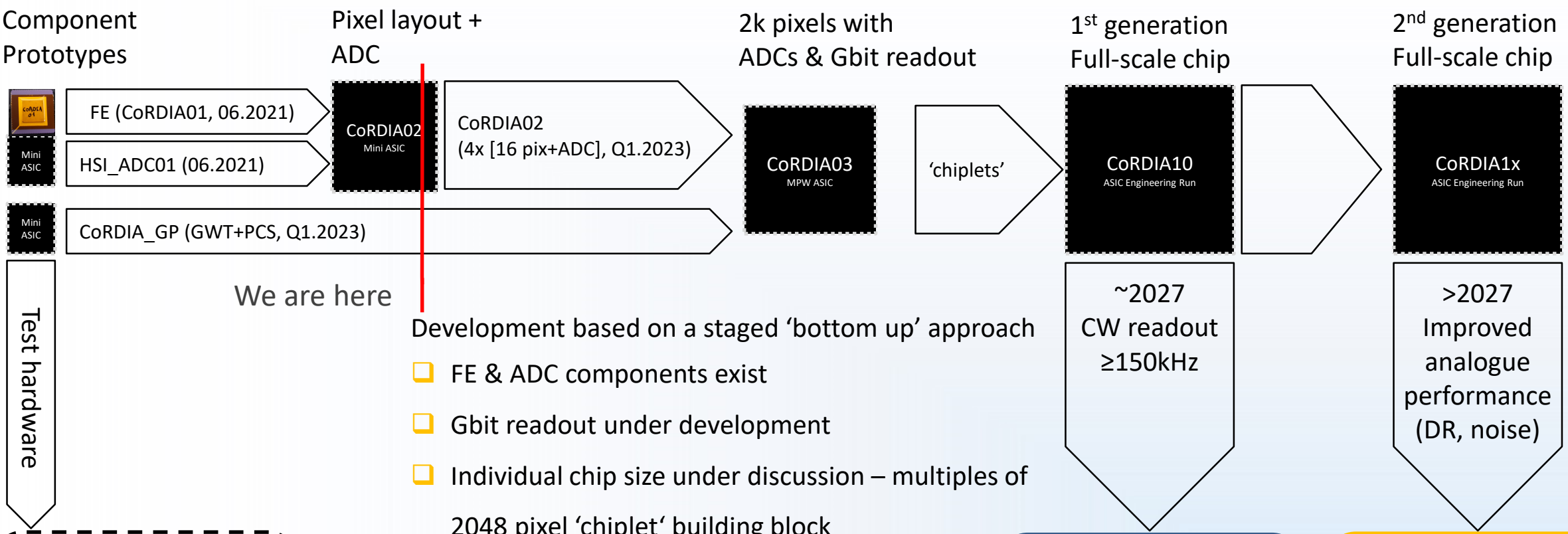


Timepix4 GWT @5 Gbit/s

X. Llopart,
On behalf of the Medipix4 Collaboration
11 th February 2022
CERN seminar



CoRDIA Development Roadmap



Development based on a staged 'bottom up' approach

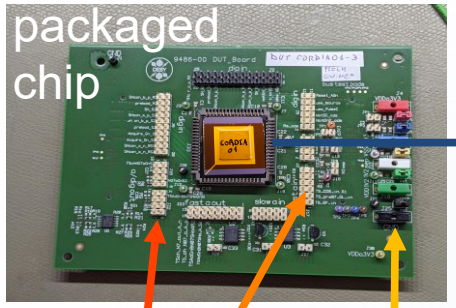
- FE & ADC components exist
- Gbit readout under development
- Individual chip size under discussion – multiples of 2048 pixel 'chiplet' building block
- Target dynamic range needs a new approch
  - Not enough real estate for a big FB cap
  - Ideas exist
- First detectors ready for the start of PETRA IV

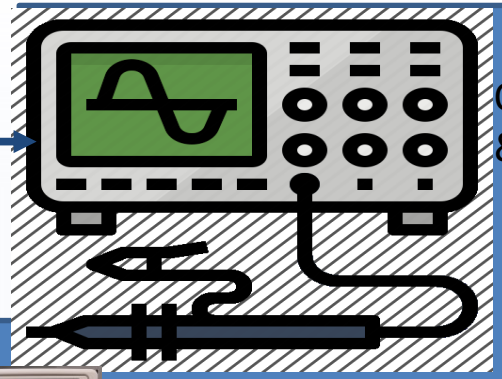
Cordia Chip Tester Board (CCTB) delayed due to excessive lead & mfg. times

Detector systems for PETRA IV (in ambient)

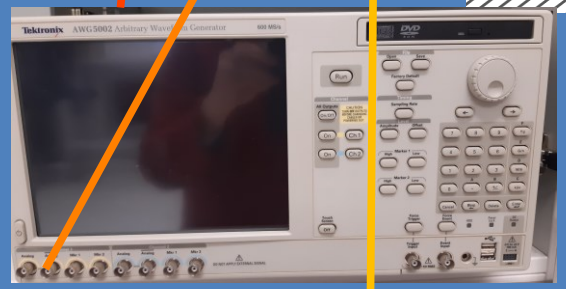
Detector systems for CW XFEL (in vacuum), Systems with high-Z and LGAD sensors

Chip Test Environment

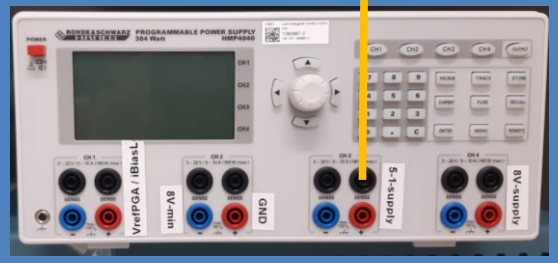




Oscilloscope
& network analyzer

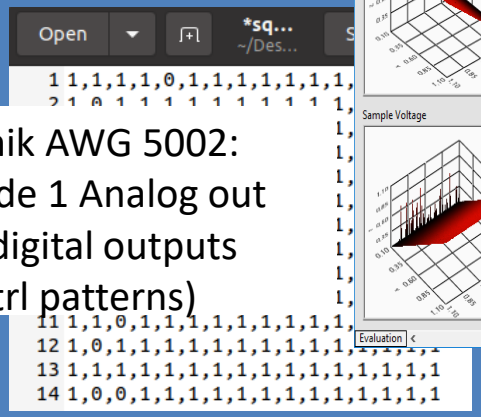


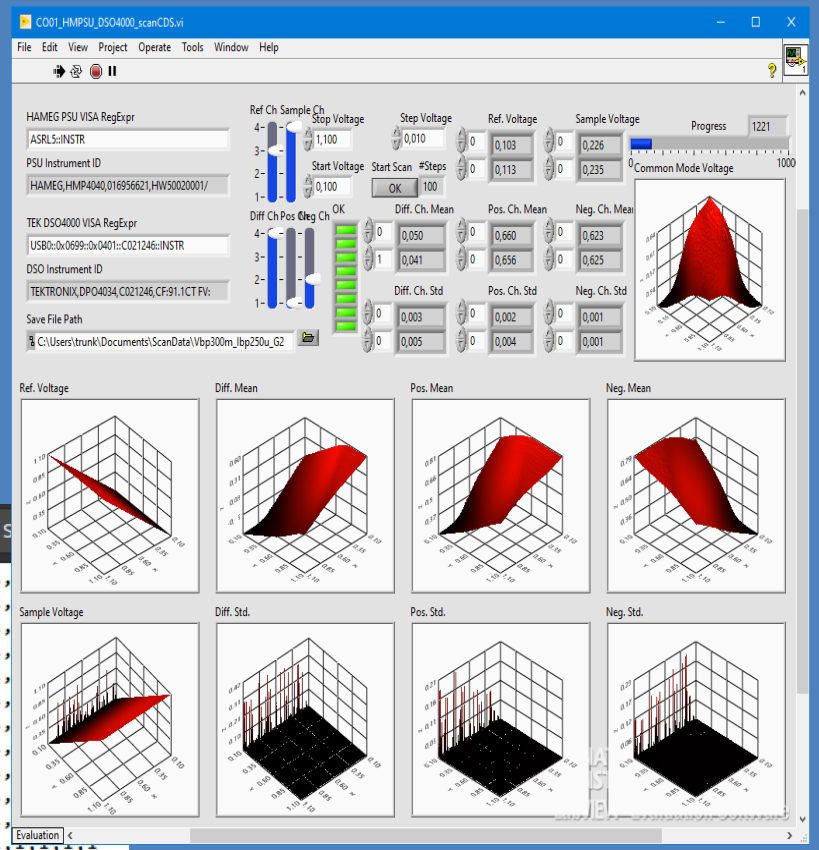
Tektronik AWG 5002 arbitrary
waveform generator
(dynamic analog inputs,
digital control signals)



Lab power supplies
(supplies, biases static inputs)

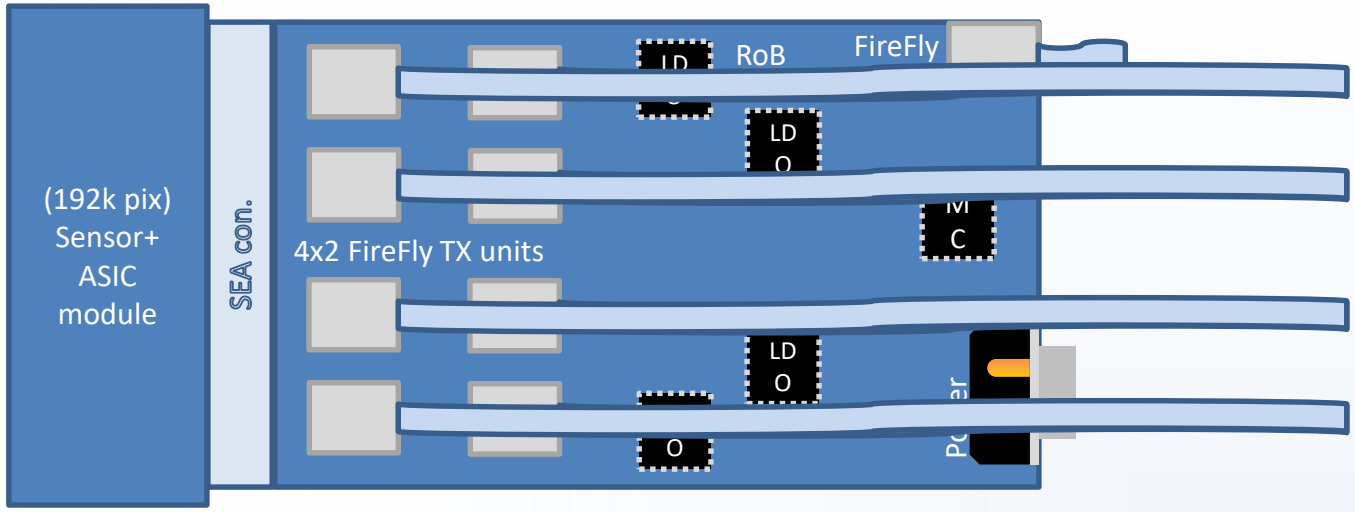
Tektronik AWG 5002:
can trade 1 Analog out
for 14 digital outputs
(dig cntrl patterns)





Measurement automation
with NI LabVIEW

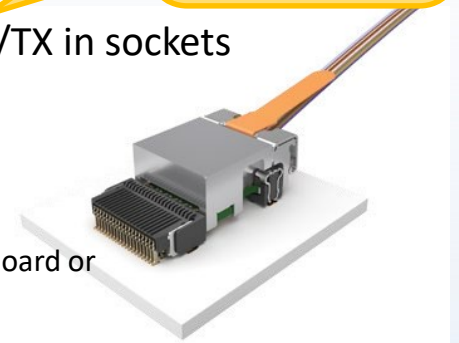
Partitioning, Chiplets & Readout Electronics



‘Dumb’ readout board option

- Only cheap components
- Microcontroller
- Voltage regulators
- Samtc FireFly optical RX/TX in sockets
- Many optical fibres to
- DAQ based on
  - FMC & FPGA evaluation board or
  - µTCA boards

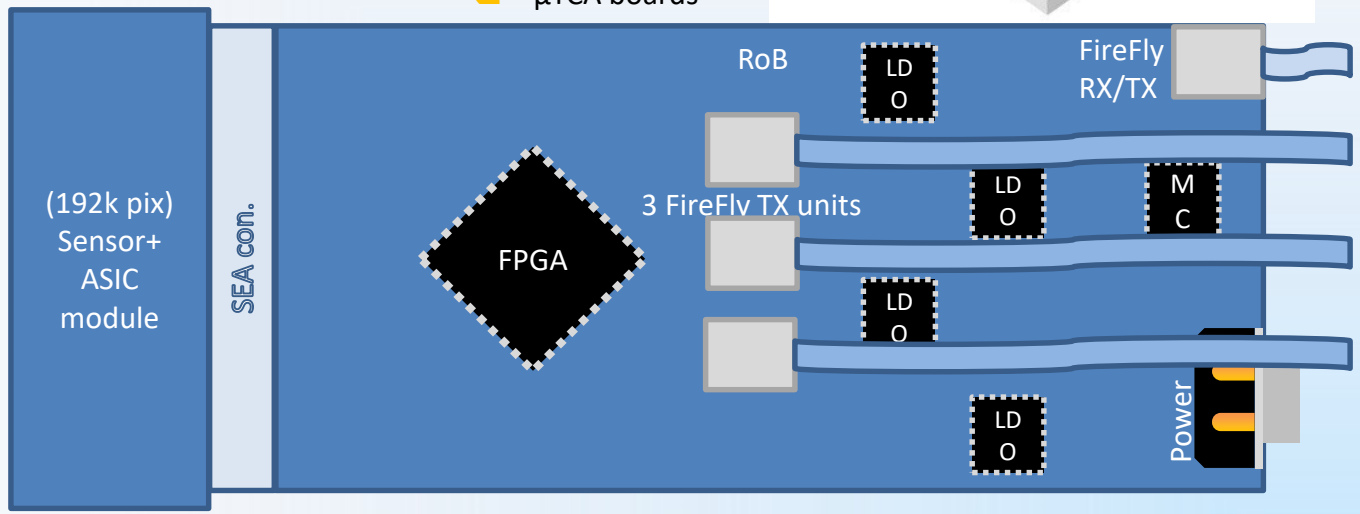
Multiples of 12 channels



Multiples of 8 channels

FPGA based readout board option

- Expensive & heat producing components
- Low number of fibres
- Direct commercial network interface to DAQ servers
- Considerable development effort



Partitioning, Chiplets & Readout Electronics

Final chip size is still under discussion…

- Multiple of (16 x 128) pixel = 2048 pixels
- Choice of ROB architecture
- Yield
- Available sensor sizes

AGIPD sized chips

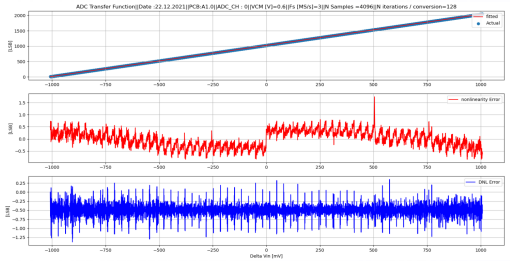
TimePix 4 sized chips

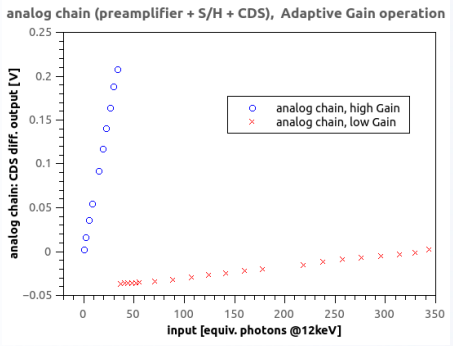
Chip size (pixl)	# of 5 Gbit links	Smallest reasonable FEM	FEM size (pixel)	# of FireFly TX (12 ch)	256 x 768 pix module size (chips)
128 x 128	8	2 x 3	256 x 384	6	2 x 6
128 x 192	12	2 x 1	256 x 192	2	2 x 4
256 x 192	24	1 x 1	256 x 192	2	1 x 4
256 x 256	32	1 x 3	256 x 768	8	1 x 3

Summary

CoRDIA – Continuous Readout Digitizing Imager Array - is…

- Targeted to DL Synchrotron sources (like PETRA IV)
- CW FELs (future CW Mode of European XFEL)
- Hybrid Pixel Detector
- Charge Integrating & dynamic gain switching
- Pixel size 100µm x 100µm
- Continuous Frame Rate f_{FR} ≈ 150kHz (≥100kHz)
- On-chip digitisation @ ≥ 10 bit
- MGbit data transmission





- All fundamental components exist
  - FE & ADC on test chips
  - MGBT readout on TimePix 4
- (Component) test chips show good performance
- Implementation of pixel blocks is ongoing
- Implementation of MGBT readout started

- Full-size chips for detectors at PETRA IV ~2027
- CW-FEL version with higher analogue performance ready for future CW operation of Eu.XFEL