Contribution ID: **112** Type: **Poster without speed talk**

Novel high-speed monolithic silicon detector for particle physics

Progress in experimental physics relies often on advances and breakthroughs in instrumentation, leading to substantial improvements in measurement accuracy, efficiency, and speed, or even opening completely innovative approaches and methods. Such experiments push the requirements for sensors technologies in several characteristics like tracking precision, timing, material budget, radiation hardness and/or data rate. The Helmholtz initiative Tangerine (Towards Next Generation Silicon Detectors) driven by DESY, GSI and KIT concentrates on research and development for both, novel sensors, and front-end technologies/architectures. To establish the availability of sensors with high spatial (20 µm) and time resolution (20 ps) for charged particles, a new concept of pixel detector is proposed. It is designed for 25 x 25 µm2 pixel pitch, time resolution less than 20 ps, charge sharing for improvement of spatial resolution and possibility to detect the impact angle of the track on the sensor. The proposed detector architecture consists of a monolithic LGAD sensor tightly integrated with a new analog front-end based on BiCMOS devices. To improve the in-pixel functionally while keeping a remarkably high granularity and simple integration concept, the monolithic sensor and analog SiGe front-end is AC-coupled to a digital ASIC developed in the recent CMOS process.
The first prototype of the monolithic sensor and the analog readout chain has been produced by the Leibniz Institute for High Performance Microelectronics (IHP) and is made in SG13G2 130nm BiCMOS technology (Pic 1). P-type bulk has epitaxial origins with a thickness of 50 µm. To increase in-pixel functionality and to fulfill the requirement to measure the position, time and energy, an improvement of both, readout architecture and ASICs technology are required. Within Tangerine project several design options are under investigation for the digital readout of 22 nanometer CMOS technologies in a fully depleted silicon-on-insulator (FDSOI) processes or 28 nm TSMC. Because each detected particle might provide information on position, time, energy and impact angle, the signal of neighboring pixels is on-chip processed by an artificial intelligence algorithm. The results are expected to be a perfectly accurate x-y-t reconstruction and at the same time might reduce the effective data rate. Both the sensor and the readout chip are attached using a thin glue layer and are AC-coupled. Such process simplifies the connection between the sensor and the front-end and has been successfully developed at KIT previously [1].
In this contribution, the first version of the monolithic sensor is presented, and the preliminary results are discussed. The main aim of the design was to study the trade-off between the charge sharing mechanism and the timing performance by a small active pixel area with an NWELL size of 10 µm by 10 µm. Collection time and charge sharing effects could be optimized for this sensor technology.

Primary author: TRIFONOVA, Ekaterina (KIT)

Co-authors: CASELLE, Michele (KIT); EHRLER, Felix (KIT); Mr ELSENHANS, Alexander (KIT); KOPMANN, Andreas (Karlsruhe Institute of Technology (KIT)); PATIL, Meghana Mahaveer (KIT); PERIC, Ivan (BELLE (BELLE II Experiment)); WEBER, Marc (KIT)

Presenter: TRIFONOVA, Ekaterina (KIT)

Session Classification: Conference Dinner with Poster exhibit

Track Classification: Detector Technologies and Systems