Towards the ALICE ITS3: mechanical intergration of the super-ALPIDE

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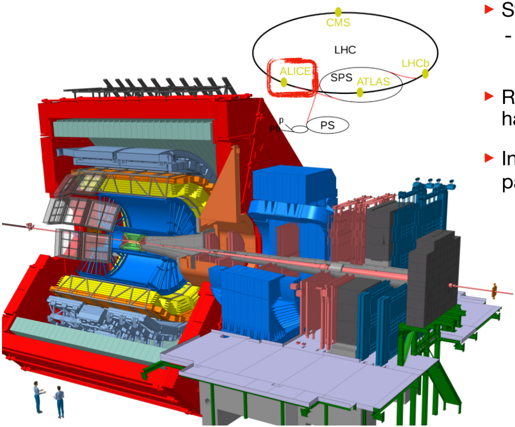
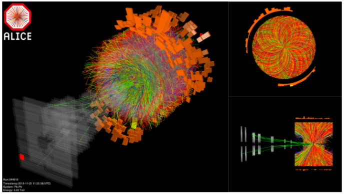
Detector and main goals



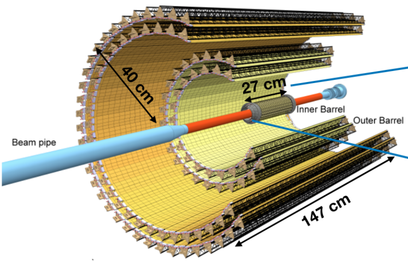
- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction



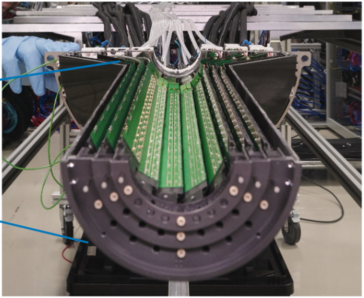
ITS2

It is fabricated in MAPS(Monolithic Active Pixel Sensor) technology. Using TowerJazz 180 nm process. Cover $10\ \text{m}^2$ features 12.5 Gpx.

Layout

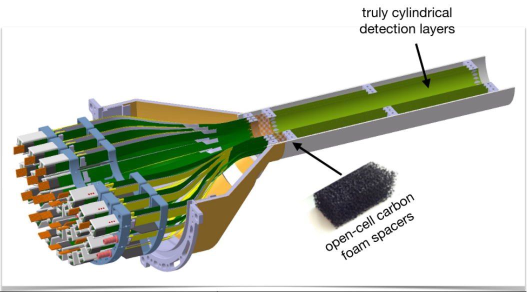


ITS2: assembled three inner-most half-layers



- ITS2 is expected to perform according to specifications or even better
- The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- **Key questions: Can we get closer to the IP? Can we reduce the material further?**

ITS3 Detector Concept



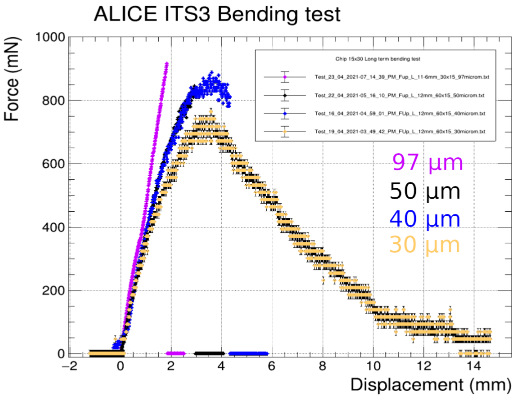
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- Key ingredients:
  - 300 mm wafer-scale chips, fabricated using stitching (65 nm TowerJazz process)
  - thinned down to 20-40 μm (0.02-0.04% X0), making them flexible
  - bent to the target radii
  - mechanically held in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X0(beampipe: 500 μm Be: 0.14% X0)
  - -homogeneous material distribution: negligible systematic error from material distribution

THE WHOLE DETECTOR WILL COMPRISE SIX (!) CHIPS (CURRENT ITS IB: 432) - AND BARELY ANYTHING ELSE

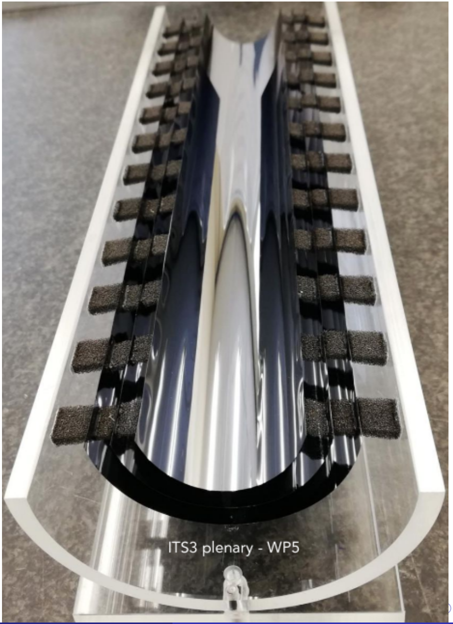
Flexibility of silicon

- Monolithic Active Pixel Sensors are quite flexible
  - already at thicknesses that are used for current detectors
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors
- Breakage at smaller radii for thinner chips
  - again benefit from thinner sensors
- **Our target values are very feasible!**

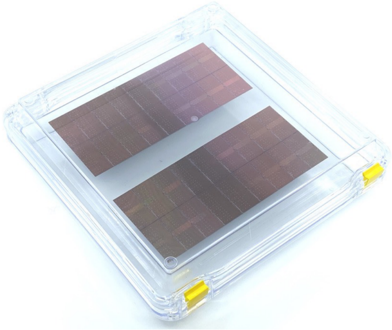


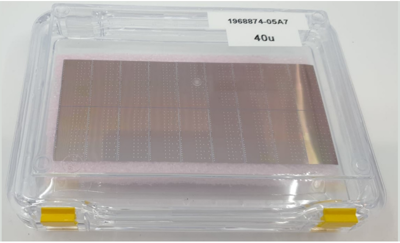
Challenges for the new sensor chips

- $300\,$mm wafer-scale chips
- thinned down to 20-$40\,\mu$m



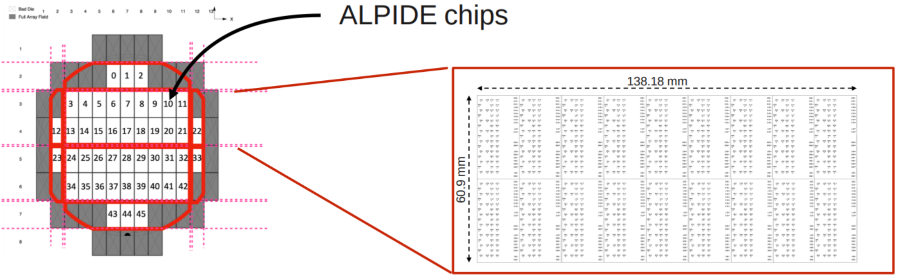
Super ALPIDE Chips



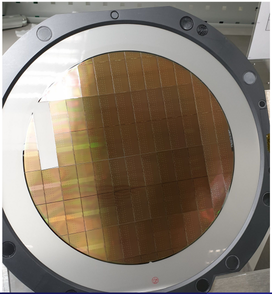


- To study the bending and interconnection of large pieces of processed chips, ”super-ALPIDE” is built
- Comprises of 1 silicon piece cut from an ALPIDE wafer size of $14\,\text{cm} \times 6\,\text{cm}$

Super ALPIDE Chips

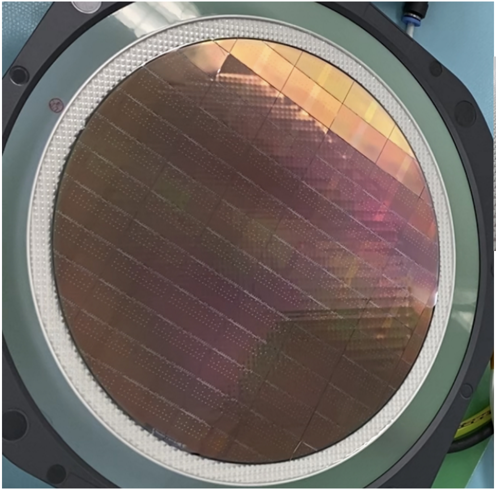


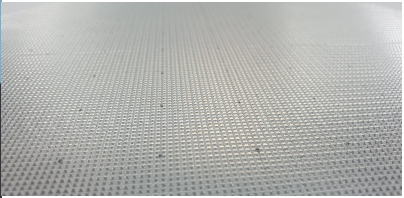
18 ALPIDE chips, covering about a half of an ITS3 half-Layer0



- Super-ALPIDEs are actually an array of ALPIDES.
- They consist 9×2 ALPIDE chips.

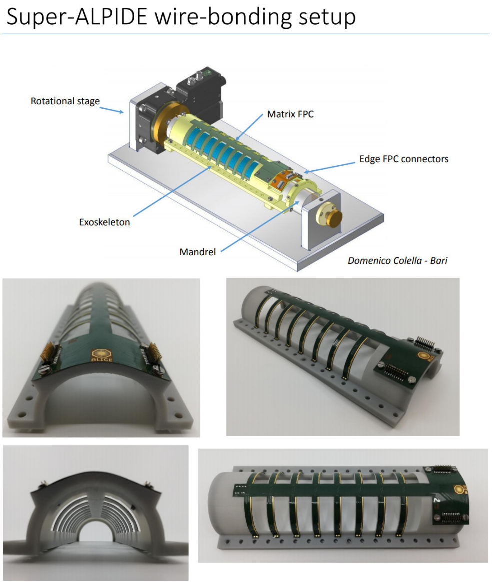
Super ALPIDE Chips





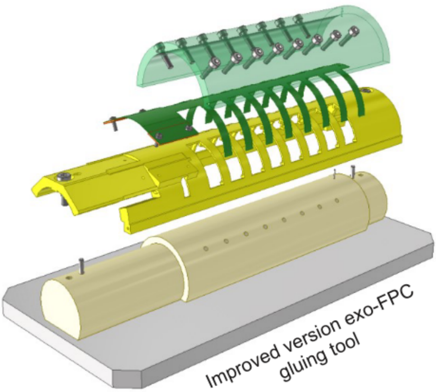
- Tested different methods how to pick large and very thinned chips
- Die-ejector with fine grid is quite efficient.

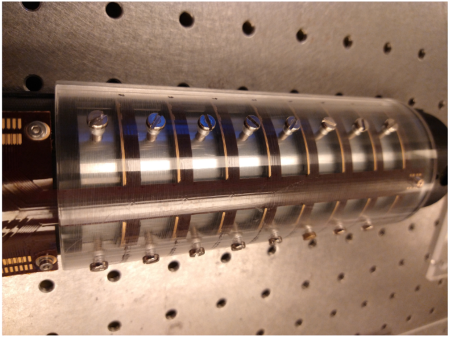
Exoskeleton

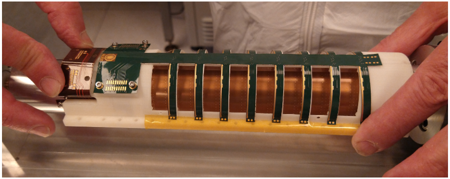


- 3-D printed.
- Designed to support super-ALPIDEs after bending.
- Windows to reach interconnection points at middle of super-ALPIDE
- FPC glued for connections

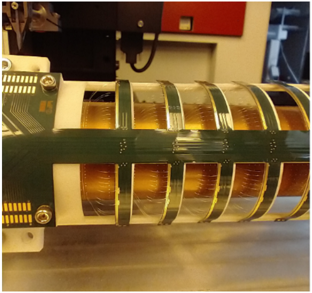
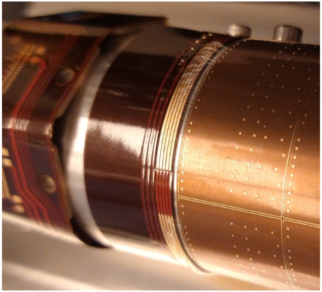
Gluing FPC







Bonding

- The first row of ALPIDEs will be wire-bonded to an edge-FPC (just like final ITS3)
- The rest will be bonded to FPC on Exoskeleton via long wires

Summary

- Super-ALPIDEs are produced and picked up successfully
- Testing setup with a exoskeleton is ready
- Bonding super-ALPIDEs are in progress
- Wafer-scale chips will be handled via Know-how learnt from super-ALPIDES