# BCM upgrade - objectives and constrains

**FrontEnd :**

- time/amplitude resolution and dynamic range
- analog/digital readout
- trigger outputs
- readout rate
- ASIC
- TTC

**BackEnd :**

- data and trigger delivery
- commercial/custom electronics
- stand-alone/CMS DAQ
- TTC

**Services :**

- cables/fibers
- patch panels
- PS



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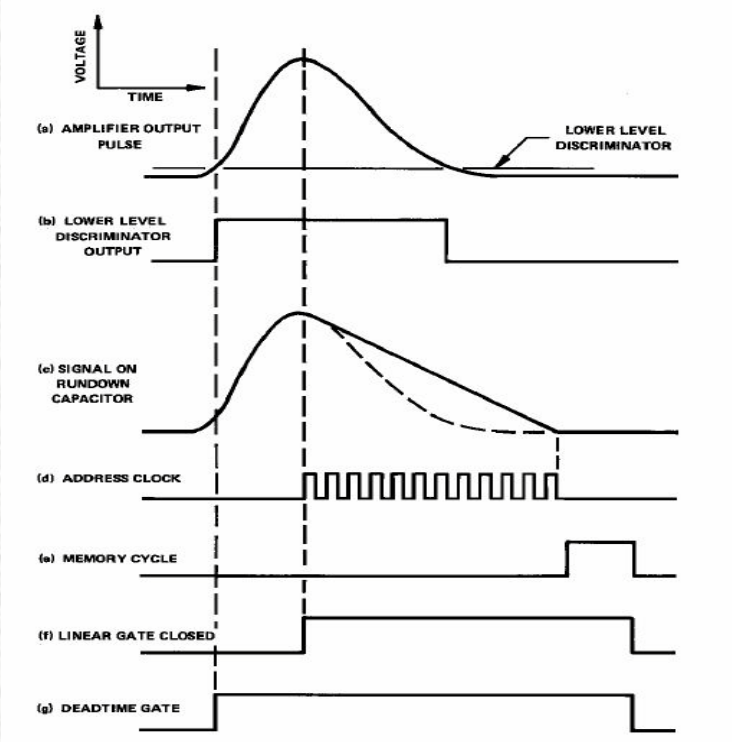
# FrontEnd ASICs

- only a few provide time+amplitude
- mostly tracker applications :
  - ✓ huge number of channels
  - ✓ slow readout
  - ✓ no fast trigger output
  - ✓ lot of control/configuration
- very ‘custom’ oriented - dynamic range/resolution




**Wilkinson ADC/TDC topology**
**TOT: Time - Over-Threshold**

- ✓ simple
- ✓ excellent differential linearity
- ✓ slow: clock rate limit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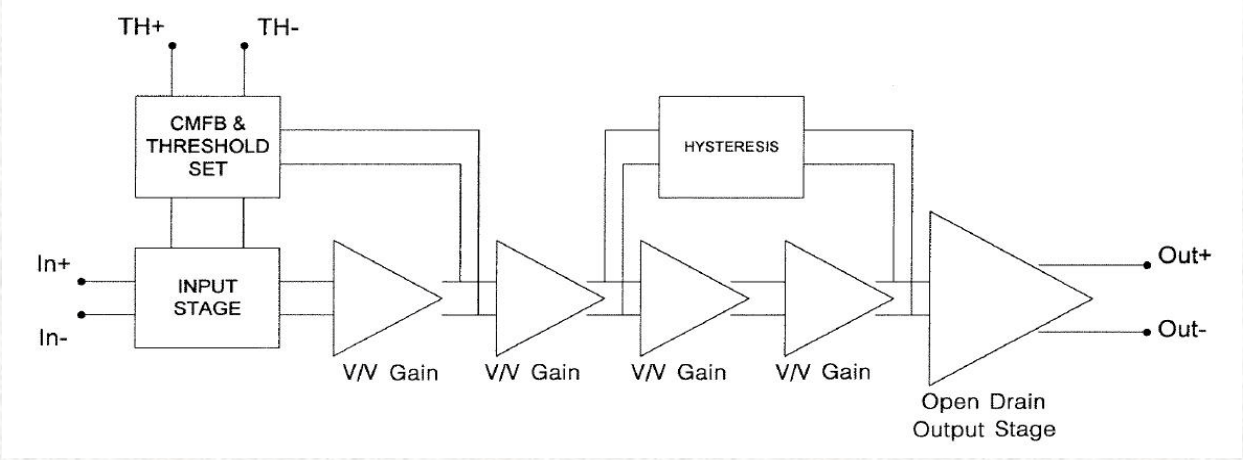
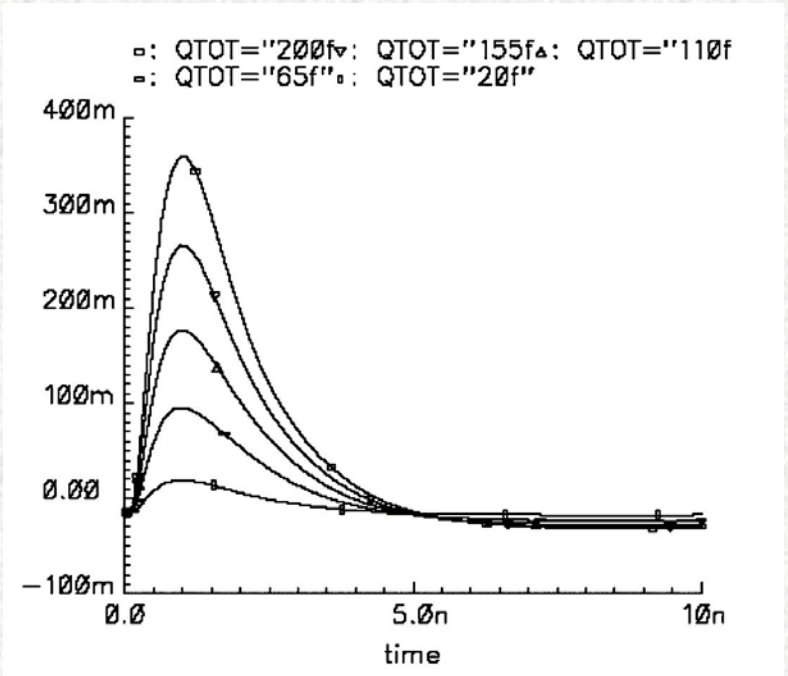
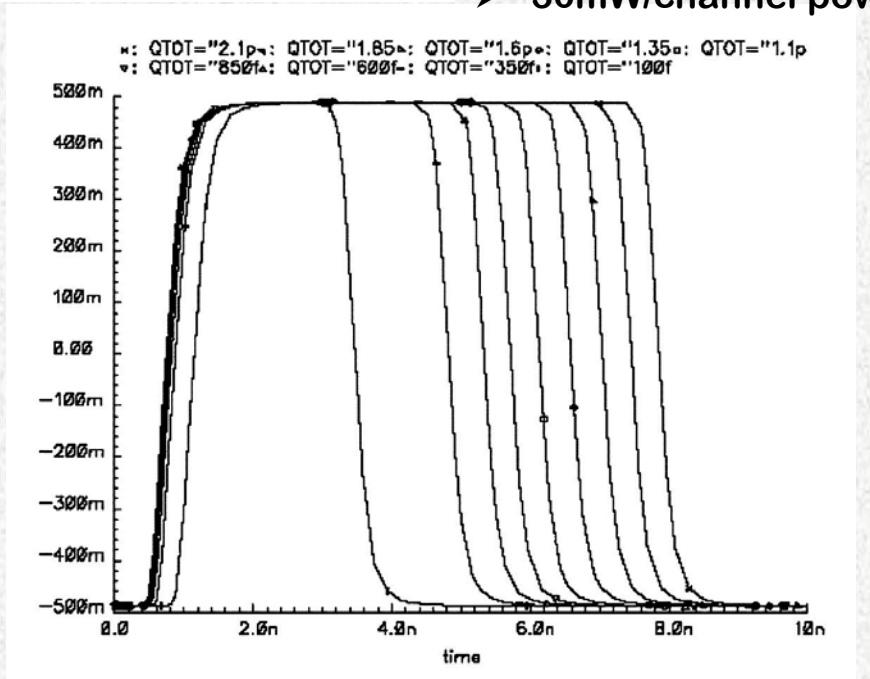
# NINO: ultrafast front-end preamplifier-discriminator




**ALICE time-of-flight detector ASIC**

- radhard IBM 0.25um CMOS
- 8 channels
- 1ns peaking time
- 0.1 - 2pC input range
- < 5000e- RMS noise with 10pF detector
- 10fC – 100fC threshold
- 30mW/channel power



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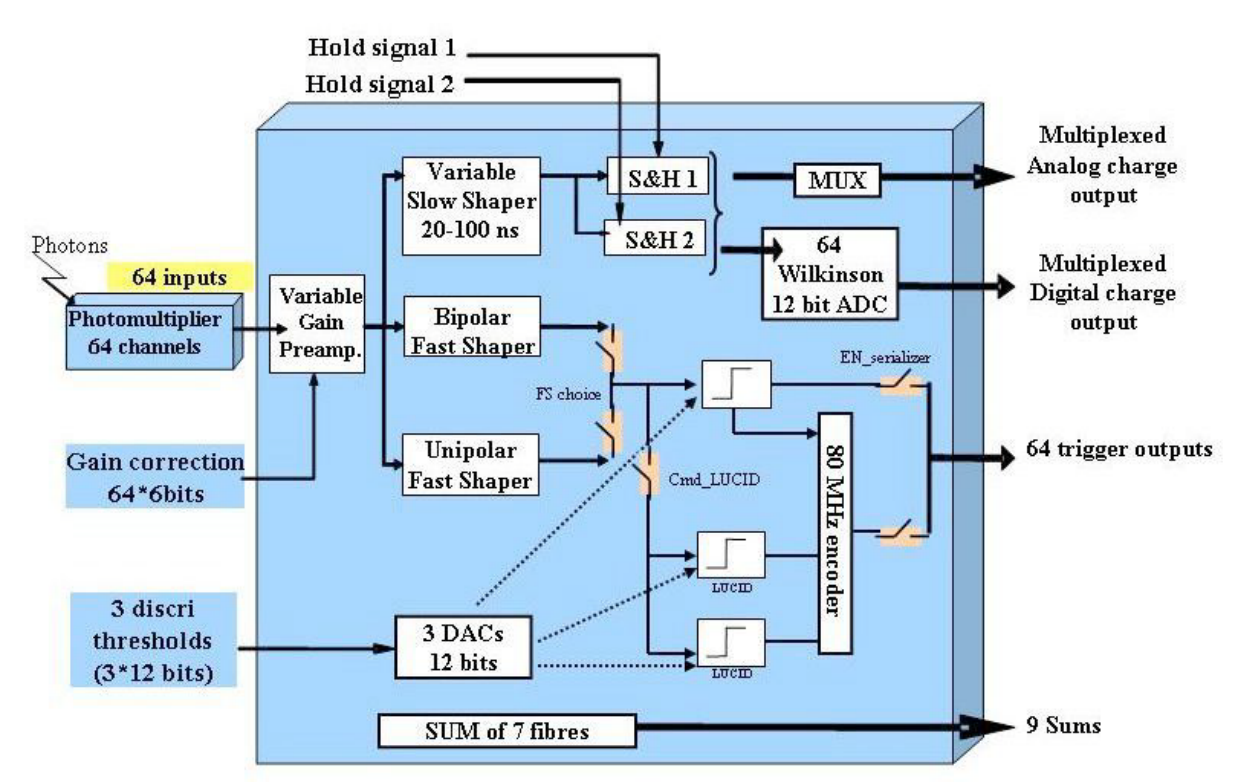
# MAROC: multi-anode readout chip




**ATLAS Roman pots ASIC**

- **AMS Si-Ge 0.35um techno**
- ……



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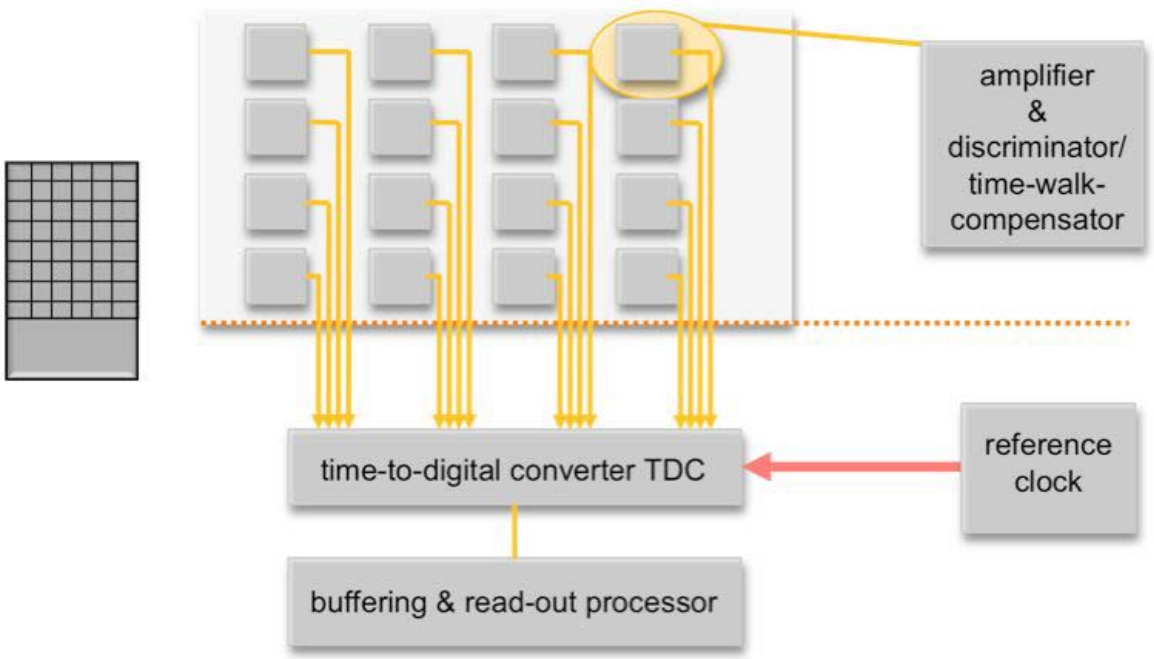
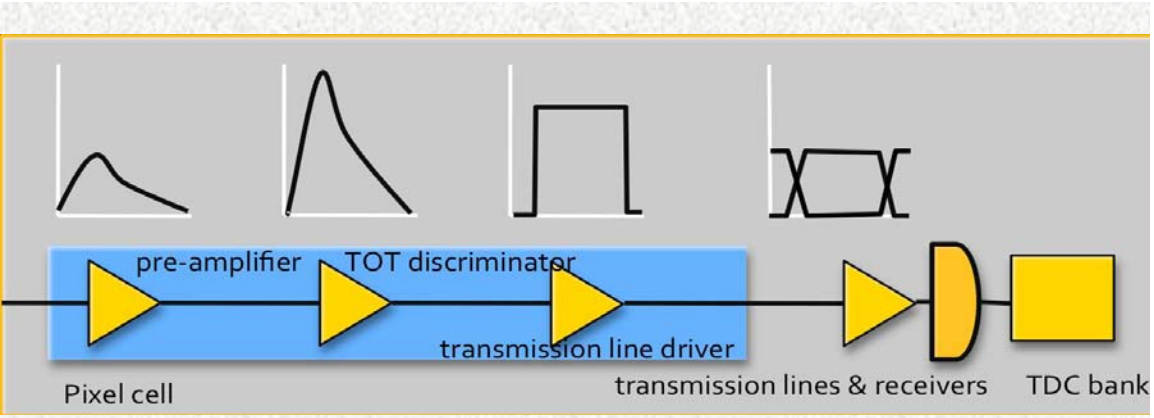
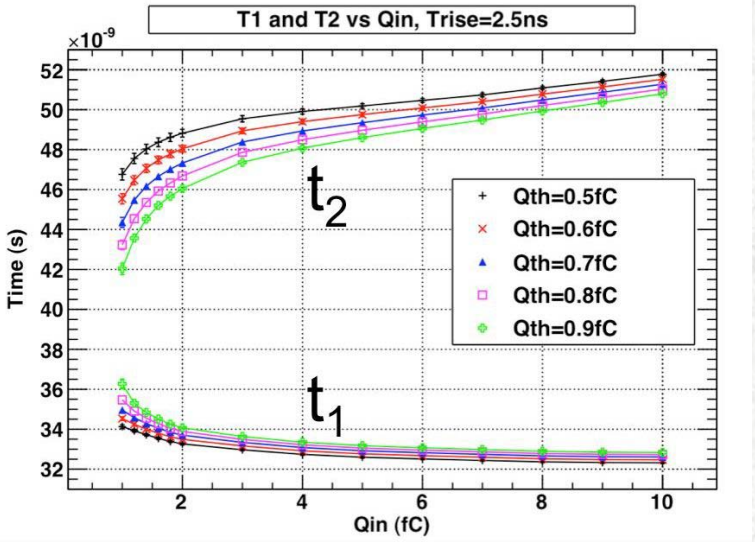
# GTK: gigatracker pixel detector chip




## NA62 pTDC and EOC ASICs

- radhard 0.13um CMOS techno
- EOC proto – 60 pixels ($1.8\times3.0mm^2$)
- pTDC proto - 105 pixels ($2.1\times4.5mm^2$)
- 2.4fC most probable input charge
- 0.6 – 10fC dynamic range
- < 200ps time resolution
- $2W/cm^2$ power consumption



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# ASIC technology availability and cost

**250nm CMOS :**

- radhard by layout techniques
- well-known (tools, libraries, etc.)
- 100kCHF per Multi Project Wafer (MPW)

**130nm CMOS :**

- naturally radhard
- complex, more expertise demanding (tools, rules, etc.)
- ~3kCHF per 1mm$^2$ (!) via MOSIS

**What can we effort in terms of budget, time and manpower?**