BCM1F 'B.T.O.' Modules

Outline

- Why 'Built to order' Modules?
- VETO Module
- Look Up Table
- Possible Extensions
- Summary

BCM1F 'B.T.O.' Modules

Why 'Built to order' Modules?

a) lack of performance of commercial modules

Here: TDC buffer memory too small or readout too slow

While block transfer is still in progress the buffer memory is already overwritten by new input data.

b) need for versatile, programmable functionality

Here: multiple logic operations on digitized sensor signals, supplemental i/o signals

Request for a flexible, multi-channel coincidence logic to allow for a fast luminosity assessment.

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VETO Module (1)

TDC Block Transfer time (16k x 32bit): 3.7ms

2nd half of buffer is filled while 1st one being read out

-> overall input rate limit per channel to avoid overflow is:

$$\frac{\text{50\% of buffer}}{\text{transfer time * nb. of channels * storage width}} = 0.54\text{MHz or } 1.85\mu\text{s}$$

Lumi estimation however gives 1.25MHz (800ns) Hit rate/channel

-> Inputs of TDC have to be blocked during readout!

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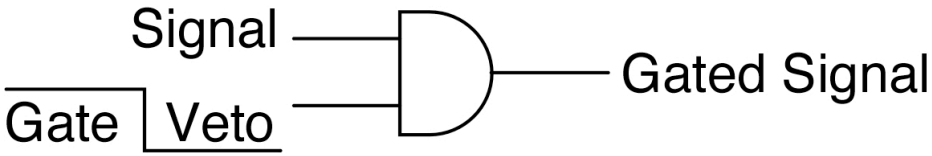
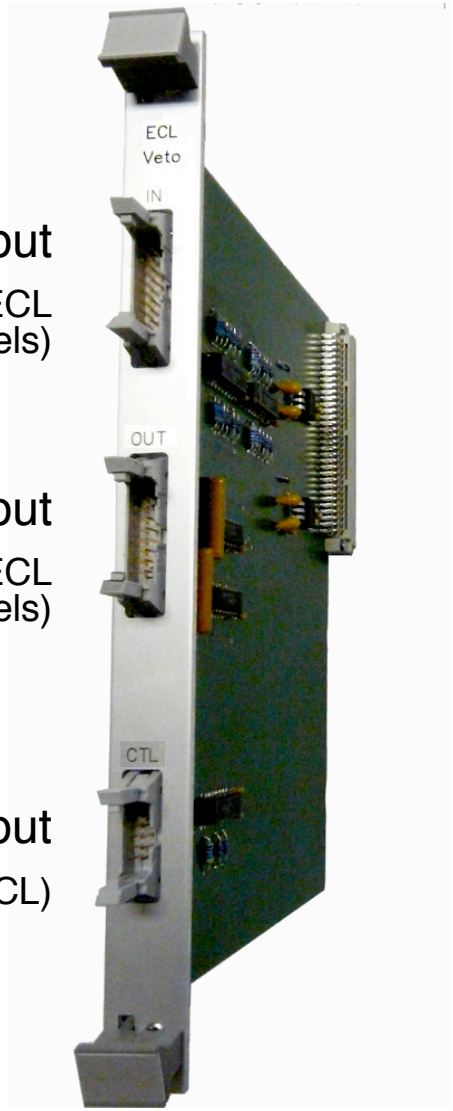
VETO Module (2)

Designed and built on-purpose.

Simple gating function:



… may as well be used as OR (common test) with inverted polarities



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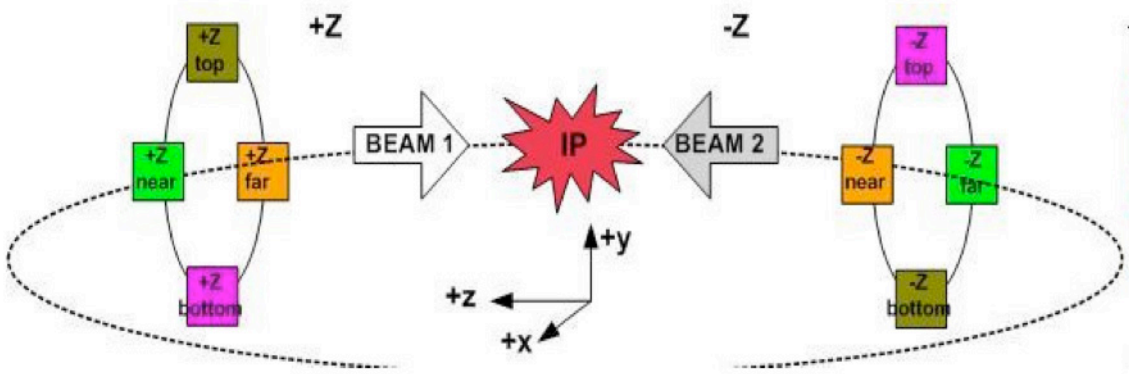
Look Up Table (1)

- Back-to-back trajectories allow estimation of luminosity
- Count coincidence rates between opposite sensors of BCM1
- Timing is in 1st approximation identical - same distance from I.P. (6ns time of flight)



A: -z TOP & +z BOTTOM
B: +z TOP & -z BOTTOM
C: +z NEAR & -z FAR
D: -z NEAR & +z FAR

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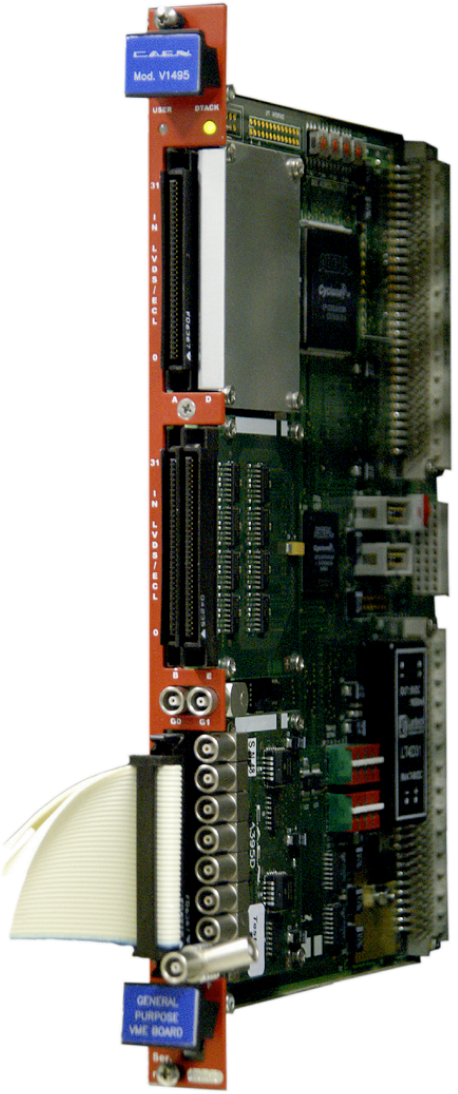
Look Up Table (2)

- General Purpose I/O Register v1495 (CAEN)
- 6U VME module with up to 6x32 channels in LVDS/ECL or TTL/NIM standard
- User configurable FPGA & several delay circuits on board
- 40MHz system clock



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Look Up Table (3)

current functionality:

- Feed 8 digitized sensor inputs (diff. ECL) to the input
- Process 4 coincidences

  (and/or more functions such as synchronisation;

  selection is subject to user accessable registers)
- Provide 4 diff. ECL outputs to (external) scalers

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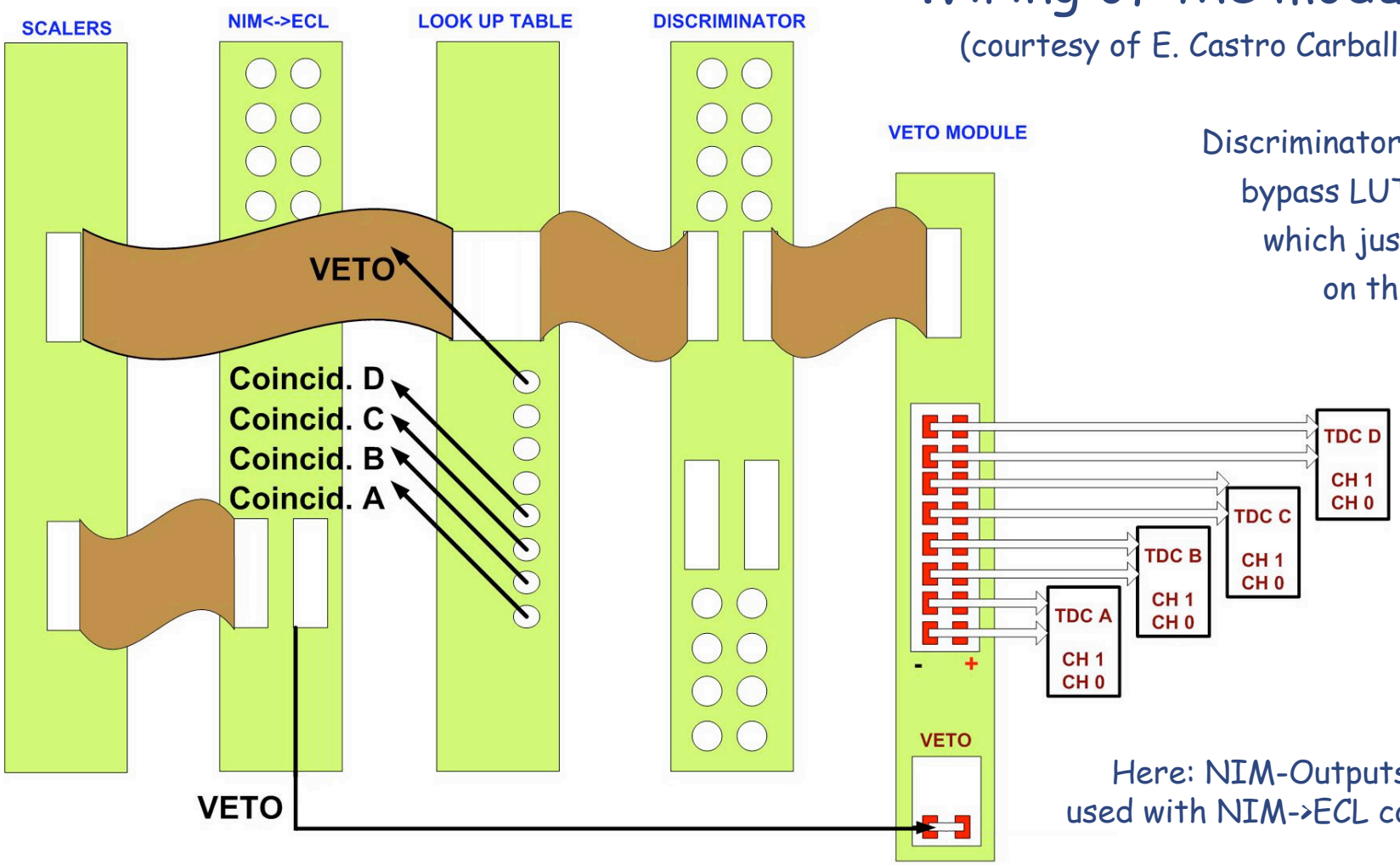
Wiring of the modules

(courtesy of E. Castro Carballo)



Discriminator outputs bypass LUT module which just 'spies' on the signals

Here: NIM-Outputs of LUT used with NIM->ECL converter

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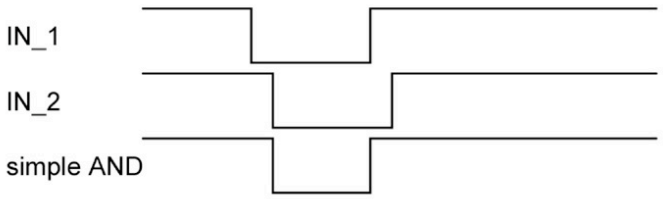
Look Up Table (4)

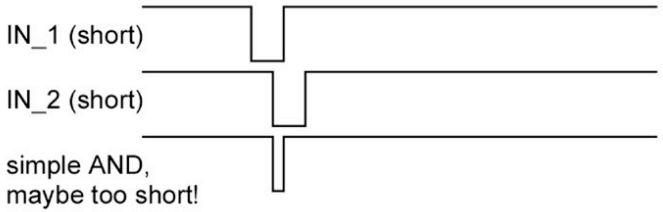
simple analog

OR

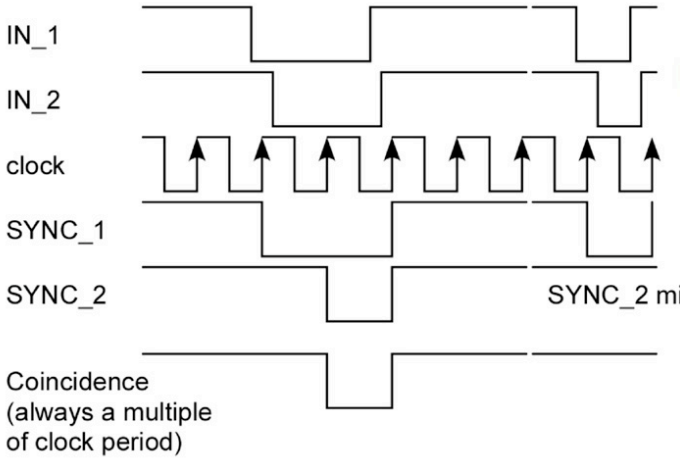
synchronized coincidence



Building a coincidence by simple logic AND function.



Problems when inputs are short and/or displaced in time!



Building a coincidence from synchronized input signals.

Problems when inputs are shorter than the clock period!

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Look Up Table (5)

- Programming of the module functionality in VHDL
- Compiling with manufacturer's software
- Flashing the module's non-volatile memory
  (Handler © M. Ohlerich/ R. Schmidt)
- Function is in effect after power-on

```
--#######################################
-- Lookup table
--#######################################

 SYNC: process(nLBRES,LCLK,DET_IN,BNCH_CLK)
   begin
       if nLBRES = '0'  then                    -- reset
         SYNC_IN <= X"00";
       elsif  LCLK'event and LCLK='1' then      -- run on LCLK clock
        if UNIT_MODE = '1' then                 -- sync to internal clock
          SYNC_IN <= DET_IN;
       else                                     -- don't sync
             SYNC_IN <= DET_IN;
       end if;
     end if;
   end process;

 LUT: process(nLBRES,LCLK, SYNC_IN, COIN_OUT)
   begin
     if nLBRES = '0'  then                      -- reset
       COIN_OUT(3 downto 0) <= X"0";
     elsif  LCLK'event and LCLK='1' then        -- run on LCLK clock
       -- mapping checked with updated wiki table (04feb10):
       COIN_OUT(0) <= SYNC_IN(0) and SYNC_IN(5);  -- -Top+Bot
       COIN_OUT(1) <= SYNC_IN(1) and SYNC_IN(4);  -- -Bot+Top
       COIN_OUT(2) <= SYNC_IN(2) and SYNC_IN(3);  -- -Out+Inn
       COIN_OUT(3) <= SYNC_IN(6) and SYNC_IN(7);  -- -Inn+Out
     end if;
     OR_OUT <= COIN_OUT(0) or COIN_OUT(1) or COIN_OUT(2) or COIN_OUT(3);
 end process;

--#######################################
```

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Look Up Table (6)

Additional features:

- Provide the gating signal for the VETO module by means of a dedicated register, which is written by the BCM1F operation program
- Latch the Beam Abort signal in a dedicated register, which is read by the BCM1F operation program

Possible extensions:

- Process more (or different) coincidences
- Implement the scalers for all coincidences
- Directly link the VETO to the DRDY signal of the TDC (exclude software interaction)
- Receive and multiplex other common LHC signals such as triggers

BCM1F 'B.T.O.' Modules

Summary

Two 'built to order' resp.'programmed to order' modules have been successfully implemented into the readout system of the BCM1F:

- an on-purpose designed and manufactured ECL gating module and
- a versatile programmable commercial module.

Extensions of it's functionality are possible and planned.