

External FPGA interface for high throughput multi-channel event timers

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PICOQUANT

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PicoQuant



Pulsed Diode Lasers



Time-resolved Confocal Microscopes & LSM upgrade kits

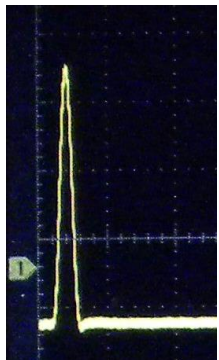


Photon Counting Instrumentation



Fluorescence Lifetime Spectrometers

What is “event timing”?



Voltage pulse:

- Single photon detectors
- Trigger diodes
- Pulse generators

...



Trigger:

- Level trigger
- Constant fraction discriminator (CFD)

...

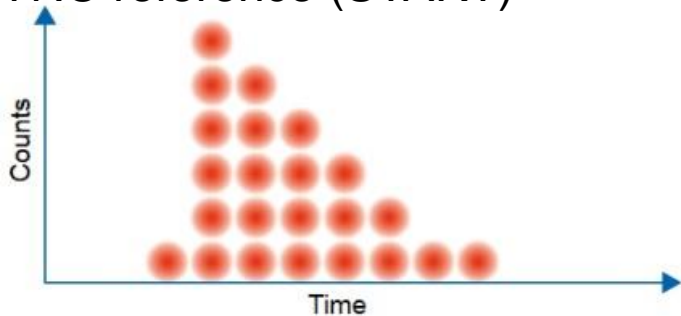


Picosecond time measurement
(Time-to-digital converters, TDC)
+ output of measured data

What is “event timing”?

Histogramming mode

Histograms of time differences between detector pulse (STOP) and SYNC reference (START)



Time Tagging modes (T2/T3)

List of time tags for each events

T2:

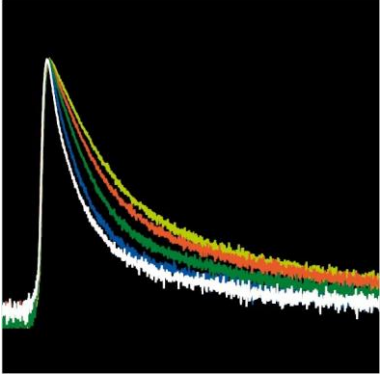
- Absolute times
- Channel info

T3:

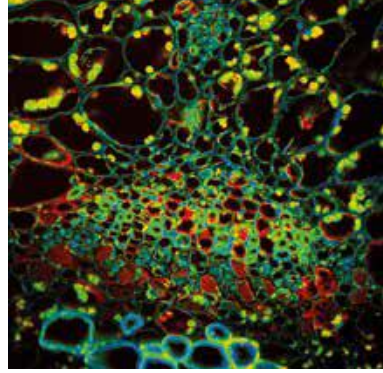
- START-STOP time difference
- Number of elapsed SYNC pulses
- Channel info

record#	chan	timetag	truetime/ps
0	CHN 1	82278	411390
1	CHN 1	282272	1411360
2	CHN 1	482281	2411405
3	CHN 1	682281	3411405
4	CHN 1	882274	4411370
5	CHN 1	1082276	5411380
6	CHN 1	1282276	6411380
7	CHN 1	1482285	7411425
8	CHN 1	1682280	8411400
9	CHN 1	1882281	9411405
10	CHN 1	2082281	10411405
11	CHN 1	2282280	11411400
12	CHN 1	2482267	12411335
13	CHN 1	2682269	13411345
14	CHN 1	2882287	14411435
15	CHN 1	3082285	15411425

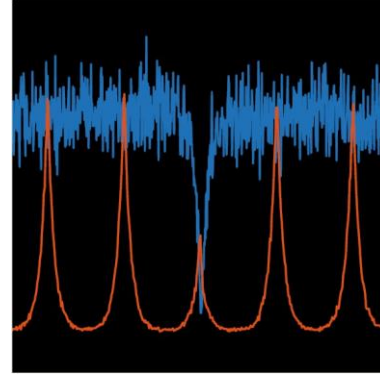
Applications for event timer



Time-resolved luminescence



Lifetime imaging



Temporal correlations

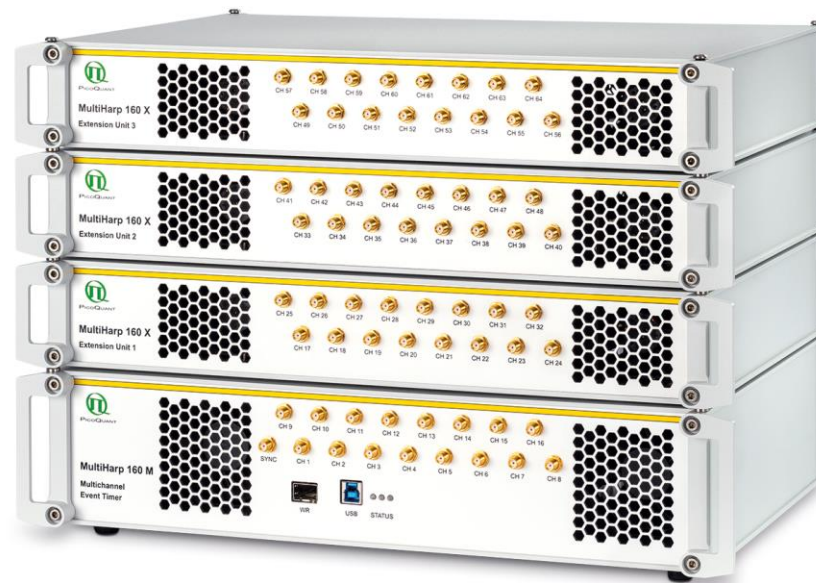


Time-of-Flight LiDAR / Ranging

Increasing demand for multiple (16+) synchronized timing channels (e.g. image scanning microscopy, diffuse optical tomography, optical quantum technologies, ...)

Scalable Multichannel Event Timer & TCSPC Unit “MultiHarp 160”

- **Up to 64 independent input channels
(assembled in units of 16)**
 - + 1 independent Sync channel
- 5 ps temporal resolution
- Single channel jitter <32 ps rms
- 650 ps dead time
(adjustable up to 160 ns)
- Device synchronization via marker inputs,
Ref In/Out
- Native White Rabbit interface
- USB 3.0 interface



USB Limitation: Bandwidth

MultiHarp 160

TDC Sync

TDC Ch. 1-8

TDC Ch. 9-16


TDC Ch. 17-32

.

.

.

TDC Ch. 57-64

 80 Mcps
(T2/T3)

USB 3
Interface

To PC

**Bandwidth limit
of USB 3 interface:**

- 80 Mcps sustained throughput
- 64+1 input channels:
~1 Mcps per channel
on average

**Data processing in PC
can further limit the
throughput!**

USB Limitation: Latency

MultiHarp 160

TDC Sync

TDC Ch. 1-8

TDC Ch. 9-16

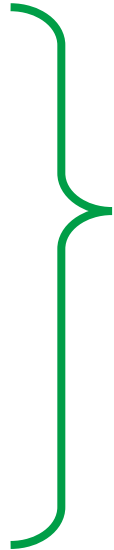
TDC Ch. 17-32

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.

TDC Ch. 57-64



USB 3
Interface

→ To PC

**Latency limit
of USB 3 interface:**

→ Neither USB 3.0 in bulk mode nor the involved Hardware and Software on the host side typically satisfy real-time requirements

Data flow

MultiHarp 160

TDC Sync

TDC Ch. 1-8

TDC Ch. 9-16

TDC Ch. 17-32

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TDC Ch. 57-64



Data pre-processing goals:

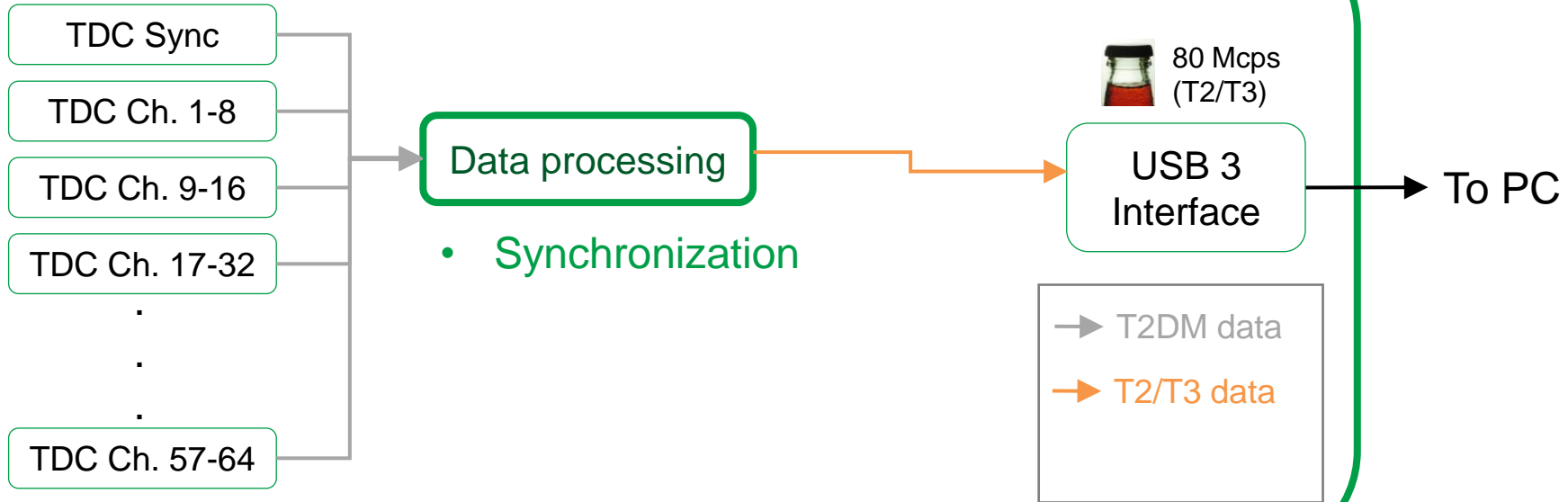
- Reduced data size
- Less processing steps by PC

USB 3
Interface

To PC

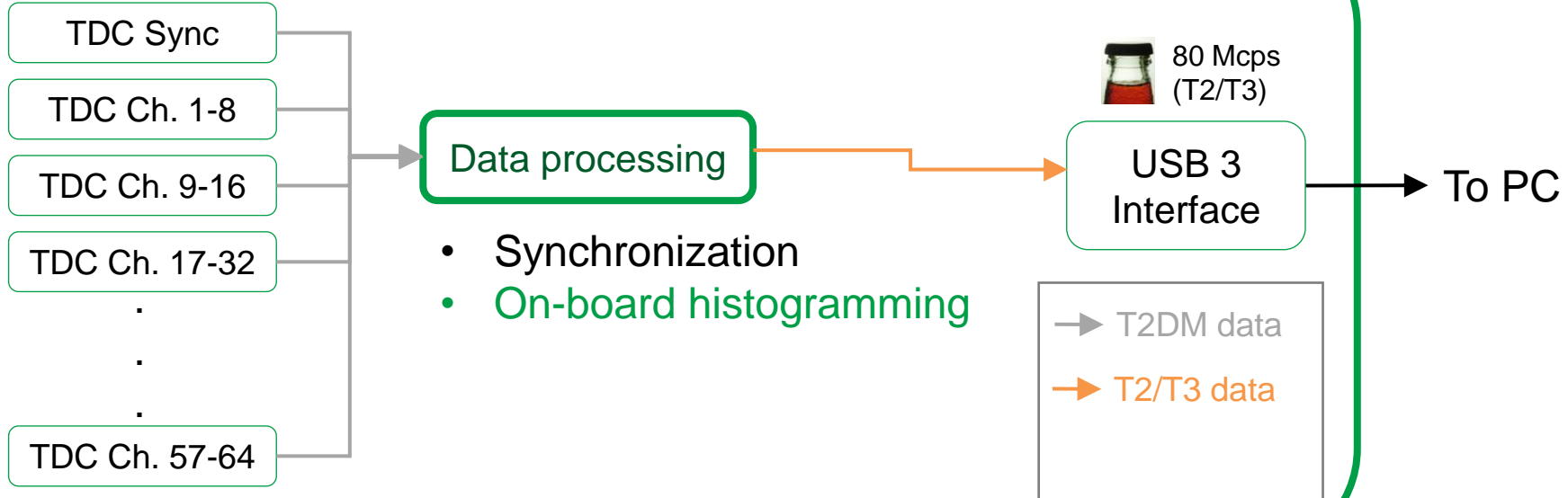
On-board data processing

MultiHarp 160



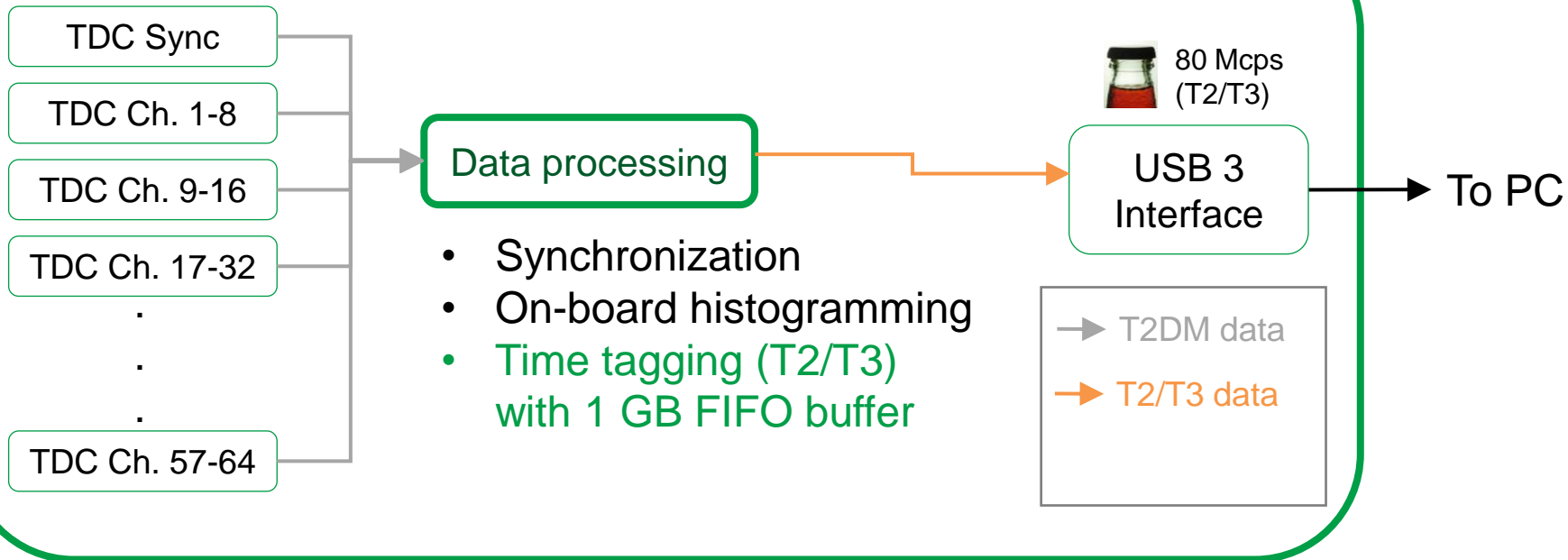
On-board data processing

MultiHarp 160



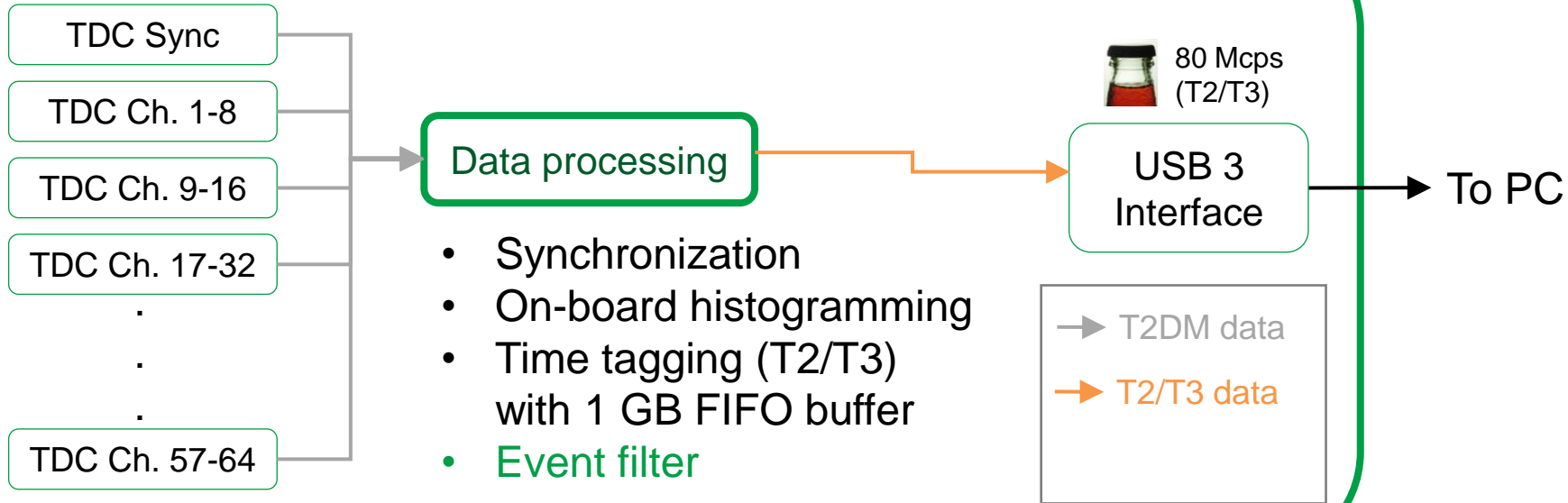
On-board data processing

MultiHarp 160



On-board data processing

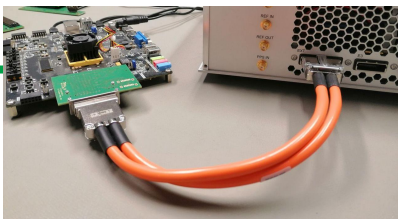
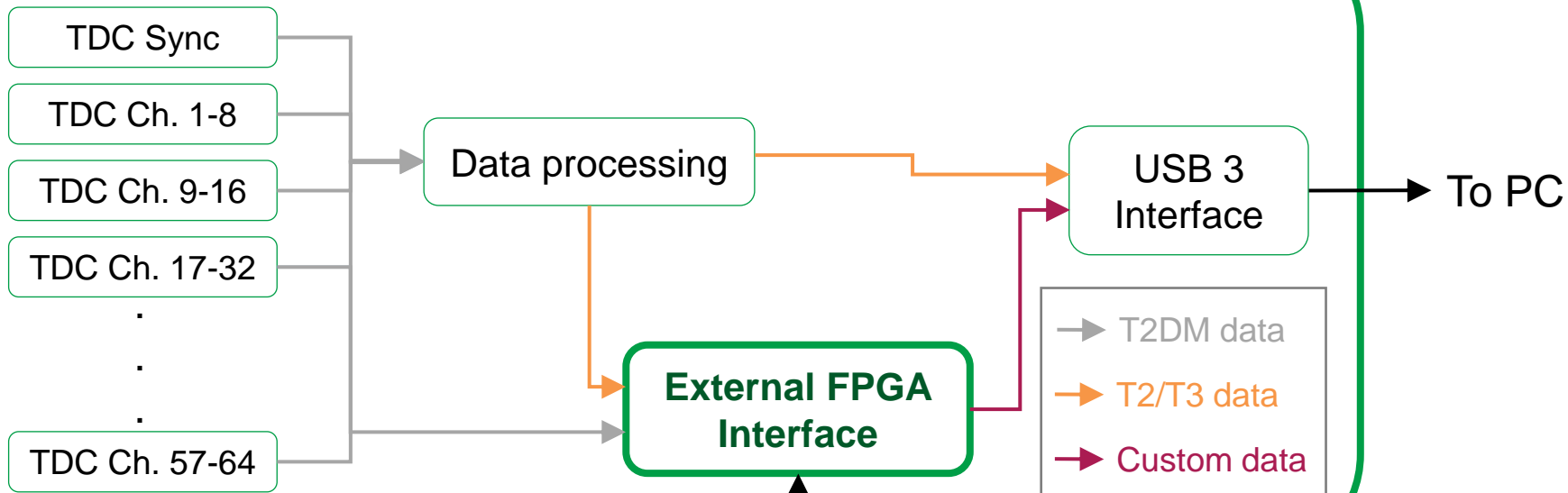
MultiHarp 160



But: Optimal processing is application-specific!

External FPGA interface (EFI)

MultiHarp 160

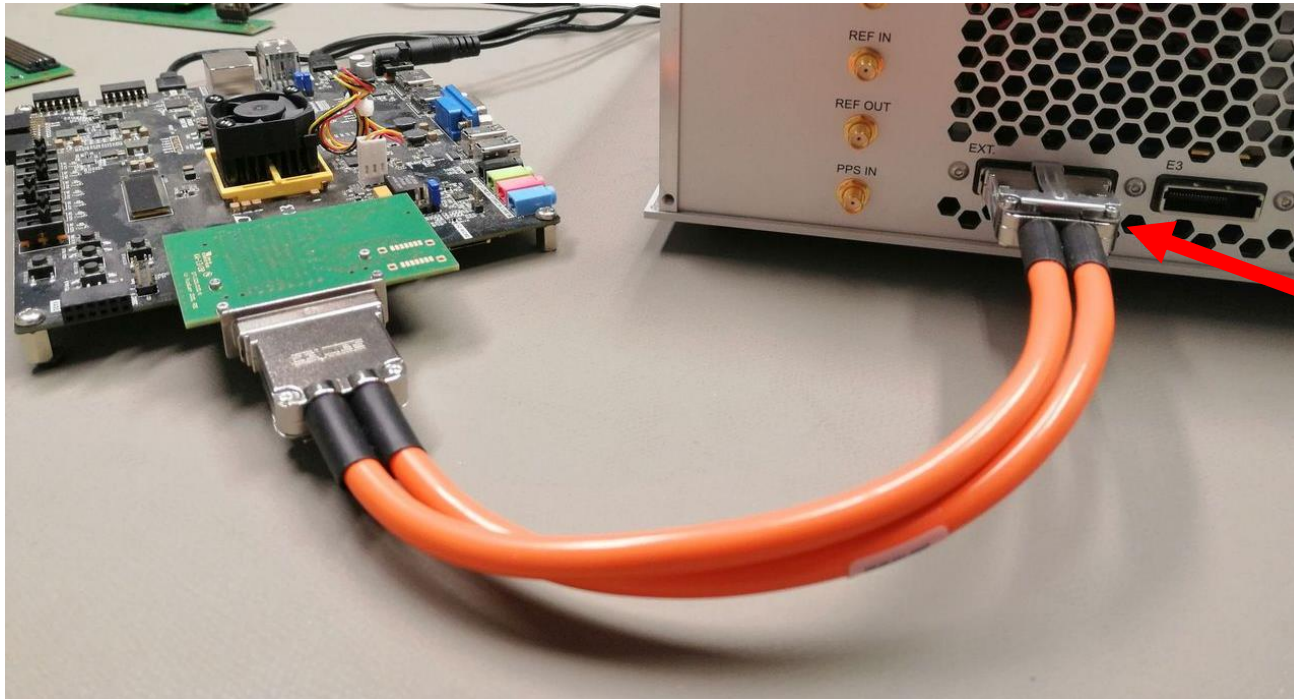


High speed serial I/O

External FPGA interface (EFI)

- High speed serial link for fast data transfer between MultiHarp 160 and external FPGA
- Enables custom tailored on-the-fly processing of time tags

external
FPGA



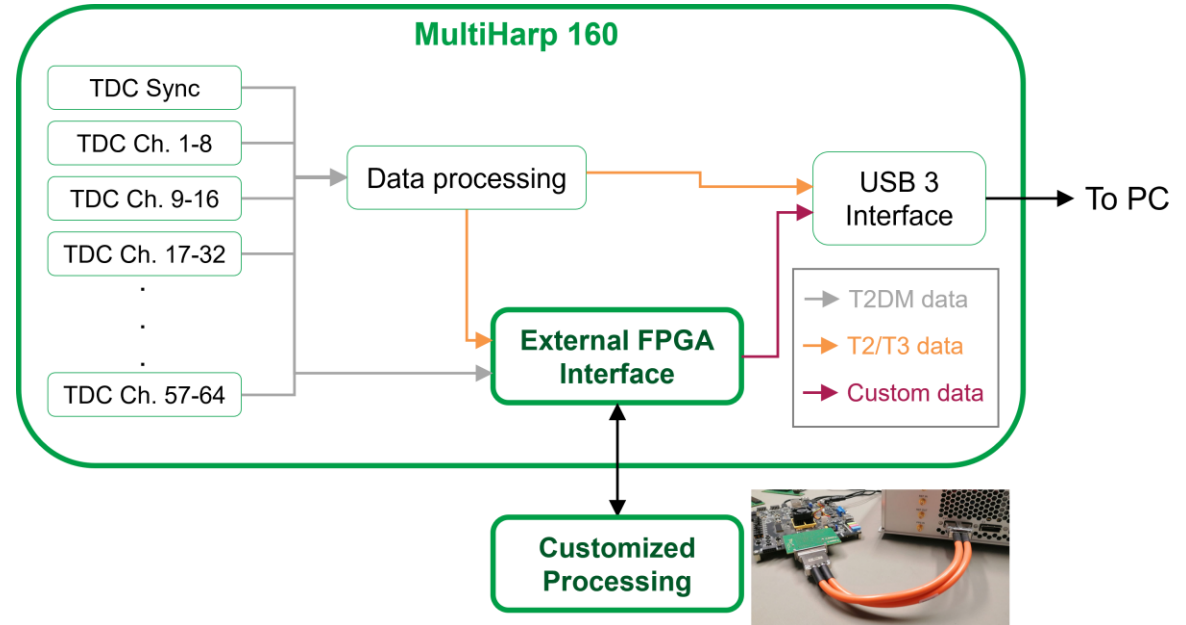
MultiHarp 160 M
back side

FPGA interface

External FPGA interface (EFI)

T2/T3 data via EFI:

- Up to 200 million events/sec
- Latency: 4.5 to 5.5 μ s



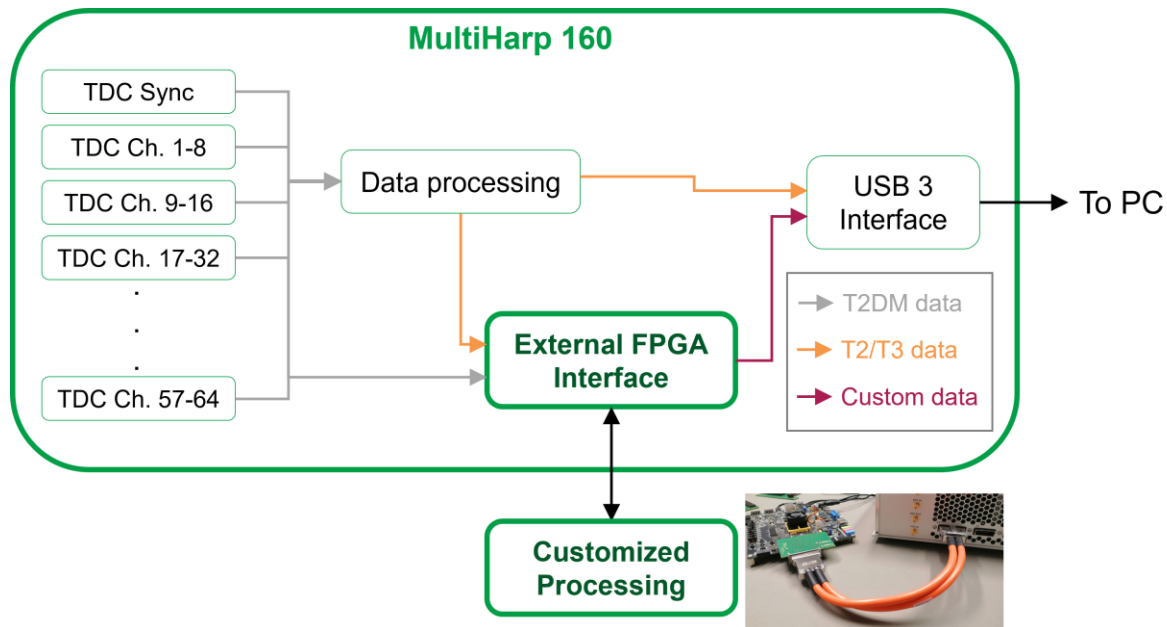
External FPGA interface (EFI)

T2/T3 data via EFI:

- Up to 200 million events/sec
- Latency: 4.5 to 5.5 μs

T2 Direct Mode via EFI:

- Up to 200 million events/sec per row of 8 inputs + full SYNC input data rate
(Total = 1.6 G events/sec)
- SYNC latency: 1.7 to 1.8 μs
- Latency other inputs: 0.8 to 1.2 μs



EFI – An open development platform

- Interface is based on the open Aurora standard
- Xilinx offers a free to use Aurora 8b/10b IP core for most FPGAs
- PicoQuant provides an example design for the Digilent Genesys 2 FPGA
- The package is written in VHDL and contains simulation testbenches and step-by-step instructions for the setup



Download the EFI example package here:



Take home messages

MultiHarp 160: PicoQuant's newest multichannel event timer

- Scalable up to 64 channels with 5 ps digital resolution and <650 ps dead time
- On-board data-processing (histogramming mode, T2/T3 time tagging modes, event filters)
- External FPGA interface:
 - By-passing the bottlenecks of USB bandwidth & data processing in software
 - Enables customized processing of events on external FPGAs for novel applications
 - Low latency data transfer down to microseconds and below
 - Data rates up to 1.6 billion events per second
 - Get started quickly with the EFI example design package