Phase1 pixel upgrade simulation:

Seeding efficiency for iterative tracking
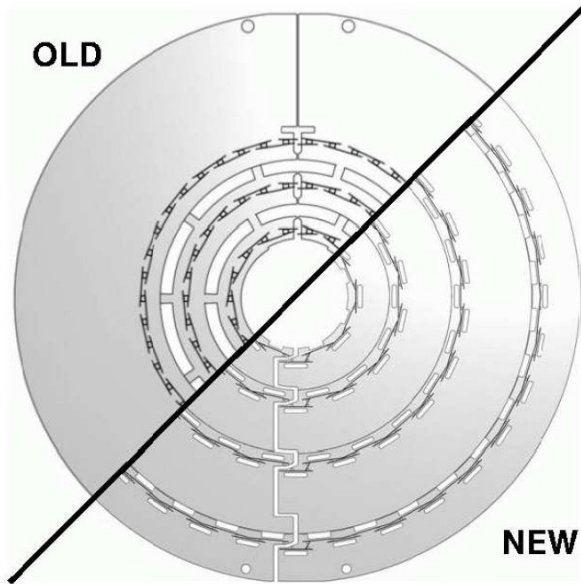

Quadruplet tracking in HLT

M. Aldaya, J. Olzem
DESY

Phase1 pixel upgrade

Phase1 upgrade -
- upgrade to 4 BPix layers / 3 FPix disks
- expect improved vertex / IP resolution
- investigate b-tag performance for:
  - HLT (pixel only tracks)
  - "offline" (full tracker)
- CMSSW_336, full simulation, ttbar & qcd
- participate in Phase1 Upgrade Technical Proposal (due Sep. 2010)

Current CMSSW tracking code cannot fully cope with 4 BPIX / 3 FPIX layers

→ several modifications necessary:

- replaced HLT (pixel-only) track fitting algorithms (for fitting 4 hits to a track)
- implemented modules for creating 4-hit track seeds from triplets
- removed quirks in Phase1 geometry
- ...
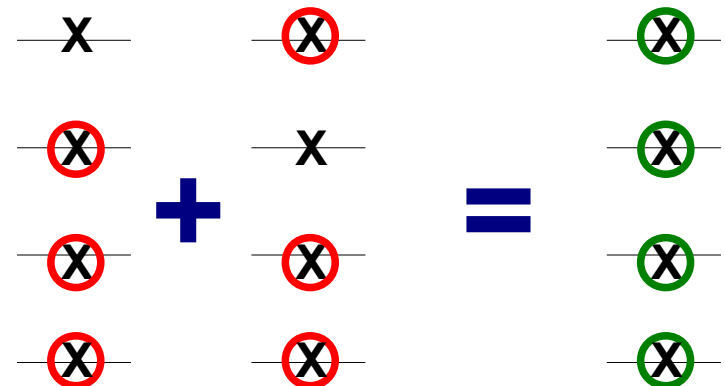
Seeding efficiency for iterative tracking
- all silicon tracker -

Simulation:
- Fullsim CMSSW_3_3_6
- R39F16 phase1, geometry tag 28, std. pixel size
- Process: 6k ttbar, pu0 & pu25 (no jet pT range defined)

- **3-hit seeds** on phase1 geometry ("3-out-of-4") yet
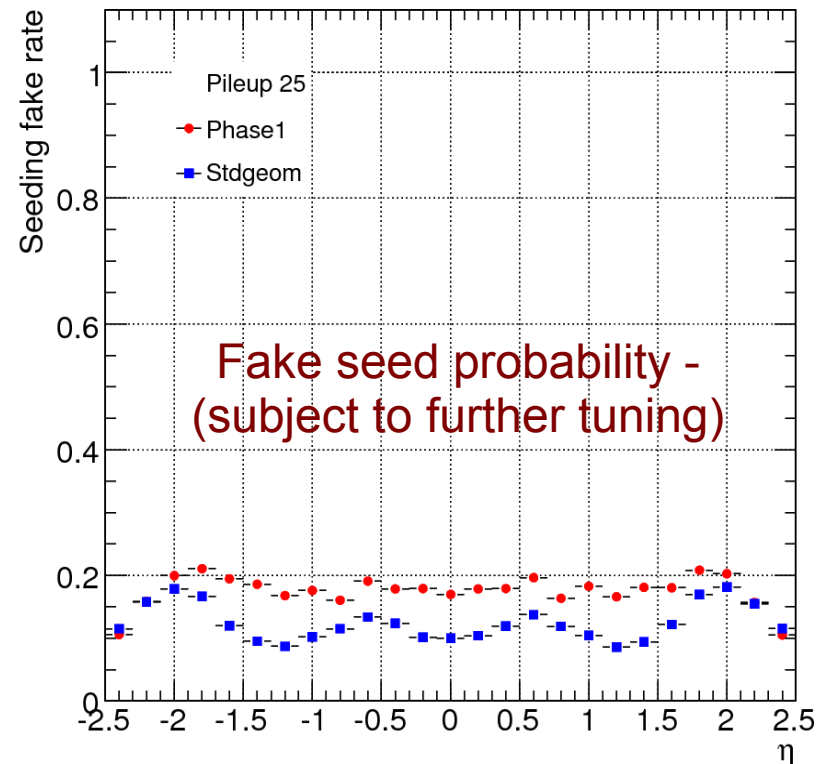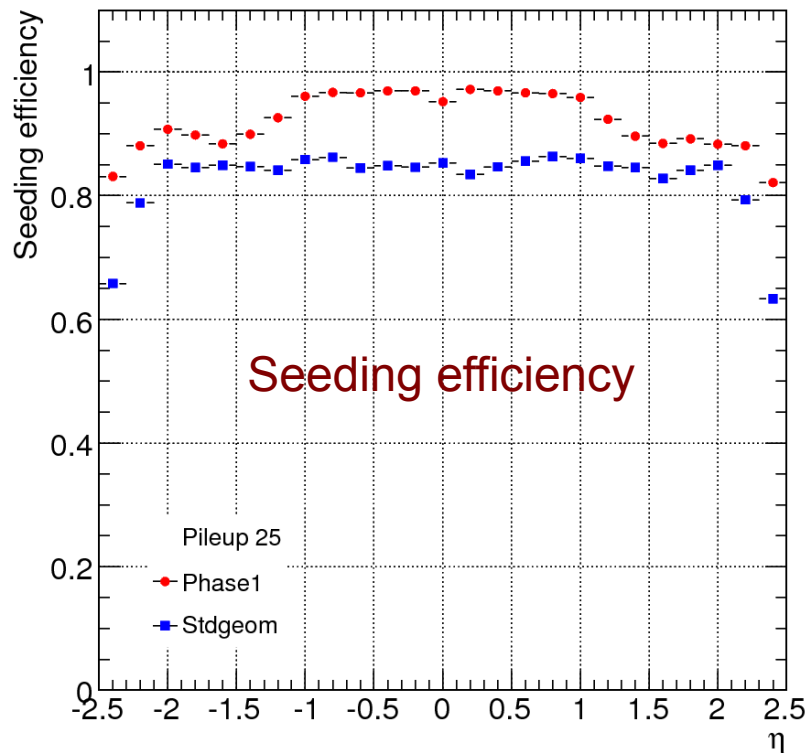- **quadruplet seeding** being commissioned & investigated

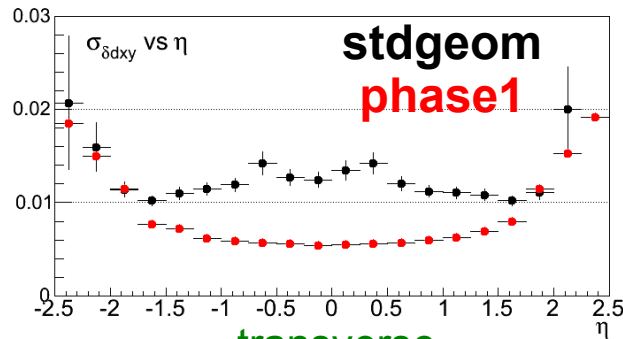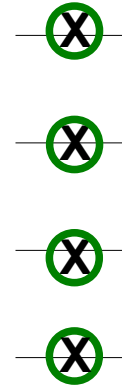→ plots for inclusion in upgrade TP (for LHCC)

Seeding efficiency

Pileup 25
Phase1
Stdgeom

Fake seed probability -
(subject to further tuning)
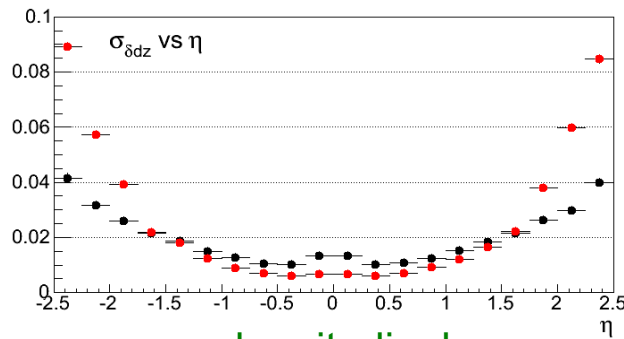
Pileup 25
Phase1
Stdgeom

Quadruplet tracking in HLT
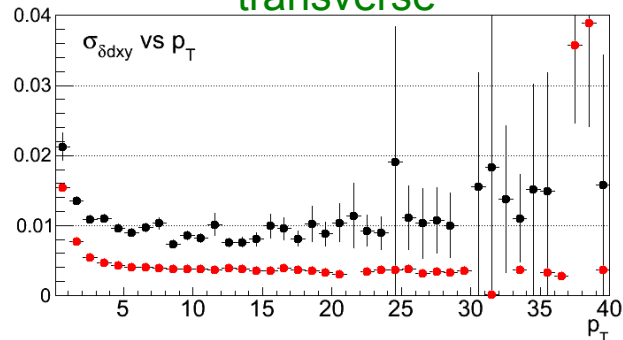## - pixel-only -

- For pixel-only HLT tracking:
  Quadruplet ("4-out-of-4") seeding & tracking already **in place**

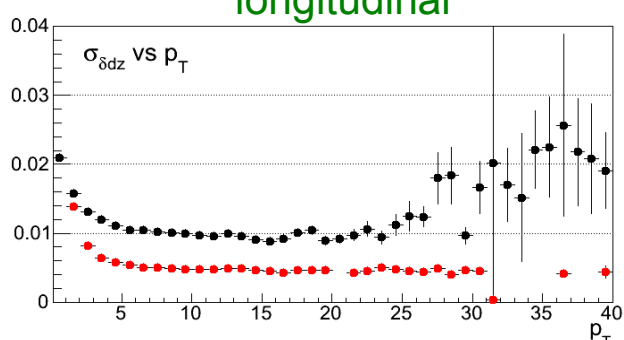- See **significant improvement** in track reconstruction ...
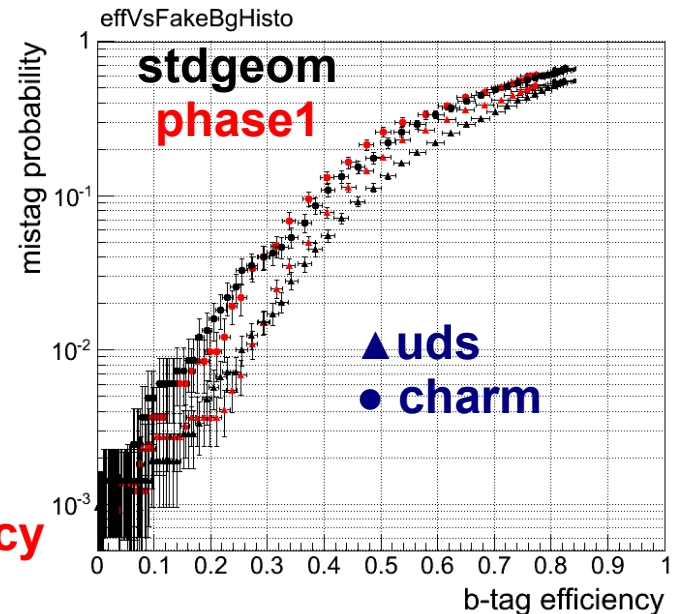

transverse
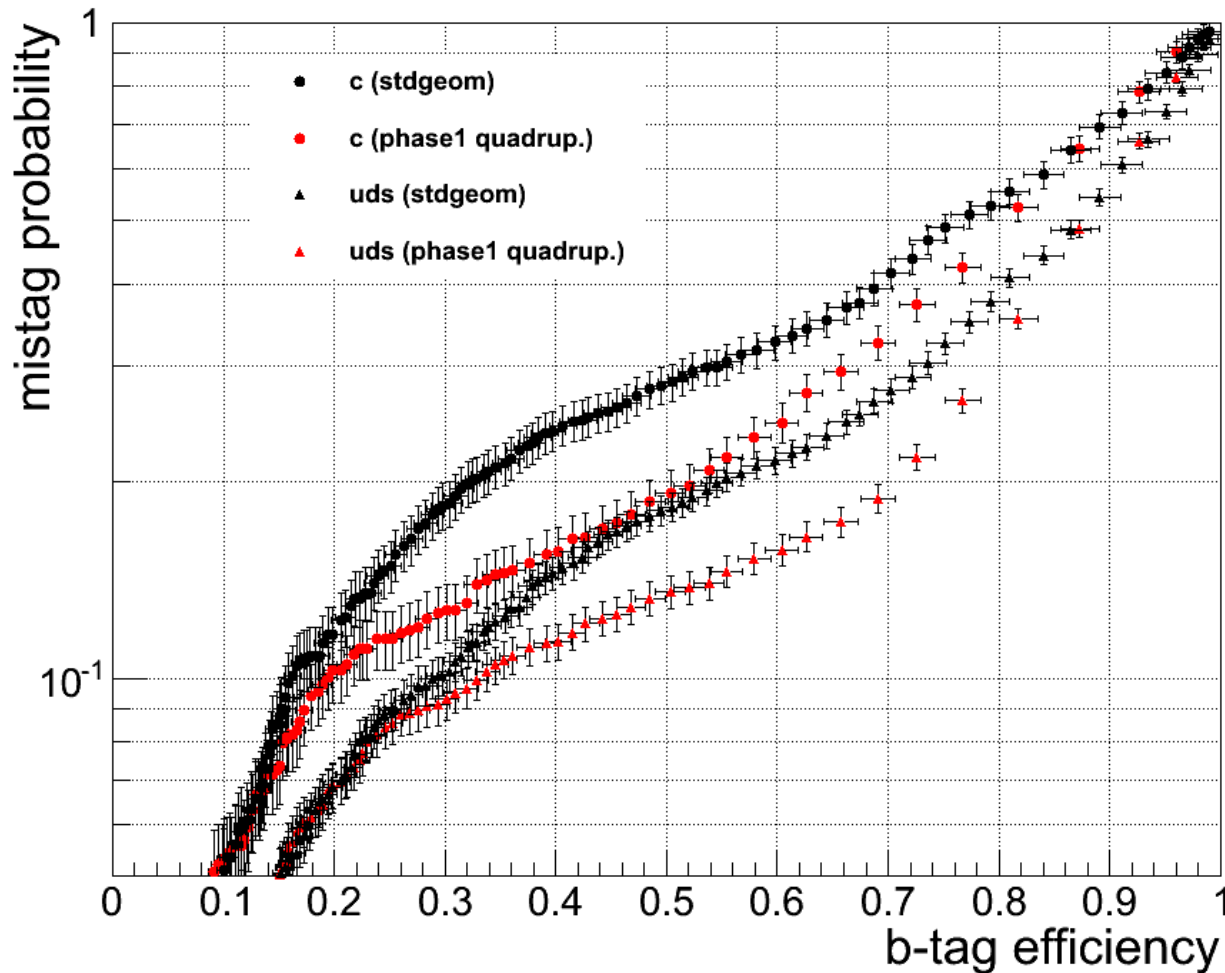
longitudinal

impact parameter resolution

… but no improvement in b-tagging efficiency

HLT quadruplet tracking

Wrote standalone b-tagging algorithm (based on track-counting 3D high efficiency algo)

- Siginificantly better efficiency ./. fake
- To be improved by further tuning

→ More places in CMSSW tracking code where the current geometry is implicitly hard-coded

→ downstream of the IP calculation (`TrackIPProducer` or B-Tagging modules)

→ several 1000 lines of code to be investigated