Overview on the Tangerine MLR1 Chip

First 65nm CMOS Pixel Detector developed at DESY

Gianpiero Vignola & Tangerine group Hamburg, 02 Mar 2022



HELMHOLTZ



Tangerine Project overview

First half of 2020

- **Goal**: Design a monolithic pixel detector in 65nm CMOS imaging technology
 - Main application: beam telescope
 - **Potential applications**: linear collider experiments, etc.
- Requirements:
 - Position resolution: ~ 3µm
 - Rate capabilities: 1 MHz particle rate
 - Time resolution: ~ 1-10 ns
 - Low material budget: < 0.05% X/X₀
 - Energy measurement via ToT
- Founded By InnoPool & DESY
- Tangerine project start in Sep. 2020





Why Monolitic Active Pixel Sensor?

In 65 nm CMOS imaging process

- Reduce: Material budjet, Production cost & Complexity
- Recent improvements thanks ALICE ITS:
 - Small collection electrode (reduce noise and power consumption order ~ 40 mW cm⁻²)
 - Spatial resolution ~ 5 μ m
 - 180 nm CMOS process
- 65 nm process allow:
 - Higher logic density → small pixel pitch and/or increase in-pixel functionality
 - further decrease in power consumption
- Three processes available for the sensitive volume design: Standard, Modified, Modified with N-gap



MLR1 production

Second half of 2020, first half of 2021

- Multi Layer Reticle 1 divided up into "sites" of 1410x1410 μm for different test chips shared between DESY, CERN, RAL, Nikhef, etc.
- TJ 65nm ISC Process limitations in MLR1:
 - Only 3+1 metal layer
 - 10µm epitaxial layer
- MLR1 timetable:
 - Design submitted
 01-Dec-2020
 - GDS files approved 15-Dec-2020
 - MLR1 at CERN

June 2021



Tangerine MLR1 Chip Details

Cini

Become familiar with the 65 nm process

2 CSAs with different gains

- a) feedback cap 1.5fF \rightarrow 107 $\mu\text{V/e}$
- b) feedback cap 2.0fF \rightarrow 80 $\mu\text{V/e-}$
- Use Charge injection as stimulus
- No Pixel diode
- Aim: Evaluation of CSA performance

Block of 2x2 pixel with CSA

- **Gain**: 80 μ V/e- , Cf = 2fF (typ)
- Sensing node: nwell hexagon 1.2µm diameter
- **Pitch**: 16 µm
- outputs: 4 analog read-out
- Aim: Pixel characterization



Tangerine MLR1 Chip at DESY

October 2021

- MLR1 Chip arrived at DESY in early October
- different samples, same structure with slightly different doping profiles (details not known)
- In the meantime, the Tangerine group has grown
- Chip glued and bonded on DUT board (designed and ready at DESY)
- ASIC designers carry out the first tests on CSAs comparing them with simulations Evaluation of: Gain, Delay, Rise Time, Falling edge
- First waveforms obtained with Fe⁵⁵ source





Fe⁵⁵ source studies



Example reported:

- Sample ID: 4 pixel 0
- Exposure time: ~ 1 night
- # Trigger: 6929 (all 4 channels)
- Thresholds: 20 mV over noise

Signal amplitude Expected:

(@ Christian Reckleben)

- K_{α} : 5.8 keV \rightarrow ~ 1590 e-
- @ Cf = 2fF $\pm 10\% \rightarrow \sim 127 \text{ mV}$
- Gain 1.33 \rightarrow ~ 168 mV ±10%



DESY Test Beam

18 Oct - 01 Nov 2021

Setup / Data taking

- Oscilloscope based Read-out of 4 pixels
- Few event per hour expected
- Two data taking used

Veto Scintillator Mode

- 3 scintillator used (one with hole) combined with NIM logic
- Trigger rate few Hz (>99% of junk data)
- Efficiency studies possible

Scope used to trigger the telescope

- Scope trigger delay not relevant for mimosa
- Event rate 1 event every 5-15 minutes

@ L. Huth





DESY Test Beam: Results

18 Oct - 01 Nov 2021

- Most populated run in 2 weeks: **110 events**
- only low statistic preliminary results:
 - MIP response order of 50 mV
 - Rise time 5-10 ns
 - Slew rate on the order of mV/ns
 - Noise fluctuations
- Main outcomes:
 - gained confidence with the Chip
 - rate too low at DESY Facility



@ F. Feindt

CERN Test Beam

SPS 10 - 15 Nov 2021

Setup / Data taking

- Oscilloscope based readout
- Timepix3 reference telescopes
- Trigger as input to SPIDR DAQ +
 offline sync
- 120 Gev pions, High intensity 1e6 per spill

Results

- Scope trigger correlate nicely in time → time resolution ~ 2.4 ns
- Thanks to the excellent spatial resolution of the telescope, the pixel structure is recognizable
- Also in this case few events for hour, event rate extremely lower than expected!

@ L. Huth & A. Simancas











MLR1 Real Chip

Explanation for the low efficiency of the chip

- The very low rate at DESY and CERN prompted an in-depth analysis of the MLR1 chip
- After Interactions with CERN people involved in MLR1 production, a sensor layout issue in DESY MLR1 Chip was found
- TCAD simulations confirmed that the chip cannot perform as expected
- The expected efficiency is now ~ 0.5%
- The observed rates now make sense but there was not enough beam time to collect sufficient statistics

Doping Concentration





Mainz Test Beam

MAMI Microtron 02 – 06 Dec 2021

- Electron energy: 855 MeV
- Beam Imax: ~ 100 µA
- Beam size: ~ 1mm²
- Trigger: provided by MLR1 (scope)
- Tigger rate: Few Hz
- Recorded events: > 500k











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Mainz Test Beam: Results

Waveform Analysis with ROOT

- Tested Sample #4 & sample #7
- IB5U scan (amps bias current) 4-14 μ A (VB5U 0.65 1.4 V)
- VSUB scan (pwell sub voltage, sensor cathode) 1.25 2.2 V

140.0

120.0

100.0

80.0

60.0

40.0

20.0

0.0

0.6

0.7

0.8

0.9

Mean Time over Threshold Sample #7

1.1

VB5U (V)

■Pix0 ◆Pix1

▲Pix2

▲ Pix 3

1.2 1.3 1.4 1.5







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Mainz Test Beam: Results

Corryvreckan Analysis



- ALPIDE busy time caused misalignment between telescope and MLR1 data and made resynchronization necessary
- Residuals (Difference between positions from track interpolation and DUT meas) ~ 6µm is dominated by ALPIDE resolution and low beam momentum







@ F. Feindt

Conclusions

Results with the tangerine MLR1 Chip

- A 65 nm CMOS pixel detector was for the **first time** developed & investigated at DESY
- DESY MLR1 Chip allowed the first tests on designed CSAs with the direct study of the waveforms
- The Chip shows a time resolution of 2-3 ns with MIPs (preliminary)
- Spatial resolution of a few µm for MLR1 (considering the sensor layout issue and the small pitch)
- Results of the studies on MLR1 will allow improvements in the **next prototype**



Tangerine project present & future

Towards the next prototype

- MLR1 is just the beginning of the story
- The Tangerine group is now focused on TCAD and Allpix² simulations
- The ASIC design of the next prototype(s) is in the final stages of preparation for submission
- The next Chip with larger matrix and digital read-out is expected at DESY by the end of 2022



Slides presented in Tangerine meetings

Thank you

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