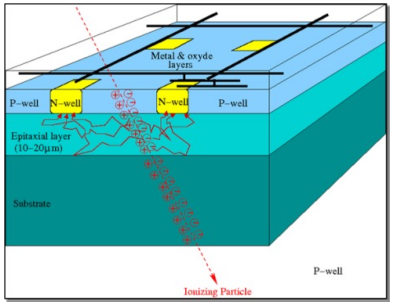
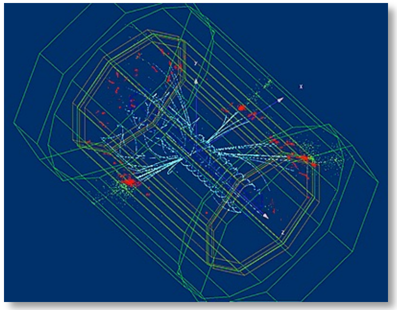
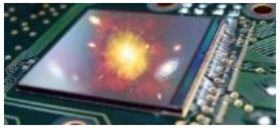
Towards a vertex detector suited for a future Higgs Factory based on CMOS pixel sensors



Ziad EL BITAR, Auguste BESSON



On behalf of the
PICSEL group & C4PI Platform



PICSEL

C4PI-Platform

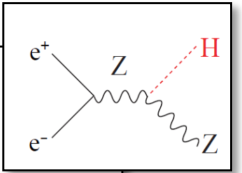
Outline

- Introduction: requirements & strategy
- MIMOSIS chip development (IPHC-IKF-GSI Collaboration)
- 65 nm R&D (with CERN EP R&D WP 1.2 & ALICE ITS-3)
- Stitching and bending
- Conclusion & Synergies in CMOS R&D

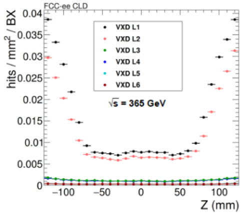
	Z	Higgs	ttbar
√s [GeV]	91.2	240	365
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	230	8.5	1.7
no. of bunches / beam	16640	393	48
Bunch separation (ns)	20	994	3000

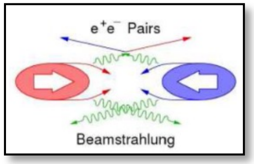
Higgs Factory Vertex detector requirements

Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks
- ⇨ Vertex/Jet charge determination



Vertex barrel





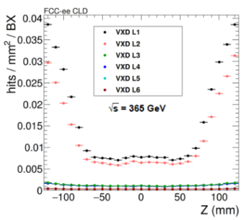
Physics O(Hz/cm²)

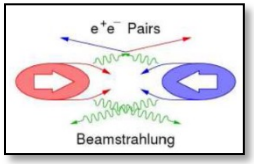
Beam background O(10-50 MHz/cm²)

	Z	Higgs	ttbar
√s [GeV]	91.2	240	365
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	230	8.5	1.7
no. of bunches / beam	16640	393	48
Bunch separation (ns)	20	994	3000

Higgs Factory Vertex detector requirements

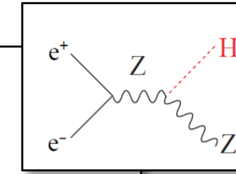
Vertex barrel





Physics O(Hz/cm²)

Beam background O(10-50 MHz/cm²)



Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks
- ⇨ Vertex/Jet charge determination

Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17-20 μm
- ⇨ (σ_{sp} ~3-4 um)

Material Budget
- ⇨ ~ 0.15% X_0 / layer
- ⇨ < 1% X_0 for the whole VTX
- + ~0.3 % X_0 for the beam pipe
- + 0.15% X_0 for 5 μm Gold coating

Low material detectors & supports structures

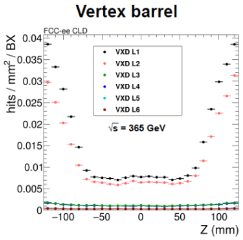
$$\sigma_{d_0} = a \oplus \frac{b}{p sin^{\frac{3}{2}}\theta}$$

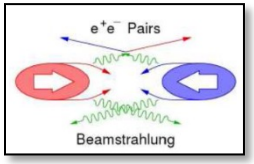
$a \simeq 5\mu m$ $\quad b \sim 15\mu m.GeV$ @FCCee

$b \sim 10\mu m.GeV$ @ILC

	Z	Higgs	ttbar
$\sqrt{s}$ [GeV]	91.2	240	365
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	230	8.5	1.7
no. of bunches / beam	16640	393	48
Bunch separation (ns)	20	994	3000

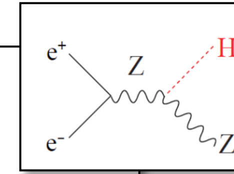
Higgs Factory Vertex detector requirements





Physics O(Hz/cm²)

Beam background O(10-50 MHz/cm²)



Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks
- ⇨ Vertex/Jet charge determination

Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17-20 µm
- ⇨ (σ_{sp} ~3-4 um)

Material Budget
- ⇨ ~ 0.15% X_0 / layer
- ⇨ < 1% X_0 for the whole VTX
- + ~0.3 % X_0 for the beam pipe
- + 0.15% X_0 for 5 µm Gold coating

Low material detectors & supports structures

$$\sigma_{d_0} = a \oplus \frac{b}{p\sin^{\frac{3}{2}}\theta}$$

$a \simeq 5\mu m$ $b \sim 15\mu m.GeV$ @FCCee

$b \sim 10\mu m.GeV$ @ILC

Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Time resolution
O(1 µs)

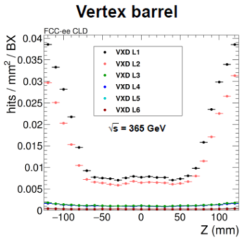
Power consumption
~< 50mW/cm²

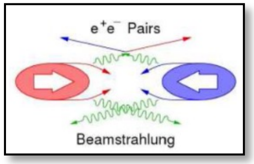
Fast read-out & low Power Architectures (~ 20 mW/cm²)

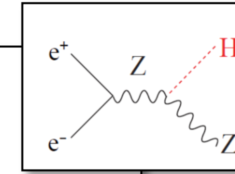
Power pulsing (ILC) vs continuous beam (FCCee)

	Z	Higgs	ttbar
$\sqrt{s}$ [GeV]	91.2	240	365
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	230	8.5	1.7
no. of bunches / beam	16640	393	48
Bunch separation (ns)	20	994	3000

Higgs Factory Vertex detector requirements







Physics
- Flavour tagging
- Low pT tracks
- Vertex/Jet charge determination

Physics O(Hz/cm²)

Beam background O(10-50 MHz/cm²)

Vertex reconstruction
- granularity
- Pitch ~17-20 µm
- (σ_{sp} ~3-4 um)

Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Material Budget
- ~ 0.15% X_0 / layer
- < 1% X_0 for the whole VTX

+ ~0.3 % X_0 for the beam pipe
+ 0.15% X_0 for 5 µm Gold coating

Time resolution
O(1 µs)

Low material detectors & supports structures

Power consumption
~< 50mW/cm²

Fast read-out & low Power Architectures (~ 20 mW/cm²)

Cooling
Stiffness / Alignment

$$\sigma_{d_0} = a \oplus \frac{b}{p sin^{\frac{3}{2}}\theta}$$

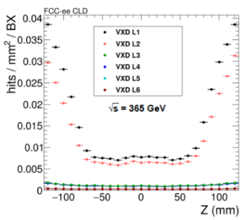
$a \simeq 5\mu m$ $b \sim 15\mu m.GeV$ @FCCee
$b \sim 10\mu m.GeV$ @ILC

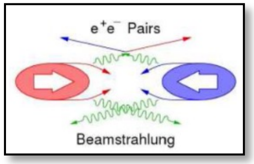
Power pulsing (ILC) vs continuous beam (FCCee)

	Z	Higgs	ttbar
$\sqrt{s}$ [GeV]	91.2	240	365
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	230	8.5	1.7
no. of bunches / beam	16640	393	48
Bunch separation (ns)	20	994	3000

Higgs Factory Vertex detector requirements

Vertex barrel



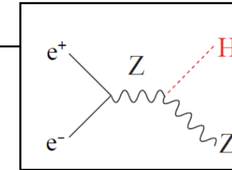


Physics O(Hz/cm²)

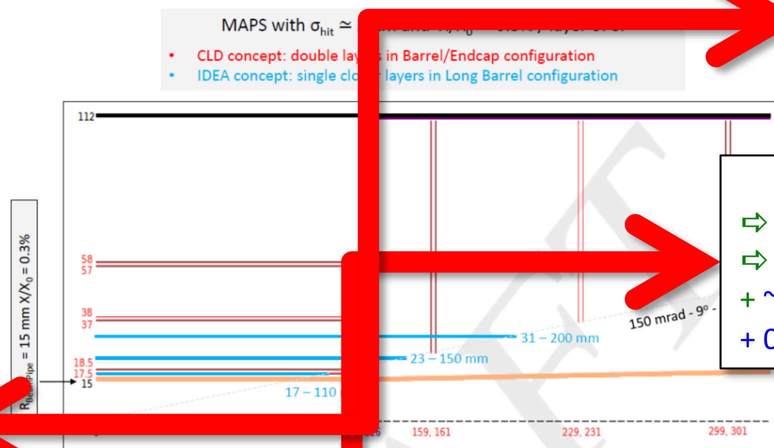
Beam background O(10-50 MHz/cm²)

CLD and IDEA Vertex Detectors designs (superimposed)

Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks
- ⇨ Vertex/Jet charge determination



Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17-20 μm
- ⇨ (σ_{sp} ~3-4 um)



(Figure: D. Contardo)

Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Time resolution
O(1 μs)

Power consumption
~< 50mW/cm²

Fast read-out & low Power Architectures (~ 20 mW/cm²)

Power pulsing (ILC) vs continuous beam (FCCee)

Cooling
Stiffness / Alignment

Material Budget
- ⇨ ~ 0.15% X_0 / layer
- ⇨ < 1% X_0 for the whole VTX
- + ~0.3 % X_0 for the beam pipe
- + 0.15% X_0 for 5 μm Gold coating

Low material detectors & supports structures

$$\sigma_{d_0} = a \oplus \frac{b}{p sin^{\frac{3}{2}}\theta}$$

$a \simeq 5\mu m$ $b \sim 15\mu m.GeV$ @FCCee

$b \sim 10\mu m.GeV$ @ILC

5 single layers or 3 double layers ?

Inner (1.7 cm or lower ?) and outer radius are key factors

Design, build and exploit CMOS pixels sensors
with <u>low material budget</u> & <u>high granularity</u>
In order to contribute to the construction of a vertex & a tracking detector in a Higgs factory.

Approach the Higgs factories vertex detector requirements

MIMOSIS chip family (180 nm)

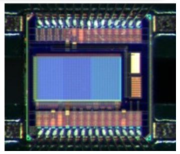
Maintain & develop the know how to build sensors to be installed in real experiments

Input for detector simulations

Optimize the parameters of the technology (e.g. sensitive layer)

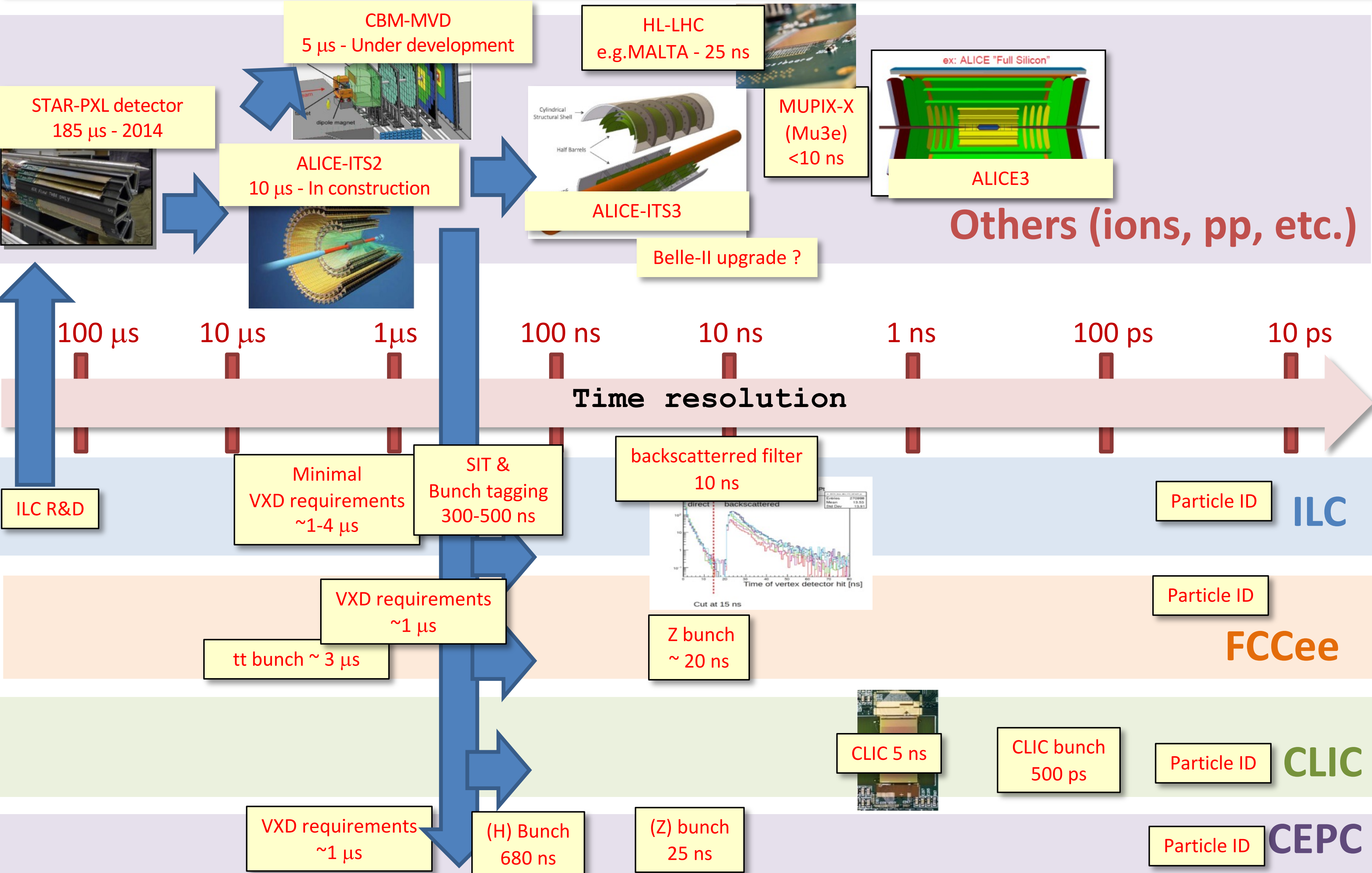
Exploit fully the potential of the CMOS technology

- R&D 65 nm



- Large surfaces (stitching)
- Bent sensors
- Integration
- Emerging technologies (e.g. double tier)

Time resolution in the context of e^+e^- colliders

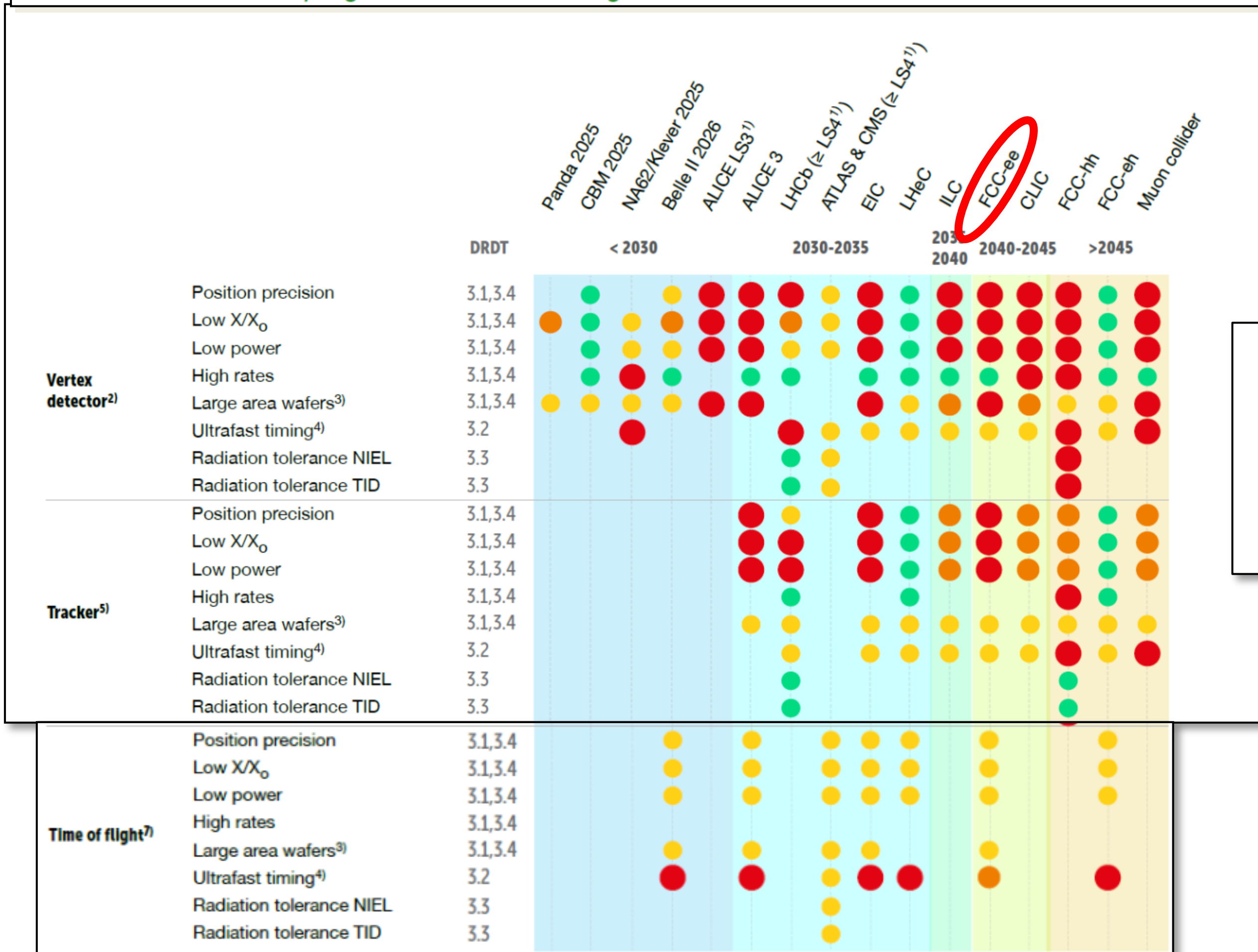


Synergies

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. ***ECFA supports a series of workshops*** *with the aim to* ***share challenges and expertise, to explore synergies in their efforts*** *and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).*

Goal: bring the entire e^+e^- Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

K. Jakobs, FCC Physics Workshop, Feb 2022

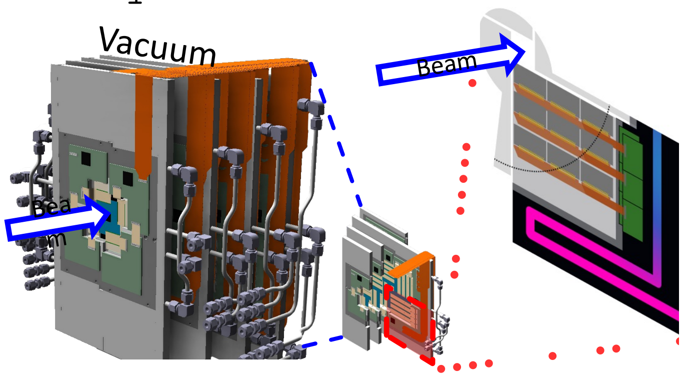


Must happen or main physics goals cannot be met · Important to meet several physics goals · Desirable to enhance physics reach · R&D needs being met

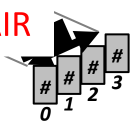
Important similarities between FCCee requirements & Heavy ions experiments (ALICE ITS3, ALICE3, EIC, etc.)

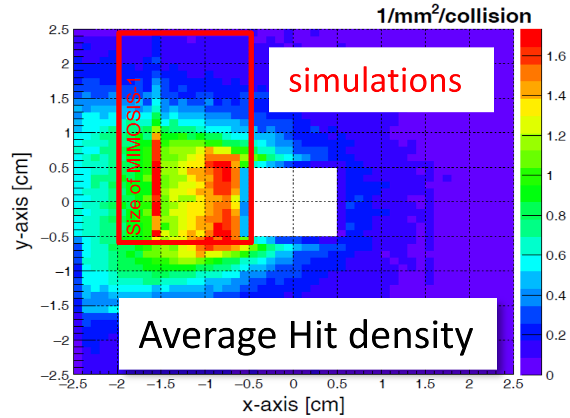
MIMOSIS requirements

- Requirements



CBM-MVD@ FAIR





Physics parameter	Requirements
Spatial resolution	~ 5 um
Time resolution	~ 5 us
Material budget	0.05% X_0
Power consumption	< 100 – 200 mW/cm^2
Operation temperature	- 40 °C to 30 °C
Temp gradient on sensor	< 5K
Radiation tol* (non-ion)	~ 7 x 10^{13} n_{eq}/cm^2
Radiation tol* (ionizing)	~ 5 MRad
Data flow (peak hit rate)	@ 7 x 10^5 / (mm^{2}s) > 2 Gbit/s

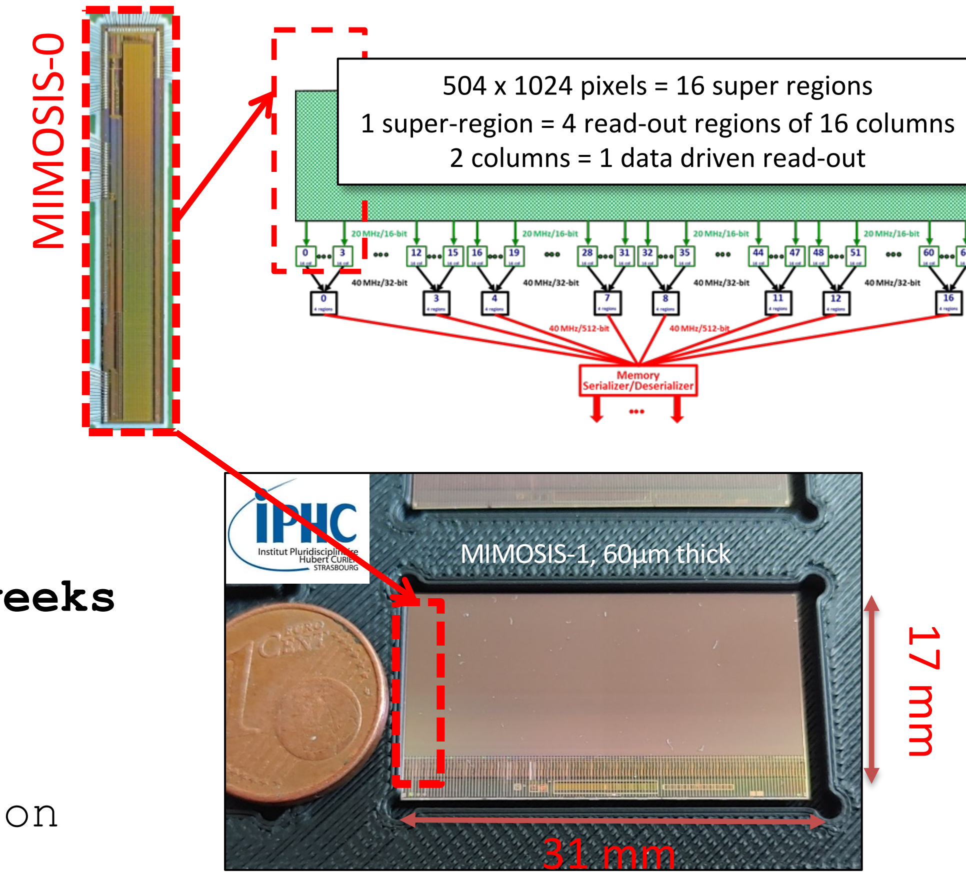
- 4 double-sided thin planar detector stations
- 100 kHz Au+Au @ 11 AGeV and 10GHz p+Au @ 30 AGeV
- Non uniform hit density in time and space
- High radiation environment, operating in vacuum

- MIMOSIS chip
  - ✓ Based on ALPIDE architecture
  - ✓ Discriminator on 27x30µm² pixel
  - ✓ Multiple data concentration steps
  - ✓ Elastic output buffer
  - ✓ 8 x 320 Mbps links (switchable)
  - ✓ Triple redundant electronics

Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	$\sim$25 µm
Epi layer resistivity	$> 1k\Omega cm$
Sensor thickness	60 µm
Pixel size	26.88 µm $\times$ 30.24 µm
Matrix size	1024 $\times$ 504 (516096 pix)
Matrix area	$\approx$4.2 cm^2
Matrix readout time	5 µs (event driven)
Power consumption	40-70 mW / cm^2

MIMOSIS roadmap

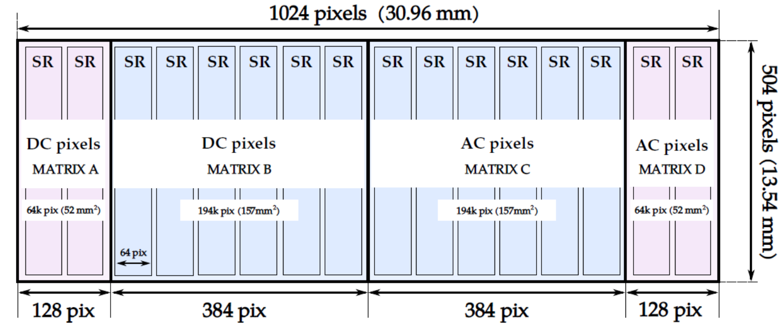
- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - ✓ Tests (2018-2019)
    - Testability
- MIMOSIS-1: 1st full size prototype
  - ✓ Elastic buffer, SEE hardened
  - ✓ Fabricated in 2020
  - ✓ Lab/beam test campaign in 2021
- **MIMOSIS-2: Submission these weeks**
  - ✓ **On-chip clustering**
  - ✓ **Thicker epi layer tests**
  - ✓ **Test prototype for 1 μs readout time**
- MIMOSIS-3: final pre-production sensor
  - ✓ ≥2023

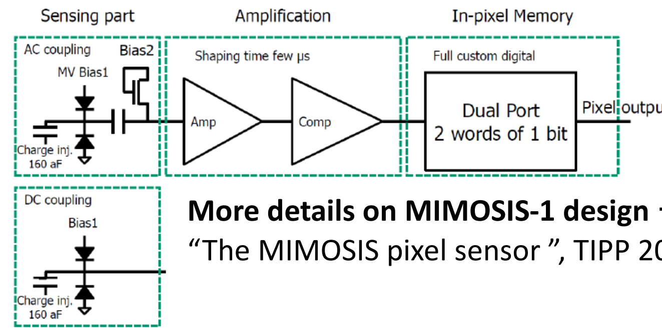


⇨ architecture adaptable to a fast sensor for a FCC vertex detector
⇨ Opportunity to study different designs/options

MIMOSIS-1

- MIMOSIS tests
  - ✓ Submatrices: DC/AC pixels
    - DC pixels: ALPIDE-derived
    - **AC pixels: top bias up to > 20V**
  - ✓ 6 epitaxial variants (18 wafers)
    - Thinned down to 60 µm
    - Study **Yield**
    - Study **charge collection / spatial res.**
    - Explore performances after **irradiation**



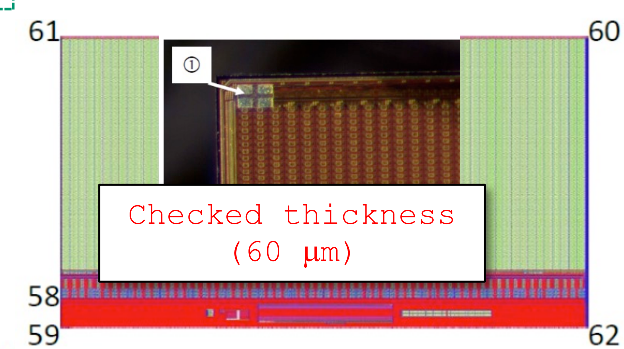


More details on MIMOSIS-1 design → F. Morel, "The MIMOSIS pixel sensor ", TIPP 2021

- Intense test program in 2021:
  - ✓ Laboratory tests
  - ✓ Irradiation tests

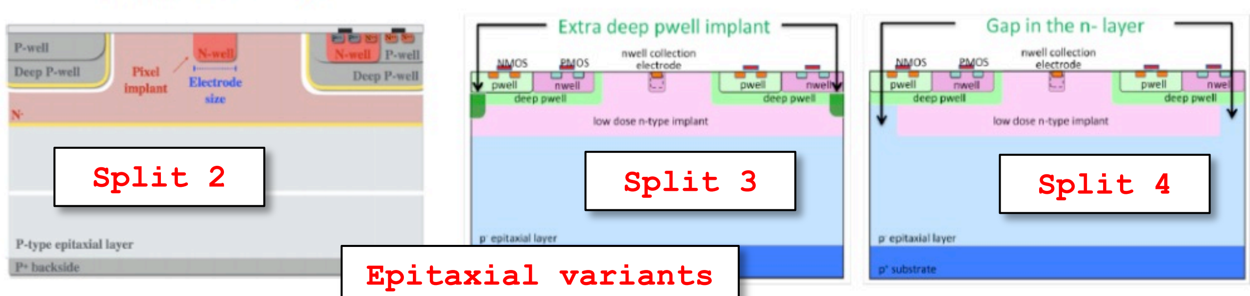
Ljubjana (TRIGA)	~1 MeV reactor neutrons
Karlsruhe (KIT)	~10 keV X-rays

  - ✓ Beam tests @ DESY/CERN (3 campaigns)
  - ✓ Latchup / SEE tests at GSI



- standard process (3 available wafers)
- continuous n-layer (blanket) (3 wafers)
- additional p-implant (3 wafers)
- gap in n-layer (3 wafers)

continuous n-layer — additional p-implant — gap in n-layer

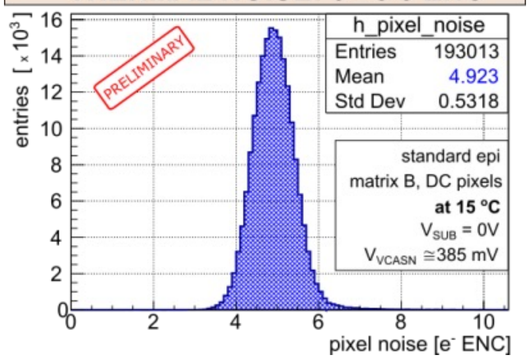


Pic from: Munker, Vertex 2018, Status of silicon detector R&D at CLIC
Carlos, TREDI 2019, Results of the Malta CMOS pixel detector prototype for the ATLAS Pixel ITK

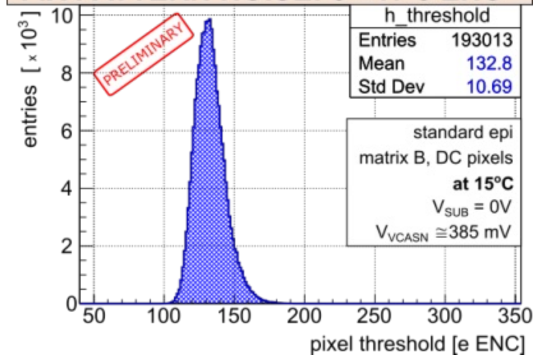
MIMOSIS beam test results

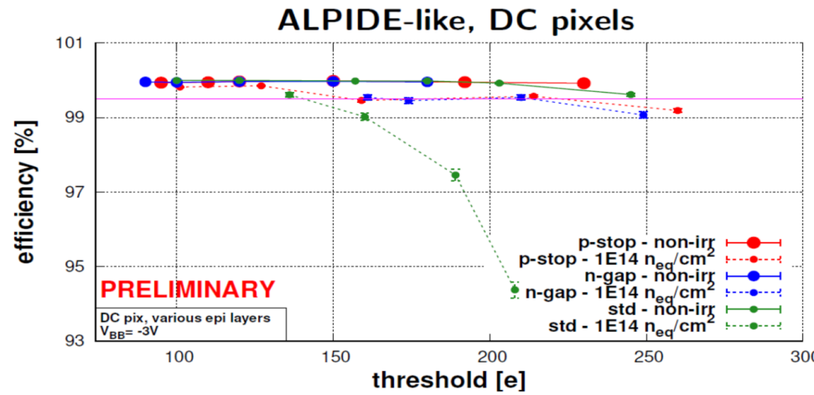
GSI Helmholtzzentrum für Schwerionenforschung

THERMAL NOISE: 3 - 5 e ENC

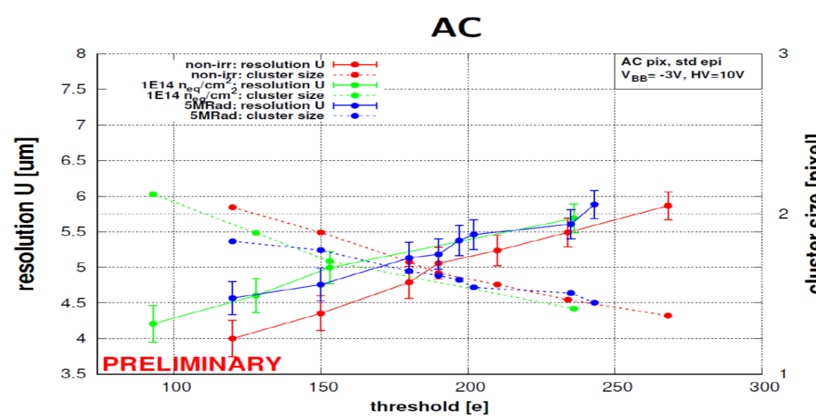


FIX PATTERN NOISE: 5 - 17 e ENC





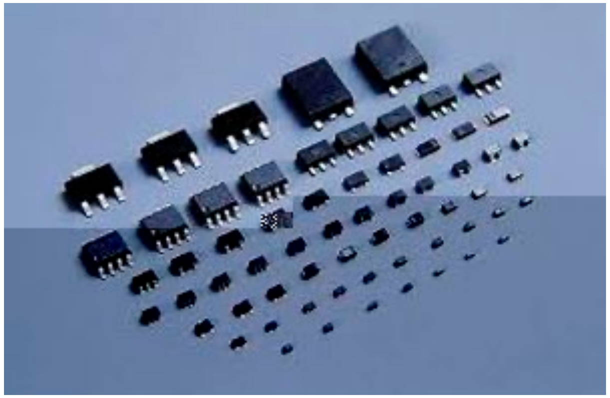
- Noise
  - ✓ DC pixels, no back bias applied) @ room T°C
  - ✓ Pixel Noise ~ 3-5 e⁻ ENC
  - ✓ FPN ~5-17 e⁻ ENC
- Efficiency
  - ✓ ≥ 99.5 %
  - ✓ Time walk correction
- Cluster multiplicity
  - ✓ Typically in the 1-2 range
- Resolution as expected
- Fake rate probably very low
  - ✓ (< 10^{-6}, tbc)

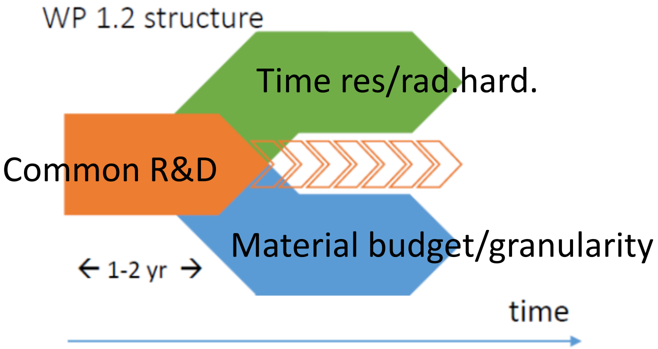


MIMOSIS = a milestone for Higgs factories (5 µm / ≤5 µs)

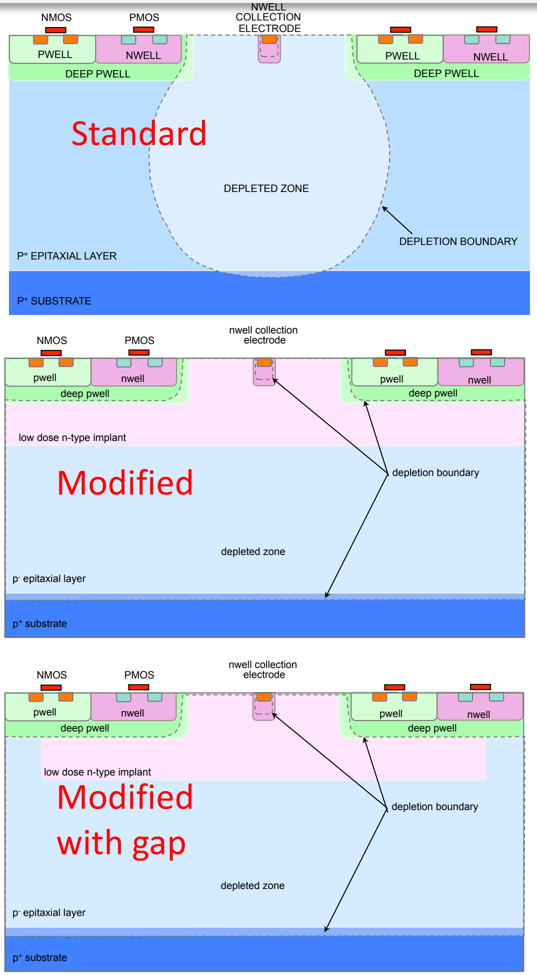
From TowerJazz 180 nm (ALPIDE@ITS2 & MIMOSIS) to TPSCo 65 nm (ITS3)

- 65 nm feature size technology
  - ✓ (ALPIDE & MIMOSIS fabricated in 180 nm)
  - ✓ Larger wafers (⇨ 30 cm)
  - ✓ More functionalities inside the pixel
  - ✓ Keeps pixel dimensions small ⇨ spatial res.
  - ✓ Potentially faster read-out
  - ✓ Lower Power consumption
- **TJ-65 nm available** (since June 2020)
  - ✓ Main driver: CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades (involves other labs) ⇨ LS3 ~ 2024-26
  - ✓ Different requirements
    - EP: time resolution and radiation tol.
    - ALICE: granularity and material budget
    - Common R&D during the 1st years.





The search for the optimal variant : depletion and doping



- ✓ 3 process variations for depletion control:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)
- ✓ 4 process splits:
  1. **Default**
  2. First intermediate optimization
  3. Second intermediate optimization
  4. **Fully optimized process**
- ✓ Lower power consumption
- ✓ Possibly better radiation harndess

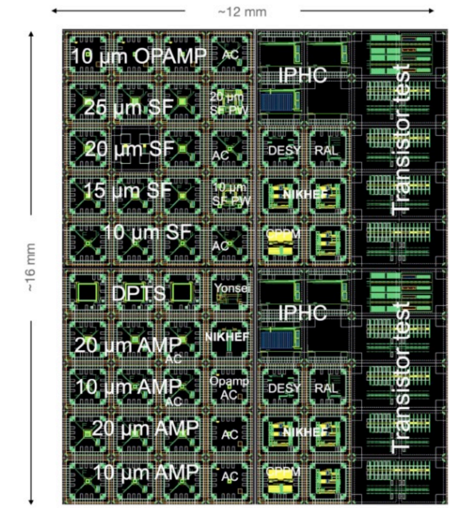
⇨ First submission: MLR1 (Q4 2020)

⇨ Synergy with Higgs factories requirements

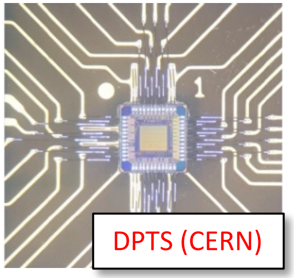
⇨ Relation with foundries and access to options is a key factor

65nm MLR1

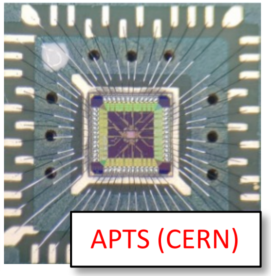
- Technology exploration
- Various pixel matrices and test structures
  - ✓ Radiation test structures
  - ✓ Amplification, DACs, LVDS, etc.
  - ✓ Pitch 15-25 um
  - ✓ Epi variants



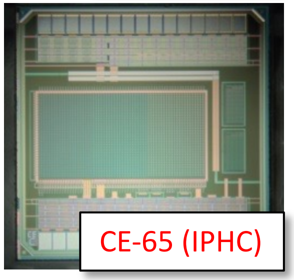
IPHC, CERN, DESY, NIKHEF, Ral, Yonsei



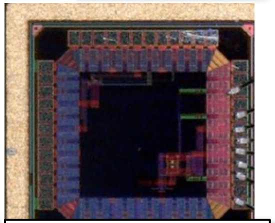
DPTS (CERN)



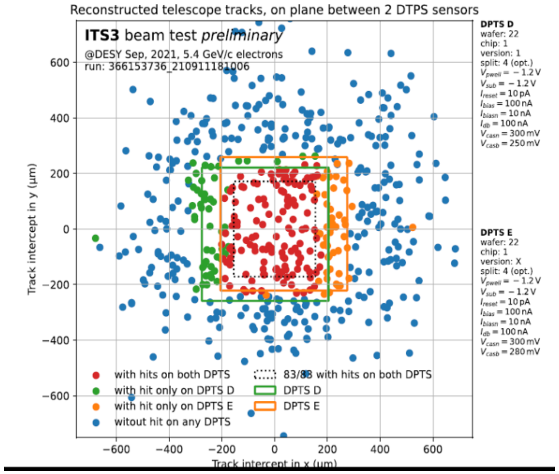
APTS (CERN)



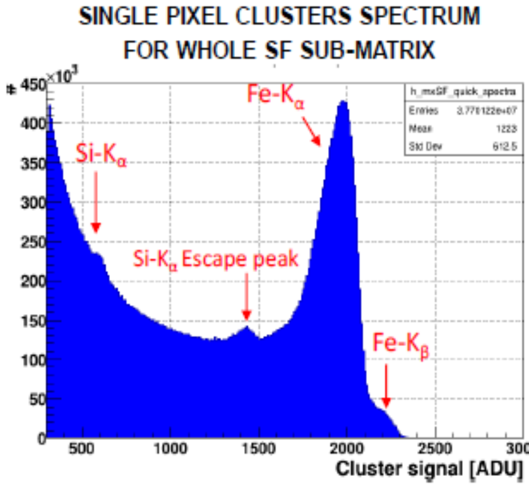
CE-65 (IPHC)



TANGERINE (DESY)

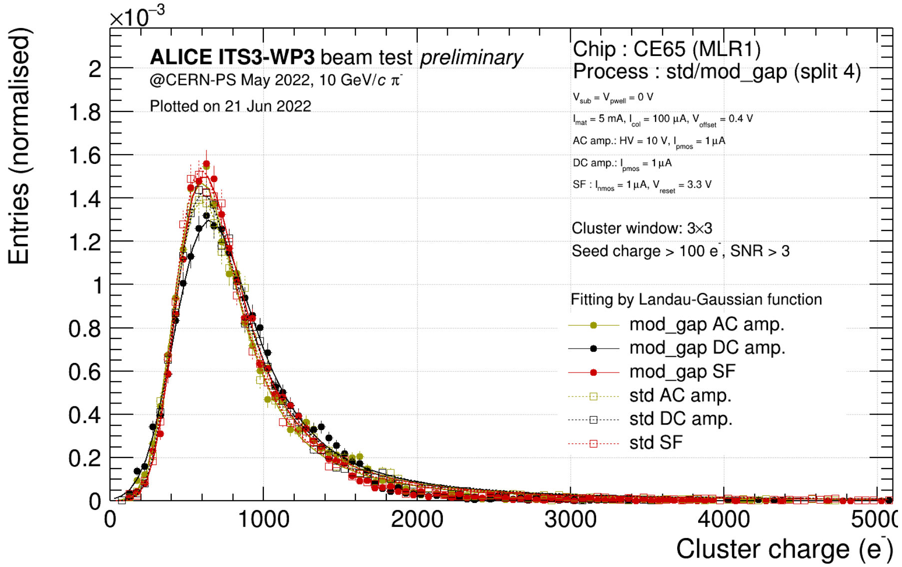


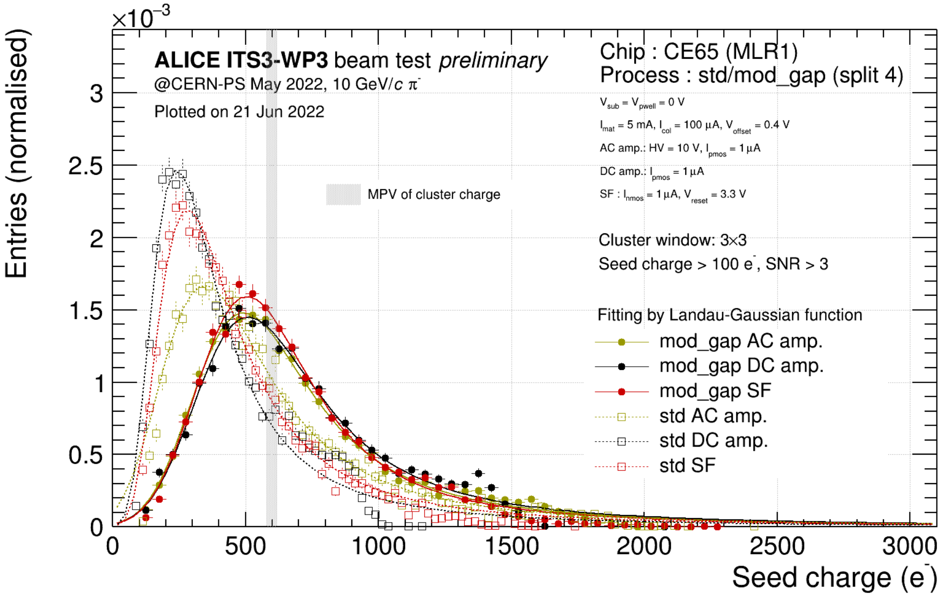
DPTS in test beam



CE_65 with ^{55}Fe

CE65: Process modification reduces charge sharing



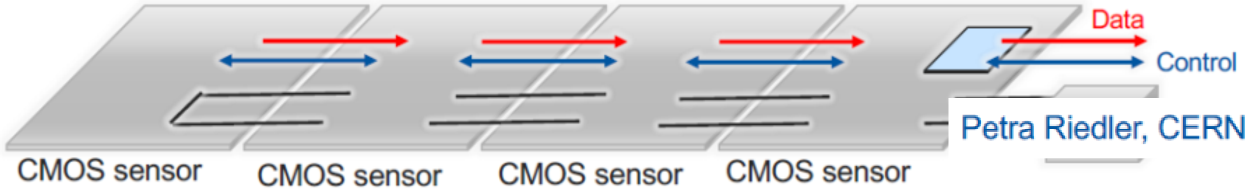


With modified process all the charge is mostly collected by a single pixel

- ✓ Excellent charge collection efficiency
- ✓ Epi variants induce different charge sharing profile -> Resol Optimisation
- ✓ Epitaxial layer thickness estimates match expectations

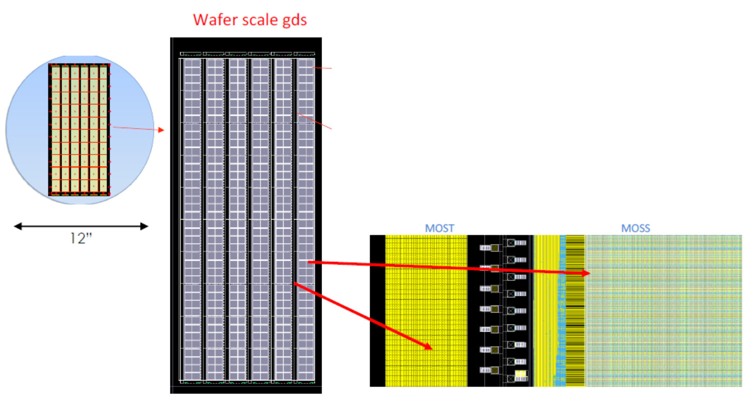
65nm future plans

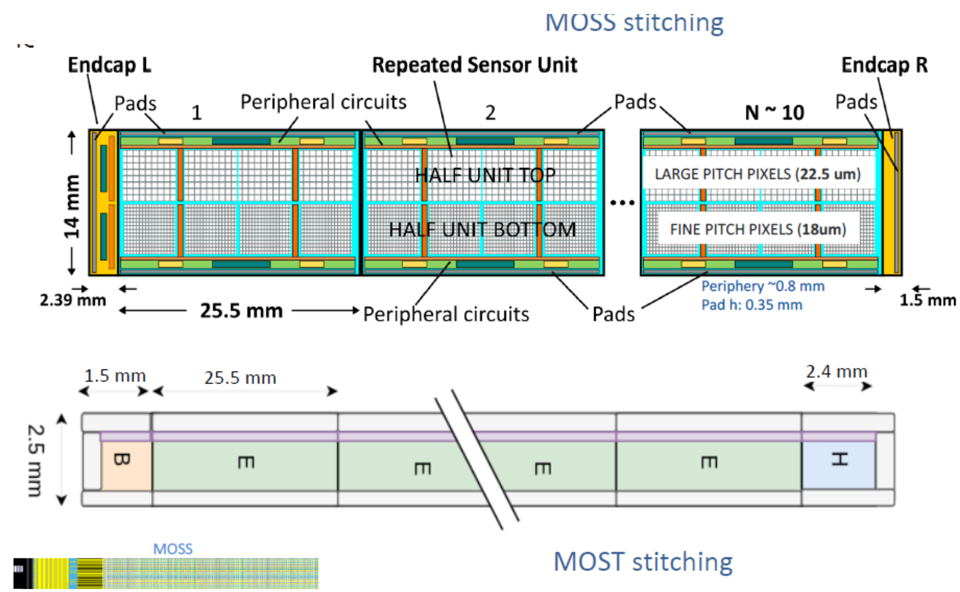
Overcoming the reticle size limitation ⇨ stitching



- Next submission: ER1 (2022)
  - CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades (Submission: Q2 2022)
  - Monolithic Stitched Sensor(MOSS) driven by CERN

✓ Goal: study Stitching and interconnection (wafer scale)
  - Yield, Power distribution, signal routing, Noise, etc.





- Beyond ER1 ⇨ ER2 (2022-23) dedicated to ITS-3

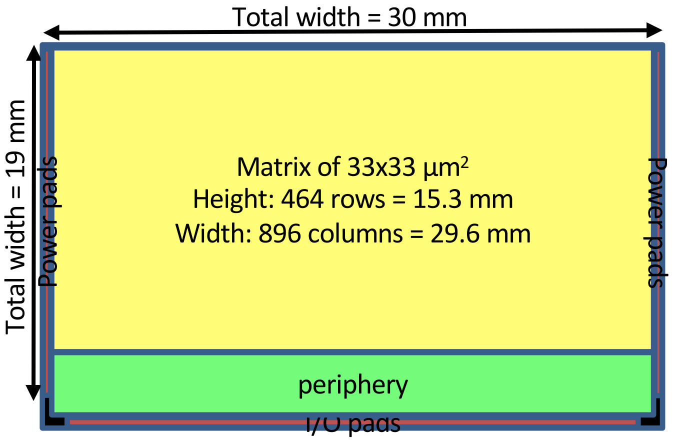
Sensors with timing precision < 1 µs

MIMOSIS-0fast prototype sensor
- Fabricated in mid-2022
- Derived from MIMOSIS architecture with faster front-end
- Explore timing in range 100-500 ns with power dissipation ≪ 100 mW/cm²
- 32x504 pixels (27x30 µm²)

14.8 x 2.0 mm²

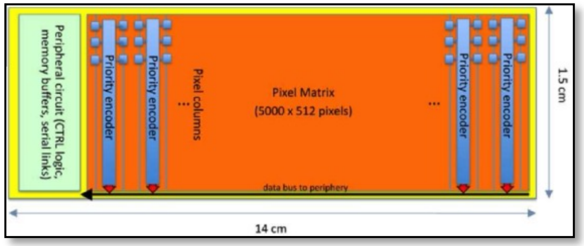
OBELIX sensor Belle II upgraded VXD
- First version submission end of 2022
- Large collab: Bonn, CPPM, HEPHY, INFN, IPHC, Valencia
- Extension of TJ-MONOPIX-2 issued from R&D for ATLAS-ITK

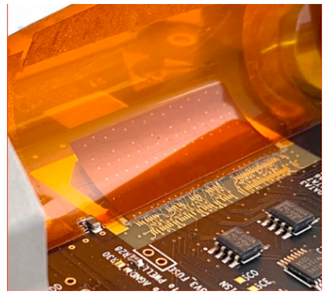
	OBELIX
Pitch	33 to 40 µm
Signal ToT	7 bits
Time stamp	7 bits
Integration time	25 To 100 ns
Bandwidth	< 1 Gbps
Power	< 200 mW/cm²

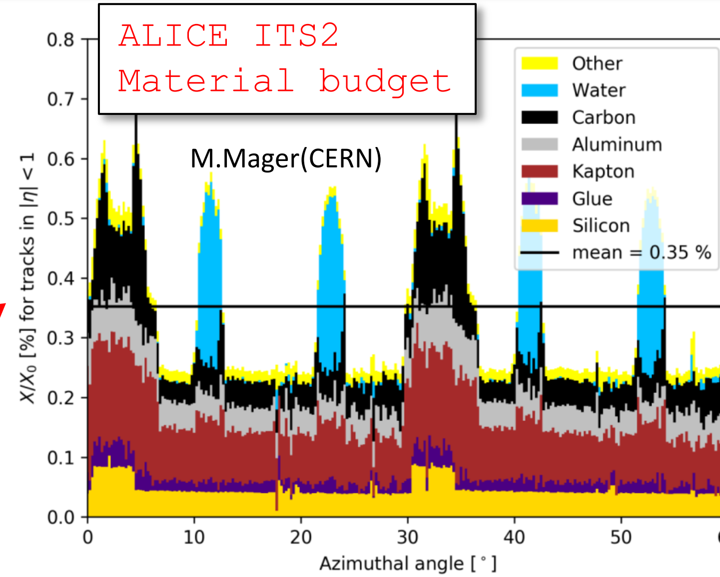


Material budget: Bent sensors & stitching

- Stitching:
  - ✓ The way to go to minimize material budget

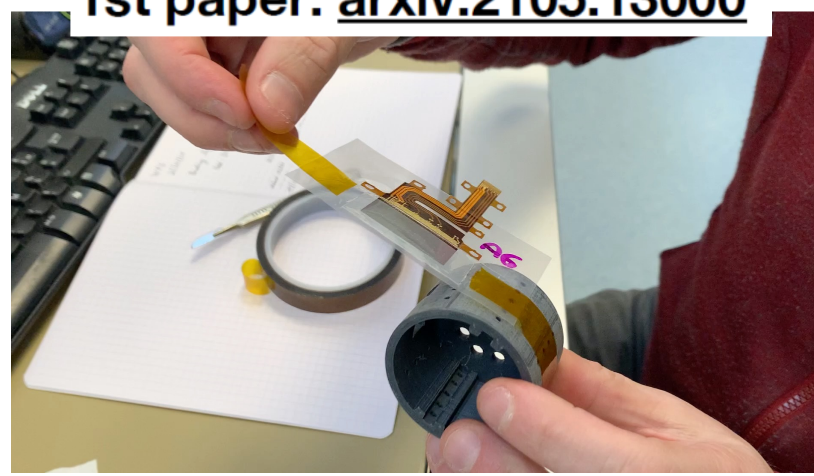


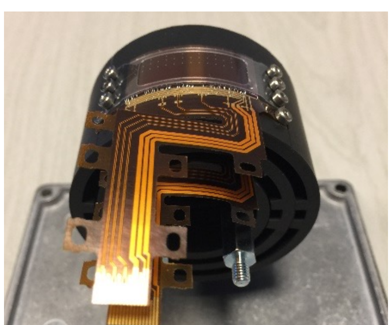


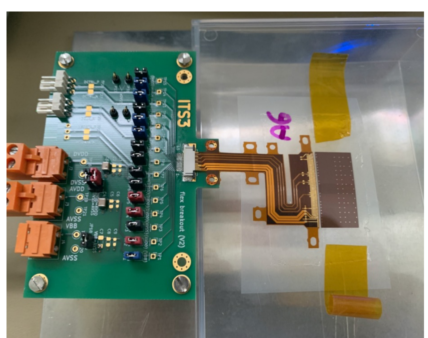


- ALICE-ITS3/CERN drive the R&D
  - ✓ Cf. M. Mager Seminar: *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS sensors*
    - https://indico.cern.ch/event/1071914/
- Micro-technics tests @IPHC
  - ✓ collaboration with ALICE-ITS3
  - ✓ Know-how acquired for bent bonding.

1st paper: arxiv:2105.13000







Bending / bonding
Or Bonding / bending
⇨Functionnal tests

Conclusion & Synergies in CMOS R&D

- Integration ➪ not discussed here!
- CMOS Pixel Sensors are the baseline for Higgs factories
  - ✓ Requirements are within reach
- Strong dynamic of CMOS pixel Sensors R&D:
  - ✓ **180 nm : MIMOSIS series**
    - **(5µm spatial res./ ≤5µs time res./ 60µm thickness / < 70 mW/cm^2)**
    - **MIMOSIS-1 ➪ full size prototype being tested**
    - **MIMOSIS-2 to be submitted (Q3 2022)**
  - ✓ **65 nm technology exploration**
    - First submission dec.2020 (MLR1)
    - **First test beam on CE_65 chips @ CERN/DESY → promising first results**
    - **2nd submission (ER1, Q1 2022): Stitching**
  - ✓ **Stitching** & large surfaces for very low mass detectors ➪ Priority for Higgs factories in the future
    - Bent sensors test beam performed by ALICE
    - Material budget & Large pixelated surfaces
  - ✓ **Synergies** with
    - CERN R&D (ALICE ITS upgrades and EP R&D WP1.2)
    - R&D programs (e.g. AIDA-Innova, EURIZON, etc.)
    - Heavy ion experiments (e.g. ALICE beyond LS3/4 proposal, CBM, EIC)
    - Other experiments: Belle-II, etc.

Thanks for your attention