uTCA fast ADC board for Bunch Arrival Time Monitor signals processing

Stefan Korolczuk, Jarosław Szewiński

Department of Detectors and Nuclear Electronics, National Center for Nuclear Research, A. Soltana 7, 05-400 Otwock-Swierk, Poland,
e-mail: Stefan.Korolczuk@ncbj.gov.pl

Abstract

Many experimental physics projects require high speed and high resolution multichannel analog to digital or digital to analog conversion and powerful enough devices to process acquired data in real time. Typically, this kind of systems are divided into two parts: the analog part with all E-M sensitive devices such as data converters, clock generation and distribution etc., and the digital part with data processing units such as DSPs or FPGAs and all other stuff like power supplies, interconnect with the rest of the system, etc. This second part is similar in many applications. The main effort in construction of the measurement devices is usually matching the ADC analog input circuitry and precision low-jitter clock distribution. Designing the analog part as a separate module, a mezzanine board which can be plugged on the carrier, simplifies the analog part design process.
In many experimental physics applications, the FPGA device is used as data processing unit. to utilize the power of FPGA IO capabilities, the FMC (FPGA Mezzanine Card) has been created. Development of the X-FEL control system brought the uTCA as an officially chosen standard. The combination of these two technologies, the uTCA FMC carrier board, be flexible platform which can be used in many applications in the FLASH and X-FEL accelerators, starting with readout of the Bunch Arrival time Monitor.

FPGA Mezzanine Card

In many experimental physics applications, the FPGA device is used as data processing unit , due to low latency and high performance. Typical processors, such as DSP, has well defined interfaces such as PCI, Rapid IO, Ethernet, etc., the FPGA interface is undefined by default - lots of parallel IO lines can be configured in many ways. Usually, one of the existing standards had to be adopted and implemented in the FPGA to communicate, which created limitations in communication. To utilize the power of large number of interconnect lines, the new standard FMC (FPGA Mezzanine Card) has been established. It does not define the meaning of lines (except data and clock lines), which allows to use maximum flexibility that FPGA offers.
Except the connection, the FMC standard defines the dimensions of the mezzanine boards, and also defines constraints how carrier boards should host these boards. FMC standard has been established by several industrial companies, including the FPGA vendors, in such way, FMC modules may be hosted on different types of boards, such as VME, AMC etc. The uTCA standard chosen by DESY uses the double height AMC boards, which may host 2 FMC sockets for handling one double size FMC module.

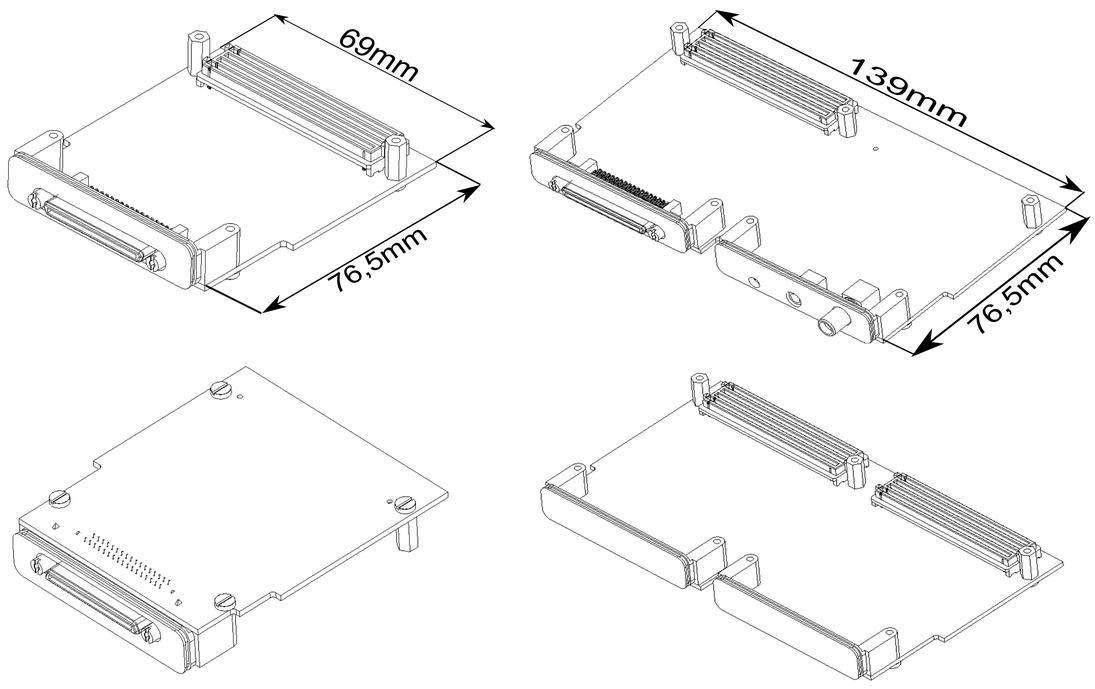

Figure 1: Single and double size FMC Modules

Carrier Board

The main aim of building this board was to provide the platform, which would be able to host 4 (or in minimal approach 2) high-speed ADCs up to 1 GSPS, with reserved 16 lines for each device. Additionally, the design fulfills the following requirements:

- Support for double width FMC
- AMC.4 compatibility with IPMI support
- High performance FPGA on board
- Possible operation as a standalone device (full-featured uTCA crate costs 10k Euro)

Figure 2: PCB outline with main component placement.

Block Diagram

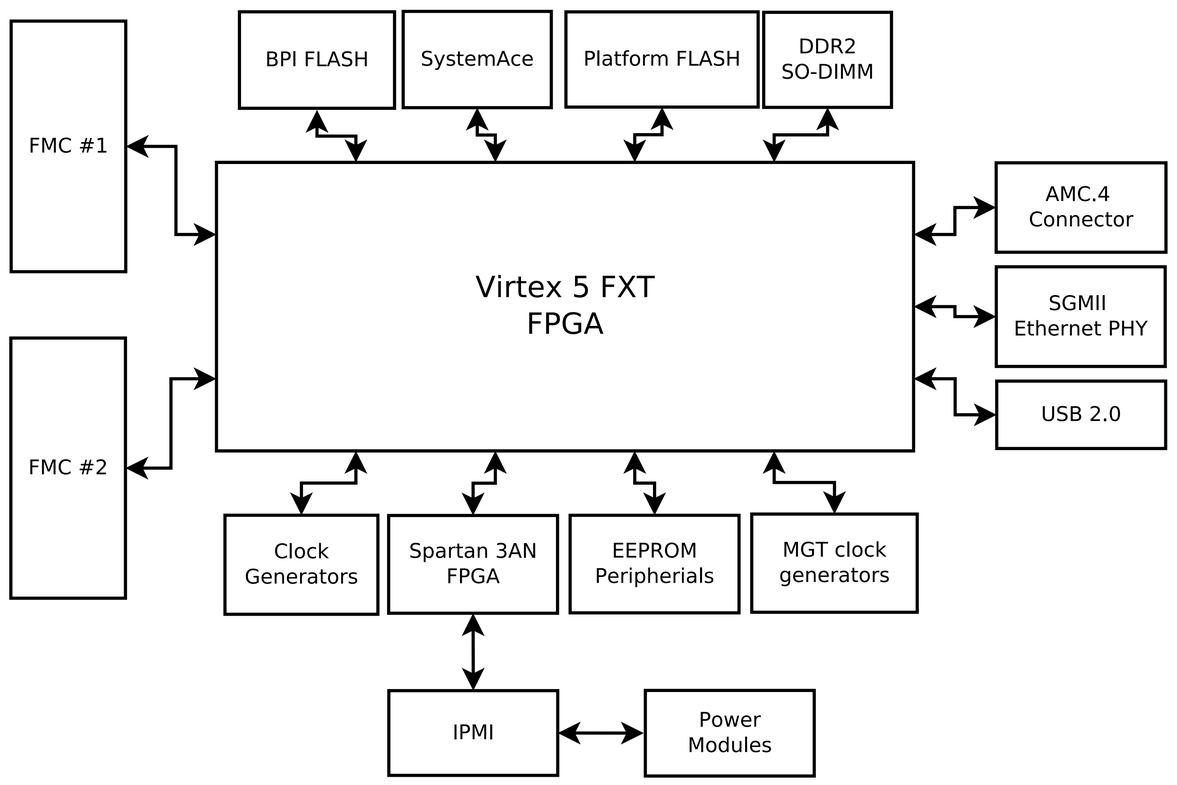

Figure 3: Block diagram of carrier board.

Board Features

- Two single or one double size FMC mezzanine support
- Over 70 differential pairs or 140 single ended signals available for each FMC slot
- Four gigabit serial channels per FMC slot
- Virtex5 FXT70 FPGA with embedded PowerPC440 processor
- DDR2 SO-DIMM connector
- IPMI unit
- Advanced configuration modes with fail-safe configuration memory
- CF card as a configuration memory, and non-volatile storage for embedded systems
- Serial port and JTAG over USB
- Gigabit Ethernet PHY and RJ45 socket for stand-alone operation
- Low noise power supply modules
- Watchdog and configuration supervisor implemented in separate small FPGA
- AMC.4 communication lanes:
  - Gigabit Ethernet
  - PCI Express
  - Two point-2-point links
  - Two M-LVDS links
  - CLKA and CLKB routed to FPGA
  - JTAG

PCB layout

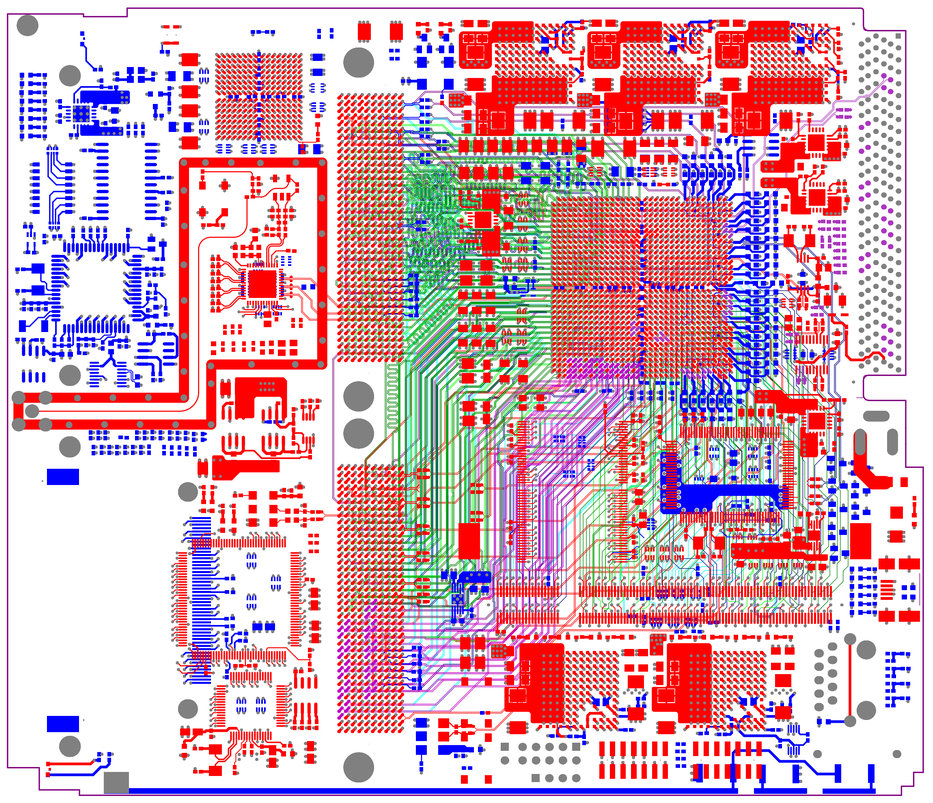

Figure 4: PCB with both FMC sockets and DDR2 SO-DIMM connector routed

References

1. Xilinx web page, http://www.xilinx.com/
2. American National Standard for FPGA Mezzanine Card (FMC) Standard, ANSI/VITA 57.1-2008, VMEbus International Trade Association, http://www.vita.com
3. AMC, uRTM and uTCA Shelf for Physics, PICMG Specification MTCA.4, PCI Industrial Computer Manufacturers Group, http://www.picmg.com/
4. Samer Bou Habib, Eight-channel Fast ADC card for Direct Sampling of GHz Signals, LLRF 2011
5. Jarosław Szewiński, Improvement of Bunch Arrival Time Monitor readout electronics by upgrade to uTCA, LLRF 2011