FPGA architecture for the Spiral2 digital low level RF

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Abstract

The LINAC of the Spiral-2 project is under construction near GANIL existing facilities in Caen (France). [1]

CEA Saclay/DSM/Irfu is in charge of the LLRF for the control of this LINAC.
For this project, a VME64x architecture was chosen, around the Irfu-developed VmeVtx5 main VME board responsible for hardware configuration, (I,Q) feedback and other digital signal processing.

At the core of the VmeVtx5 board, a Xilinx - Virtex 5 FPGA will implement all these functionalities.
The poster presents the FPGA architecture designed for smooth development of VHDL, C language and inter-connections.

Hardware description

For each superconducting cavity, the main LLRF functionalities are grouped in two VME64X electronic boards named VmeVtx5 (front board) and Sp2RF (rear-IO board) :

- VmeVtx5 is build around a powerful Virtex-5 - XC5VSX50T (Xilinx) FPGA to perform digitally the LLRF operations.
- Sp2RF is dedicated to the analog processing of the RF and low frequency signals : analog to digital and digital to analog conversions, amplification, filtering, (I,Q) modulation, etc.
- The VmeVtx5 and Sp2RF modules work with the VME CPU for the upper level Control/Command via Ethernet.

The FPGA design is split in two parts :

- A RF part including fast digital processing (DSP functions)
- A slow processing part (embedded system, VME interface, etc.)

Tools

The development tool is ISE development suite 12.4 Embedded edition. It includes ISE for VHDL development and EDK for embedded development.

These tools allows 2 independent developments :

- VHDL modules are designed with ISE and are checked using ModelSim (orange and pink areas in the figure 3)
- The C application is designed with EDK to be run in the embedded system based on MicroBlaze soft-core processor and PLB bus (green area in the figure 3).

To complete the design, the C application is merged into ISE development.

The LINAC is equipped with five types of bunching or accelerating cavities, including a RFQ, normal conducting rebunchers and superconducting resonators.

There are five LLRF cabinets to pilot cavities connected to the LINAC slow control. [2]

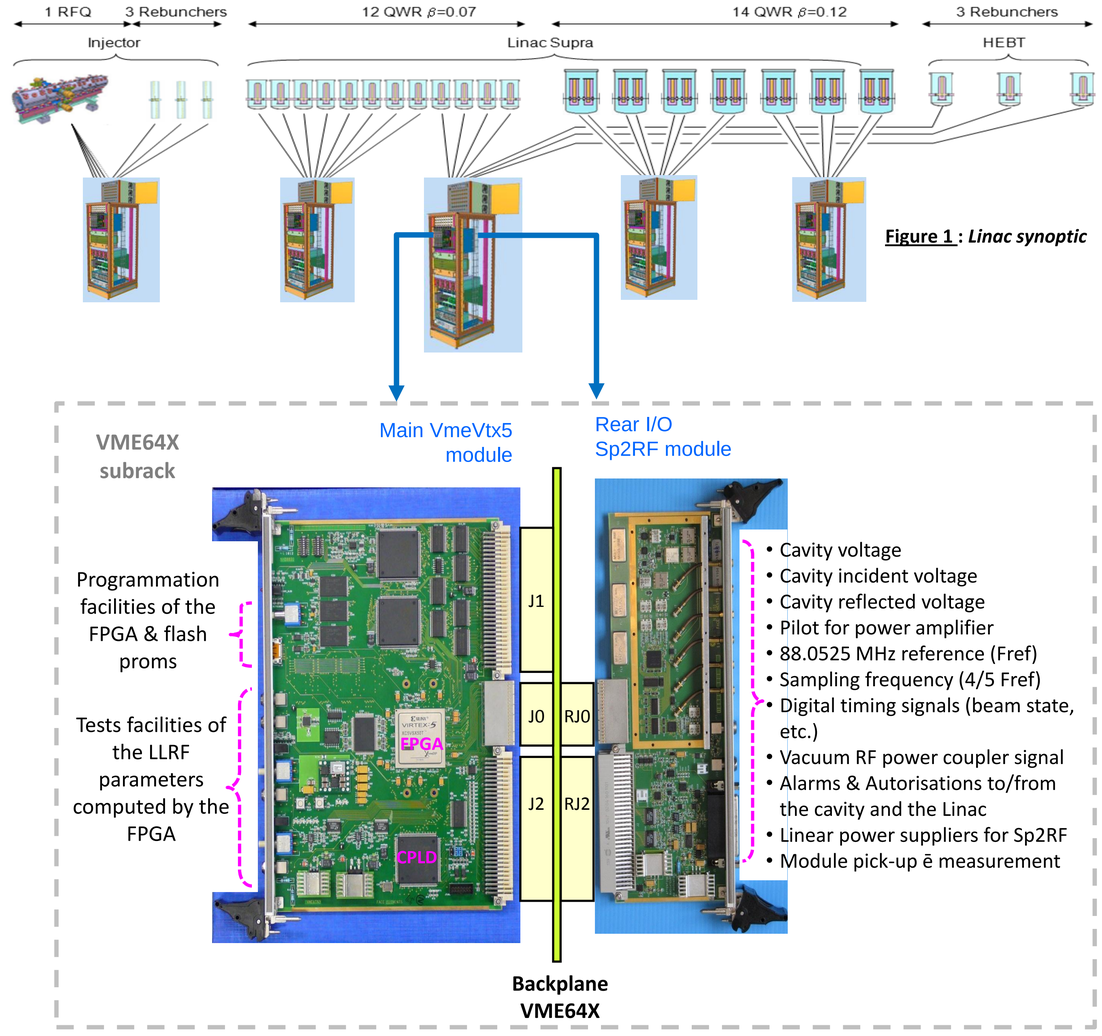

Figure 1 : *Linac synoptic*

Figure 2 : *Set of two VME64X modules grouping the core of the digital LLRF for one superconducting cavity*

Functionalities included in the ISE development

- RF feedback
- Cavity conditioning
- Cavity detuning measurements
- Pulsed mode management for the RFQ
- Incident and reflected RF voltage supervising
- RF perturbations generator
- RF acquisitions chanels calibration management
- Data acquisition into circular buffer for data storage with decimation capability
- Digital and analog test chanels management
- VME communication

Functionalities included in the EDK development

- RF power coupler security hardware supervising
- Frequency feedback for the RFQ power up
- Analog test chanels management
- Bootloader
- Configuration file management
- Distant FPGA and software update
- Tests and maintenance functionalities
- Temperatures, specific voltages supervising
- Xilinx flash access with internal Jtag (custom IP)

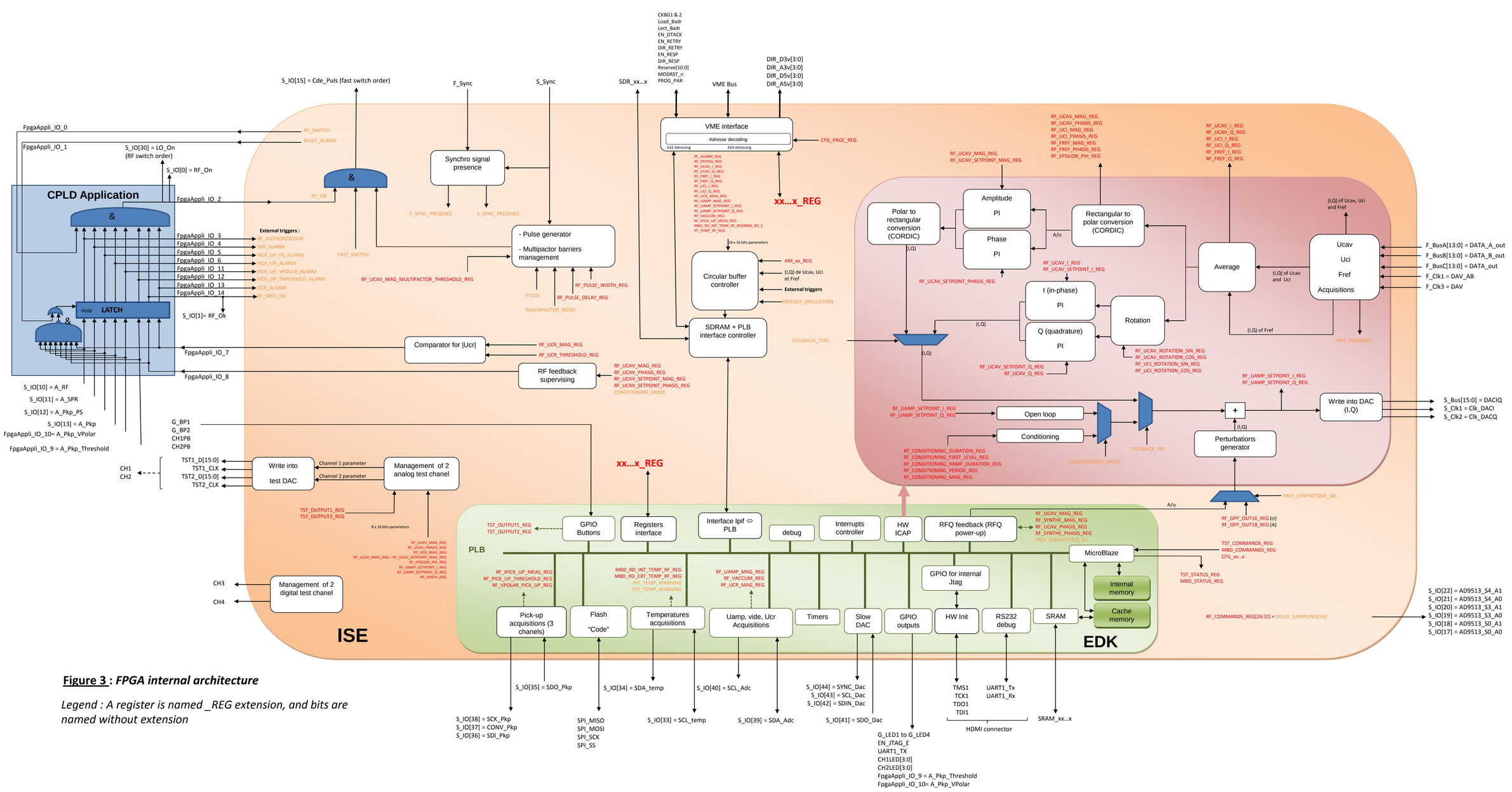

Figure 3 : *FPGA internal architecture*

Legend : A register is named _REG extension, and bits are named without extension

Synoptic (figure 3) : Main module features

- Communication between the embedded system (green area), ISE VHDL modules (orange and pink area), and the CPU Control/Command are performed with **32-bits registers** accesses. A custom tool generates the same 32-bits register database for each software environment.
- **RF functionalities and digital control loop** (pink area) : To measure the cavity signals, I and Q are acquired by direct sampling. Amplitude and phase are computed from (I,Q) data and the CORDIC algorithm. Gains and integrator time constants of PI modules are tuned to stabilize the two feedback loops.

  RF module has its own clock domain provided by the rear-IO Sp2RF board. Thus data transfer between slow processing and RF part are done by means of FIFO memories to solve metastability issues.

  Main RF hardware functions implemented in VHDL are :

  - (I,Q) demodulation by direct sampling
  - Mechanism to manage multipactor barriers during cavity conditioning
  - Hardware implementation of CORDIC algorithm in VHDL
  - CIC filters to average data
  - Two possible feedback controls : (I,Q) or amplitude/phase

- A RF_SPEC_OK signal is generated by the RF **feedback supervising module**. This signal indicates that feedback is working within specifications.
- The RF part (pink area) is located in a specific area inside the FPGA. The design allows to use a partial bitstream for this module and to do a remote dynamic reconfiguration using **ICAP** driven by MicroBlaze. An **internal Jtag module** is intended to update full and partial bitstream in Xilinx flash PROM.
- The **CPLD Application** is dedicated to the security, It ensures safety operations and switches off the RF power inside cavity in case of alarm. Authorizations and alarms come from external side or are locally generated by the FPGA.
- The **SDRAM controller** has been developped with 2 bi-directional ports (PLB bus and VME interface) and a third uni-directional port used for the data storage.

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References

[1] Robin Ferdinand, Patrick Bertrand : Status and challenges of the SPIRAL 2 facility, *LINAC 2010, Tsukuba, Japan*
[2] P. De Antoni, P. Galdemard. The architecture of the low level RF electronics for Spiral 2, Low Level Radio Frequency Workshop, October 2007, *Knoxville, TN, USA*