

Embedded diagnostics in the LEIR and PSB digital LLRF systems A. Butterworth, M.E. Angoletta CERN, Geneva, Switzerland



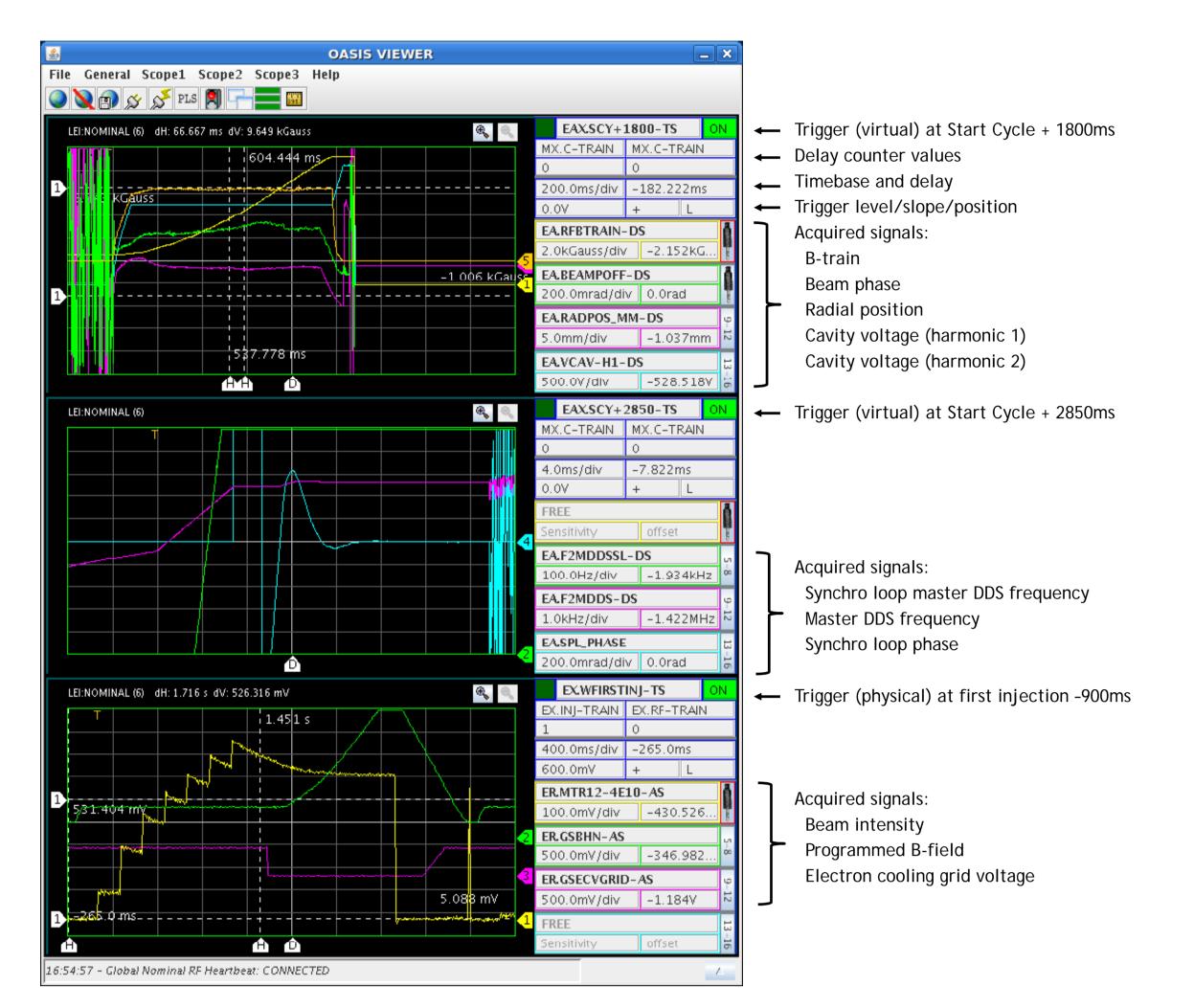
Abstract

The digital Low-Level RF systems deployed in LEIR (Low Energy Ion Ring) and the PS Booster incorporate embedded acquisition buffers for internal signals which are needed by RF specialists and control room operators for setting up and for accelerator operation. These digital signals are integrated into the Open Analogue Signal Information System (OASIS), the distributed global infrastructure used in the CERN injector complex for analogue signal acquisition and visualization. To achieve this, the necessary software interfaces were implemented on top of the digital LLRF system, enabling OASIS to be used to visualize the virtual digital signals in the standard way alongside real analogue signals from other systems. We describe here the implementation of this software in LEIR and the enhancements foreseen for the future PS Booster digital LLRF upgrade.

Introduction

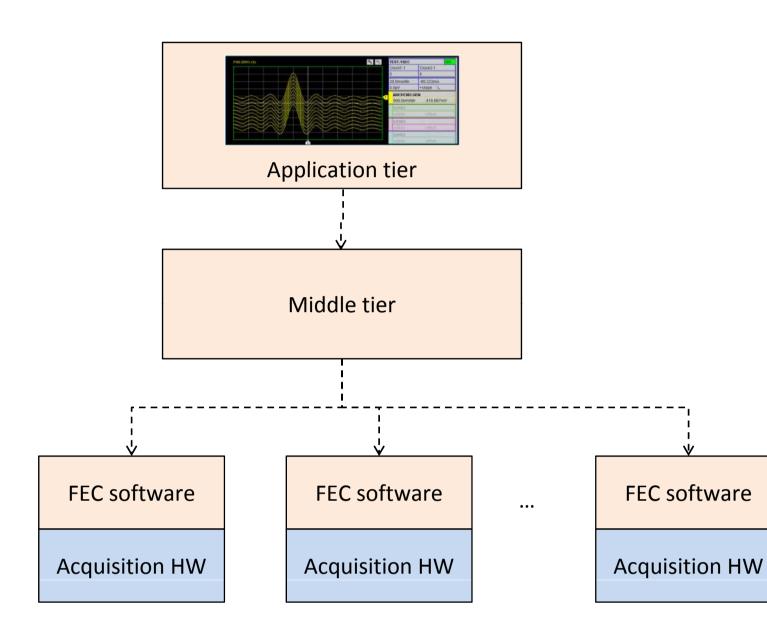
Results in LEIR

The finished system allows us to acquire and display signals from our digital channels (suffix -DS in the figure) in the same way as the standard analogue channels (suffix -AS).



OASIS [1] is an application software used throughout the CERN injector complex for acquisition and display of analogue signals. It allows signal acquisition channels in different remote parts of the accelerator to be configured and triggered in a synchronized way via the accelerator timing system, and displayed on a virtual oscilloscope interface as if they were channels of a single physical oscilloscope.

OASIS is implemented as a 3-tier Java application:



- Application tier, running on an operator console, implements the user interface:waveform display (virtual scope)
- setup parameters for the acquisition

Middle tier, running on an application server, performs resource allocation:

- manages connection of acquisition channels to application programs
- manages connection of signals to channels

Front-end tier running in the Front End Computers (FECs), handles hardware control:

- channels, scopes, counters
- analog switch matrices for connection of signals and triggers

Most of the acquisition channels available to OASIS are physical high-speed digitizer boards (CompactPCI) connected to real analogue signals.

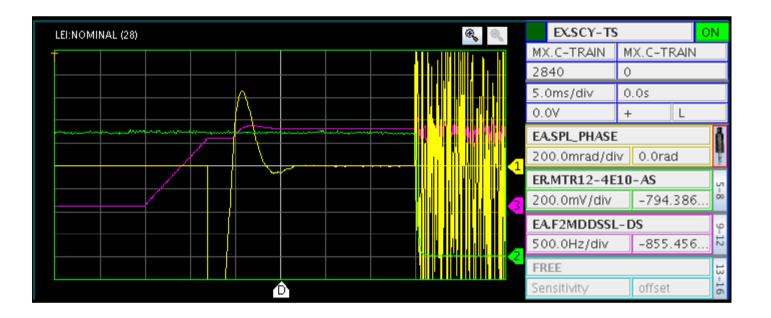
However, one of the requirements of the LEIR digital LLRF project was to be able to acquire a range of internal "virtual" signals within the DSP processing and display them via the OASIS system.

Signal acquisition in the DSP boards

Typical OASIS Viewer window showing signals from the LEIR "NOMINAL" accelerator cycle

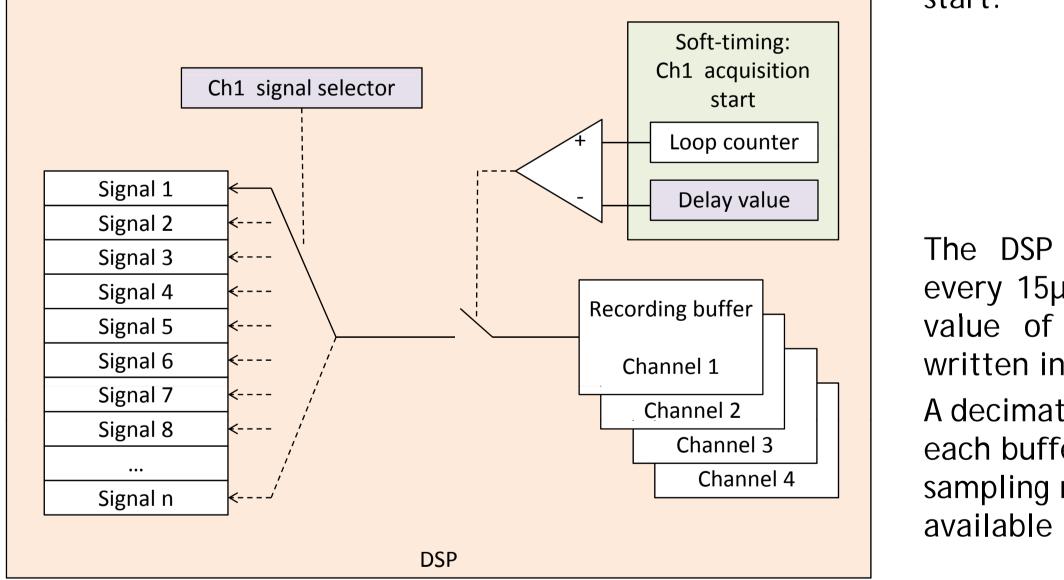
The digital channels are controlled from the user interface in exactly the same way as the analog channels, since the front-end software provides a full emulation of the OASIS interfaces.

It is even possible to display analog and digital signals on the same virtual scope with the same timebase. In order to display signals on the same virtual scope, they must share the same trigger, as in a real oscilloscope. The only hardware trigger currently available for this purpose in the LLRF crate is the Start Cycle timing. A trigger delay may be programmed by means of the counters.



Each of the three DSP boards in the LEIR LLRF system [2] has 4 acquisition memory buffers which can each record up to 1024 data points.

Up to a hundred "virtual signals", from different points in the LLRF processing, are available for connection to each buffer, configurable by setting a selector value in a register which is read by the DSP code.



The start trigger for each buffer is a "soft-timing", implemented as a loop counter in the DSP, and programmed with a count value at which the recording should start.

The DSP executes a code loop every 15µs, and at each loop the value of the selected signal is written into the buffer. A decimation value can be set for each buffer to reduce the sampling rate and increase the available time span.

Front-end software implementation

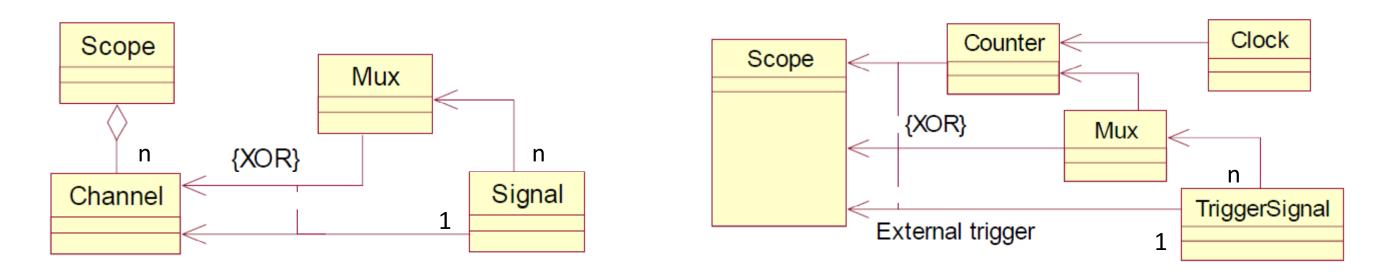
Front-end software was developed under the FESA framework [3], running in the VME FEC, which emulates the ensemble of software interfaces used by the OASIS application to control the hardware:

Analog and digital signals displayed together on the same virtual scope, triggered by the Start Cycle timing (EX.SCY-TS) with a trigger delay of 2840 ms.

Future improvements for the PS Booster

The new digital LLRF system for the PS Booster [4], which is currently under development and due to be installed in 2012 and 2013, will include a similar system of acquisition buffers. A certain number of improvements are foreseen compared with the LEIR system:

- Implementation in FPGA: In the LEIR system the acquisitions are performed by the DSP. In the new PSB system, this functionality will be handled by an FPGA, reducing the load on the DSP and enabling faster loop execution.
- Increased buffer size: The acquisition buffer size will be increased from 1024 to some tens of thousands. This will allow sampling at higher frequency for longer time spans.
- Data reduction options: The larger buffers and faster processing will allow us to provide data reduction modes such as peak detection and averaging.
- More buffers: Each acquisition buffer is in general a non-shareable resource. This has been a limitation in the LEIR system when accelerator operators and equipment experts both want access at the same time. Increasing the number of buffers will allow multiple users to work on the system more comfortably.
- Permanently connected "sampler" buffers: Much of the time, the OASIS buffers are used in the control room to observe signals through the whole accelerator cycle at a low sampling frequency. For this purpose, a small buffer (around 1024 points) will be provided for sampling at a fixed frequency (around 1kHz) of every signal permanently. This will free up the larger buffers which can be connected to a chosen signal on demand.
- Scope: the horizontal functionality (timebase and triggering) of the oscilloscope. We implement the timebase selection by controlling the buffer decimation in the DSP.
- Channel: the vertical functionality (sensitivity and scaling) of a scope channel.
- Mux: the functionality of a signal selection multiplexer (switch matrix). We emulate a switch matrix using the signal selector mechanism In the DSP.
- Signal: a description of an analogue signal [name, scaling, units]
- TriggerSignal: a description of a trigger signal [name, delay]
- Counter: a delay counter capable of counting in milliseconds. We use the TriggerSignal and Counter delays to compute the Delay value for the "acquisition start" soft-timing.



Signal and trigger interfaces exposed by the front-end software (from [1]).

References

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