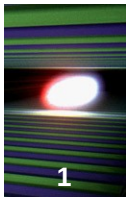
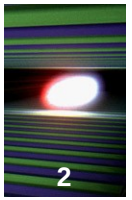


System Architecture and Hardware Development for the LLRF System for EU-XFEL using µTCA.4

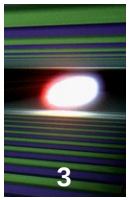
Tomasz Jezynski
for the LLRF - Team

Outline



- Background & PICMG xTCA for Physics Initiative
- LLRF system for EU-XFEL
- xTCA Crate
- Boards Development@DESY & Industry Developments to new Physics Standards
- Summary Conclusions

Background & PICMG xTCA for Physics Initiative



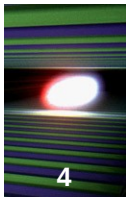
SLAC

ILC Snowmass 2005
Proposed ATCA as model for ILC controls and beamline instrumentation systems (85% uptime is required)
R&D programs at SLAC for I&C, magnet power supply systems, modulators, etc.

DESY

Proposals for ATCA (LLRF) and µTCA (Tunnel Controls) under XFEL

Background & PICMG xTCA for Physics Initiative



- ATCA Workshops: FNAL 2007 and Dresden 2008
- Formation of new PICMG standards collaboration for Physics May 09

Lab members

Founding Members: DESY, FNAL, IHEP, SLAC

Additional Lab Members: IPFN Lisbon, ITER, CERN

Industry Members

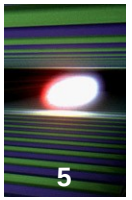
Founding Members: Cypress Point Systems, Performance Technologies, Triple Ring Technologies

Additional Members: ~43 companies total

Working Groups:

- Hardware Committee
- Software Committee

Background & PICMG xTCA for Physics Initiative



MicroTCA™

PICMG® Specification MTCA.4
R 1.0 Draft 0.9xh

MicroTCA Enhancements for Rear I/O and Precision Timing

14 July 2011

For Member Review Only - Do Not Claim Compliance To or Distribute This Draft Specification

PICMG®
Open Modular Computing Specifications

µTCA®

AdvancedTCA®

PICMG® 3.8
Draft RC1.0 for Revision 1.0

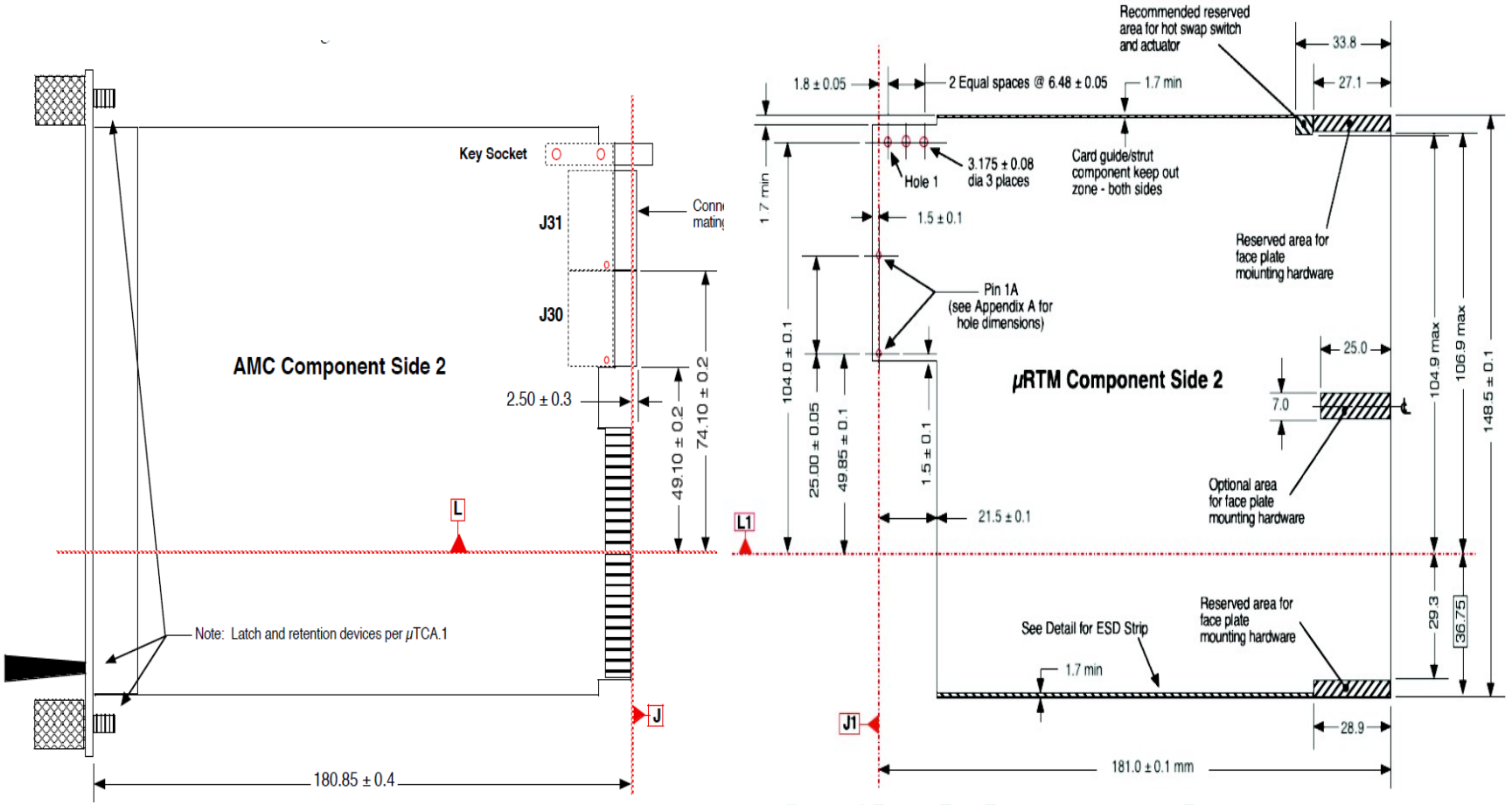
AdvancedTCA Rear Transition Module Zone 3A

For Adoption Ballot only
Do Not Claim Compliance To or Distribute this Draft Specification

26 July 2011

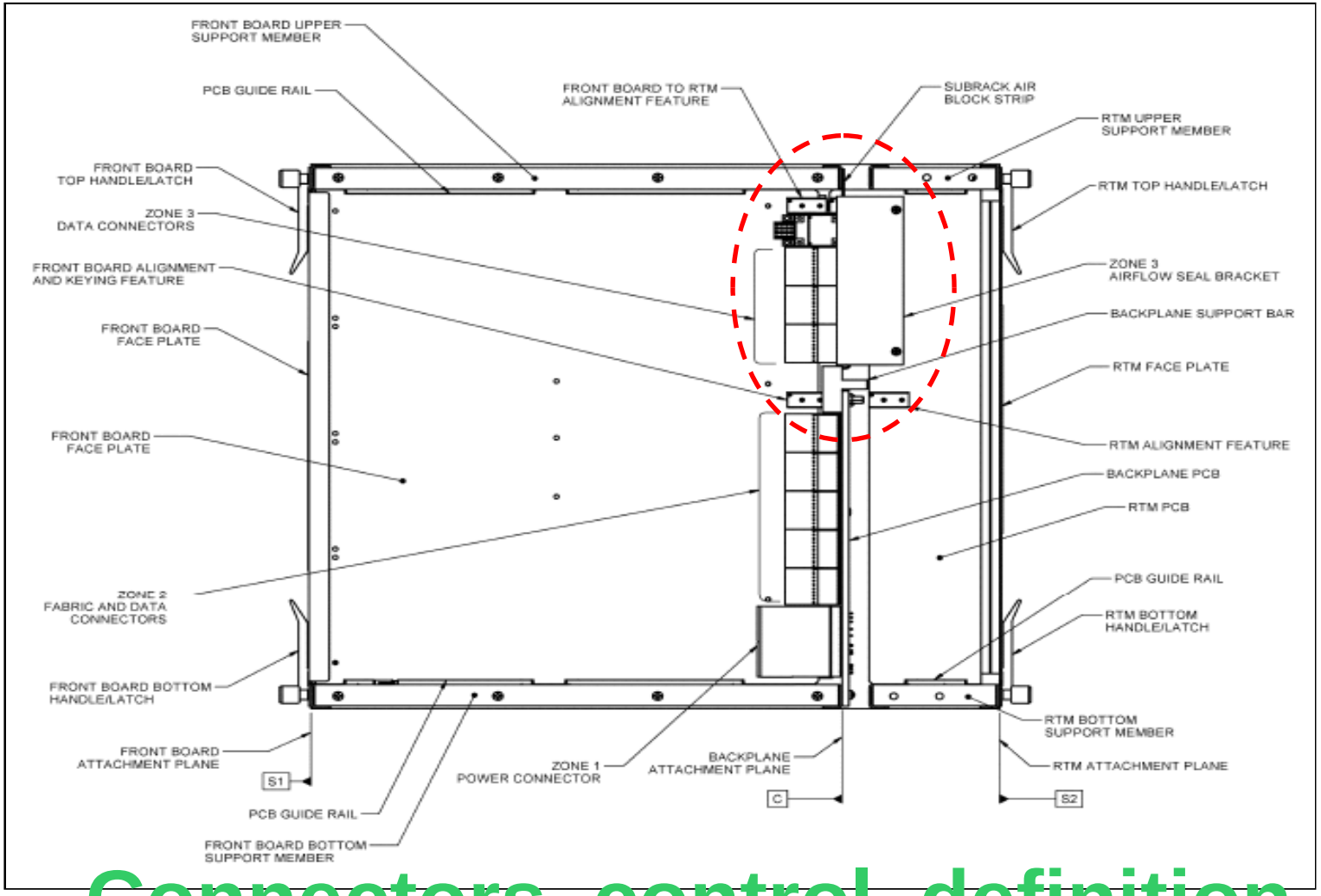
PICMG®
Open Modular Computing Specifications

Background & PICMG xTCA for Physics Initiative



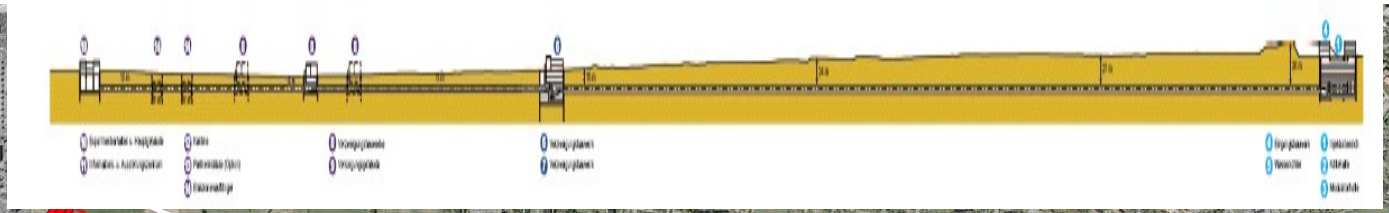
Connectors, control definition, pin assignment

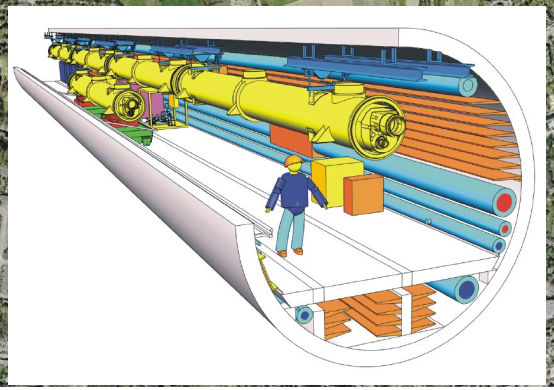
Background & PICMG xTCA for Physics Initiative



Connectors, control definition

LLRF Requirements and Motivation





- ....
- 3.3 km
- ....
- **Modularity**
- **Scalability**
- **COTS modules**

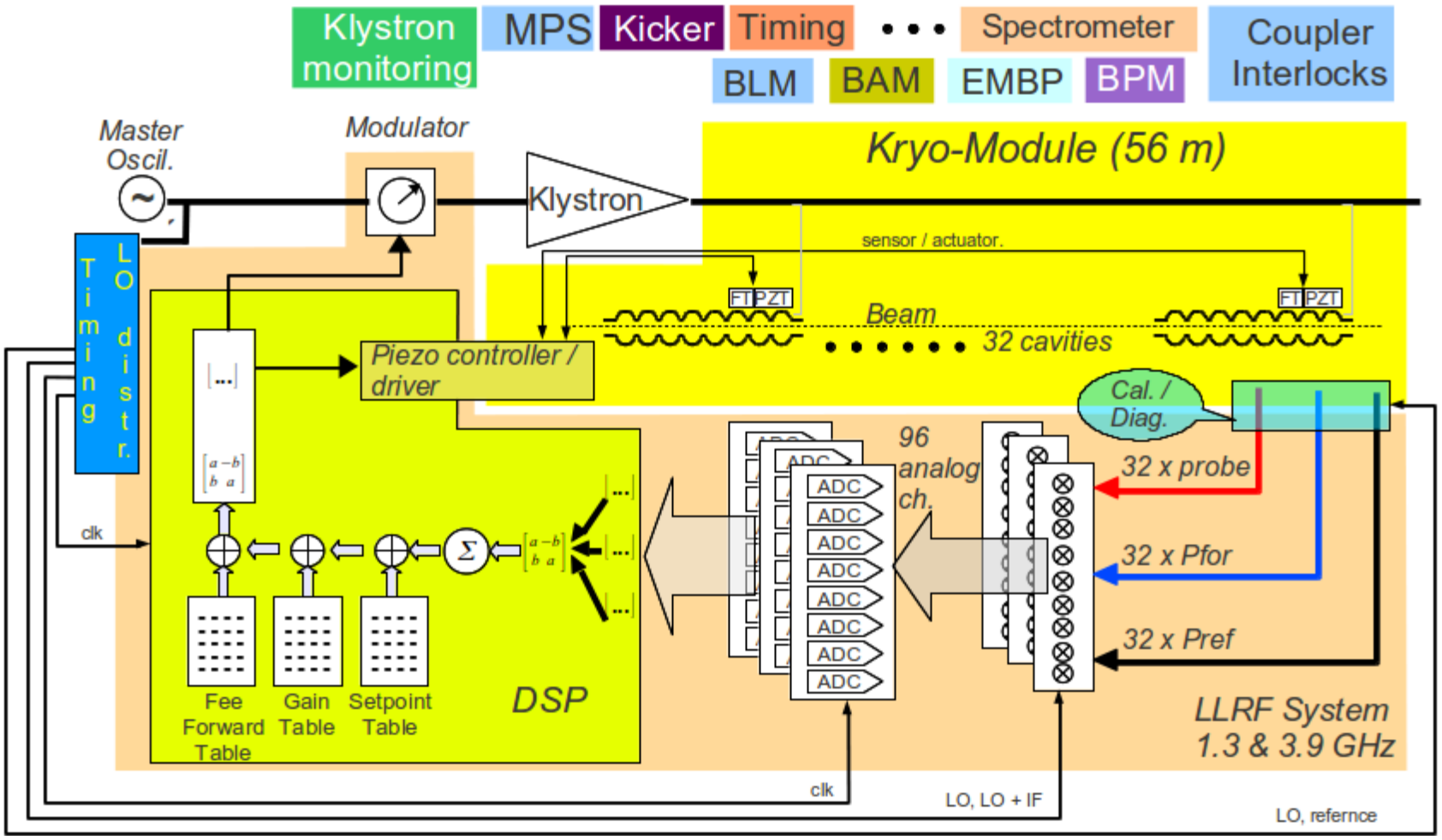
HERA

FLASH

DESY

Hamburg City Centre (7 km)

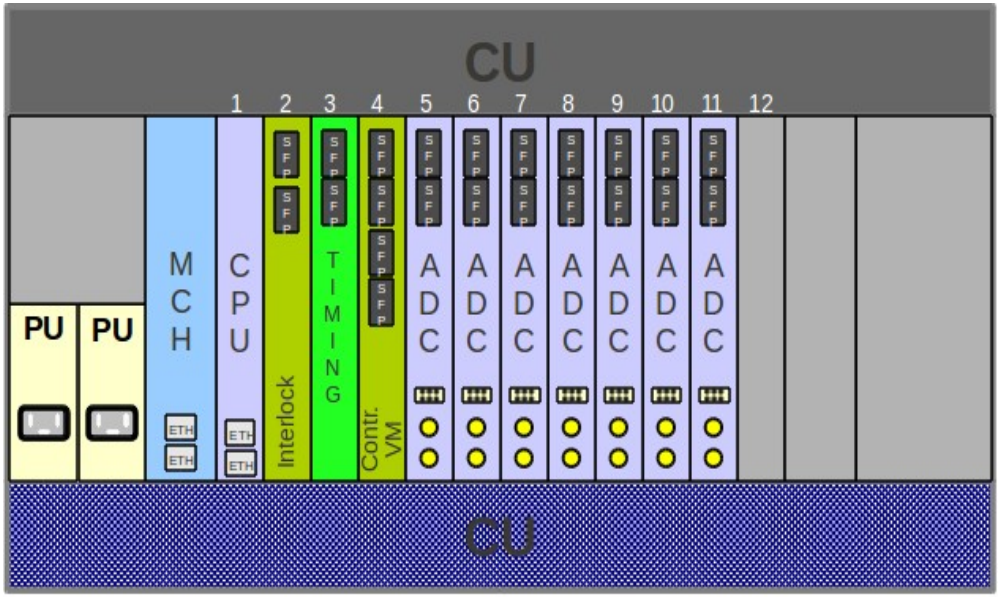
LLRF system for EU-XFEL

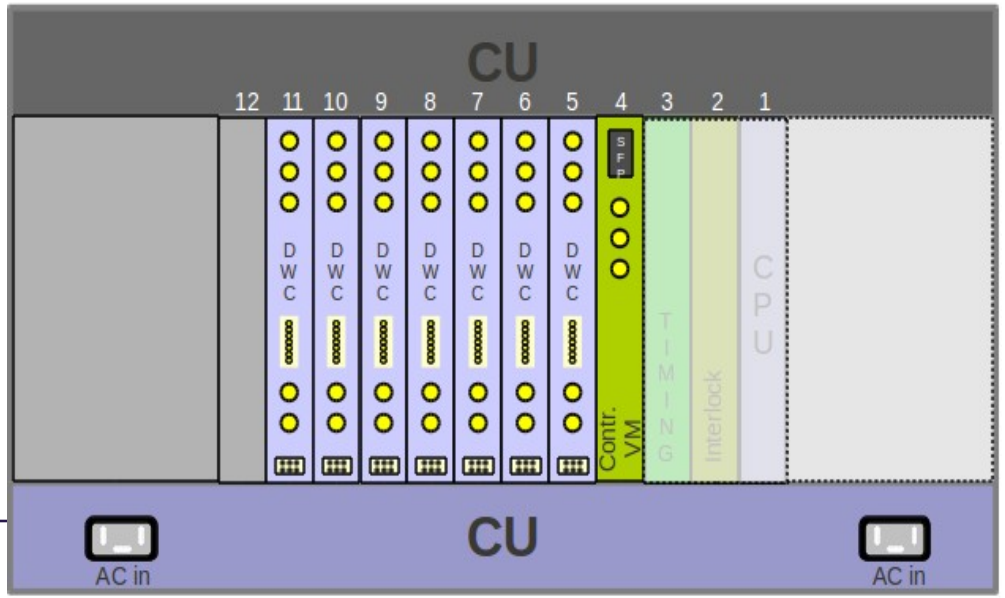


LLRF system for EU-XFEL

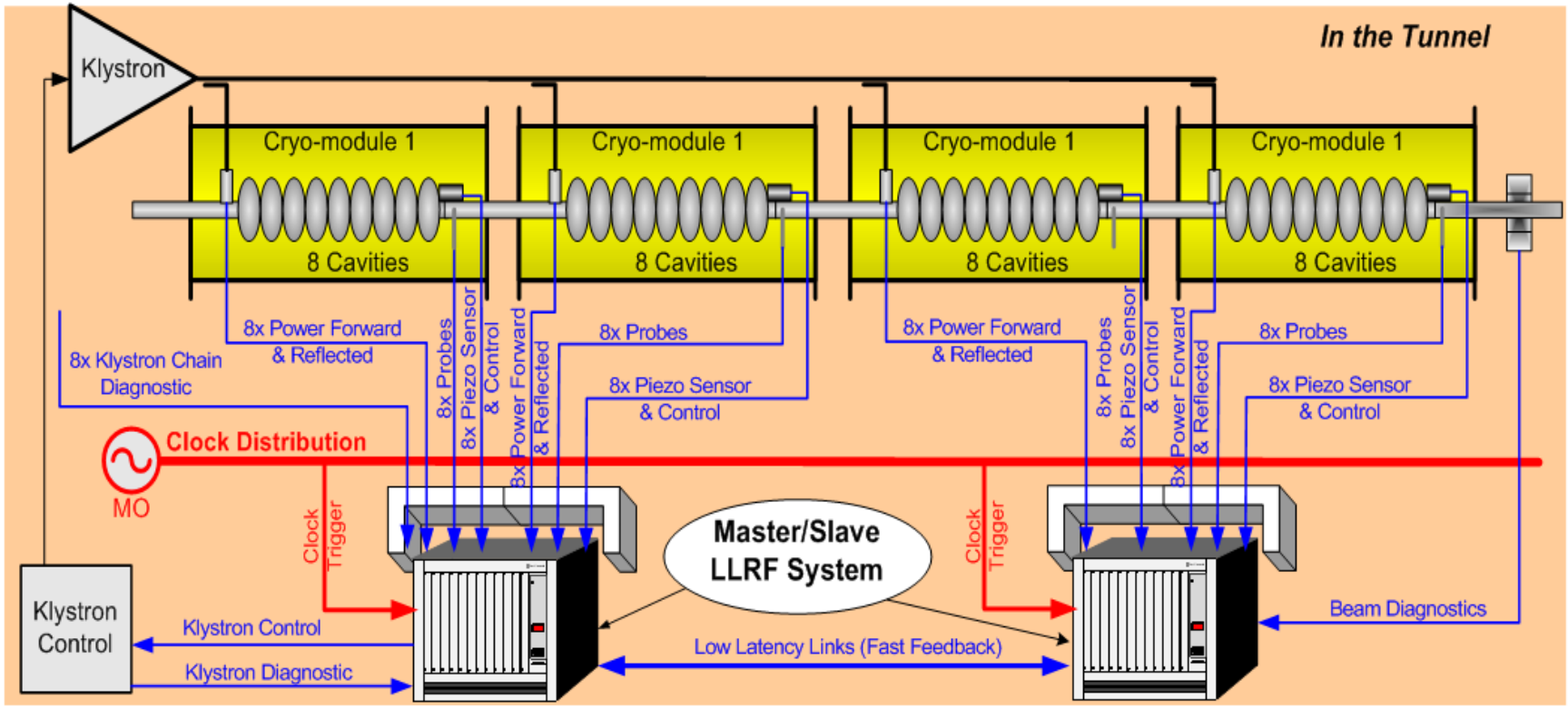
- CRATE
- POWER SUPPLY
- MCH
- CPU (AMC)

- TIMING (AMC)
- DSP (AMC)
- MODULATOR (RTM)
- IQ DETECTORS
  - ADC – AMC
  - Down-converters - RTM
- INTERLOCK (AMC + RTM)



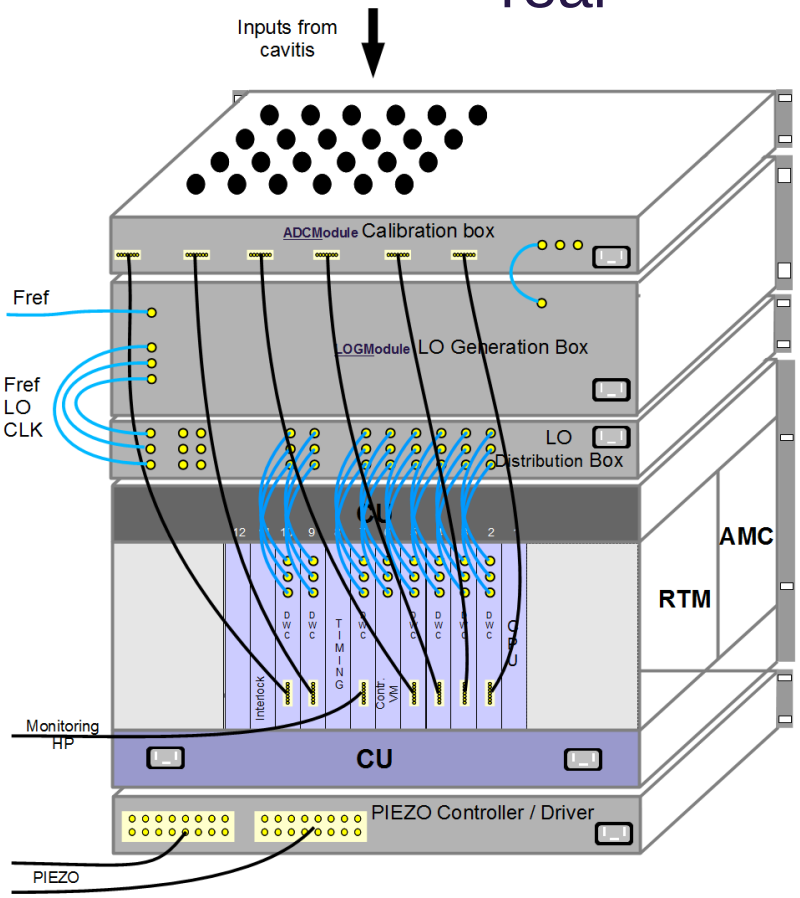


LLRF system for EU-XFEL



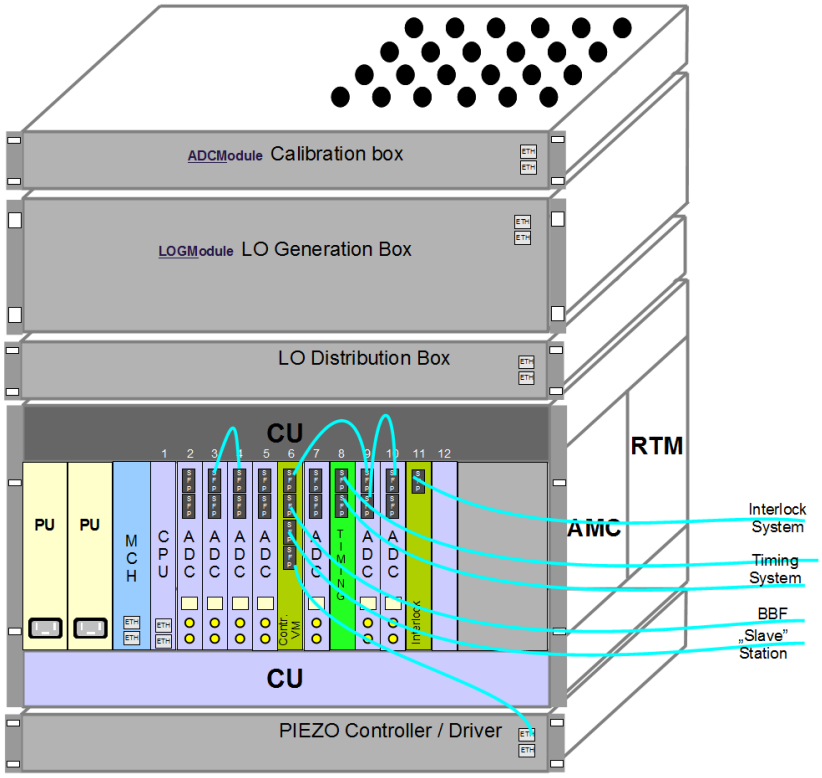
LLRF system for EU-XFEL

rear



1. CPU
2. ADC – Pref
3. ADC – Pref.
4. ADC – Prob
5. ADC – Prob
6. Contrl.+VM
7. ADC – Monitoring
8. Timing
9. ADC – Pfor.
10. ADC – Pfor.
11. Interlock

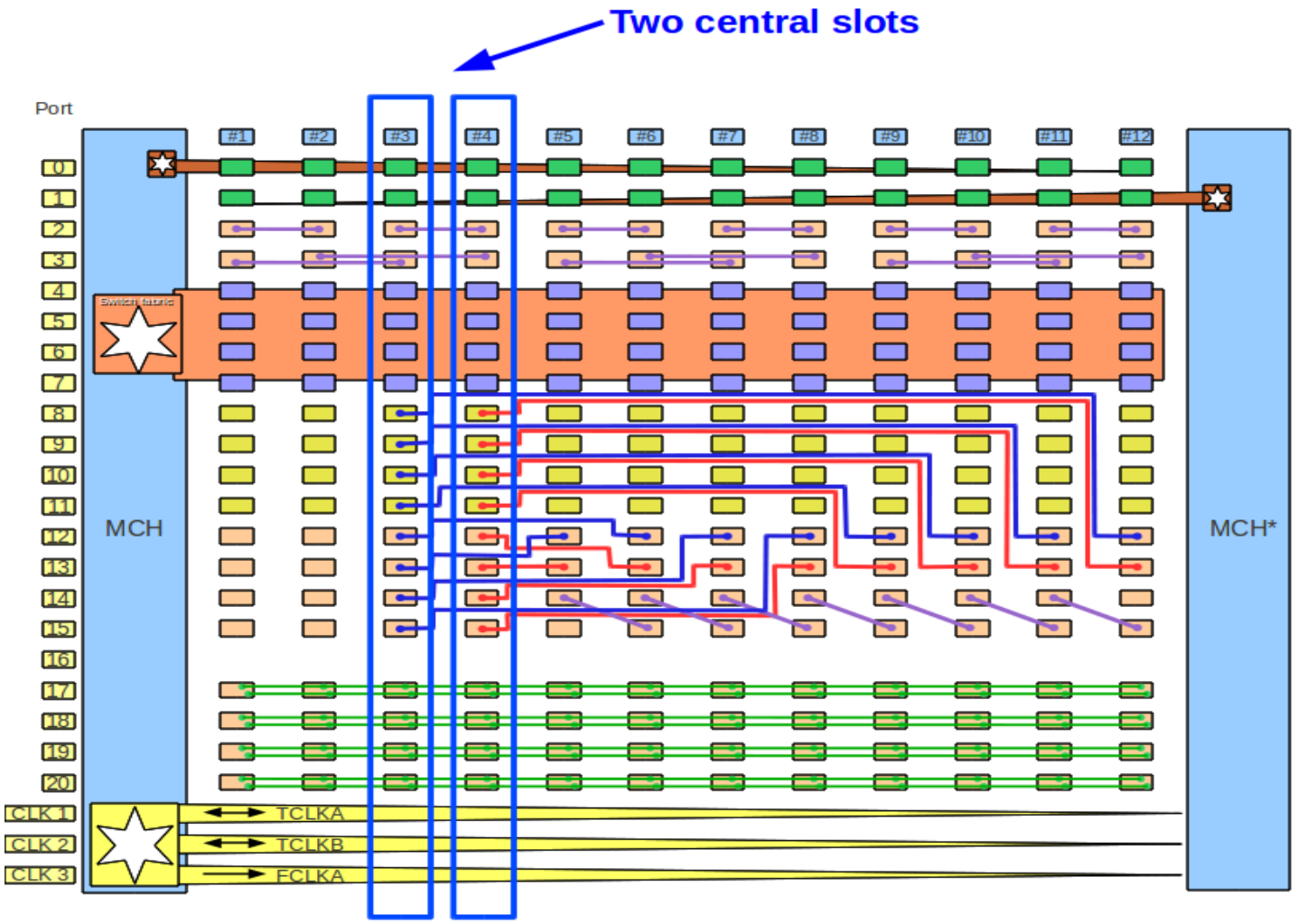
front



Many RF cables for LO distribution

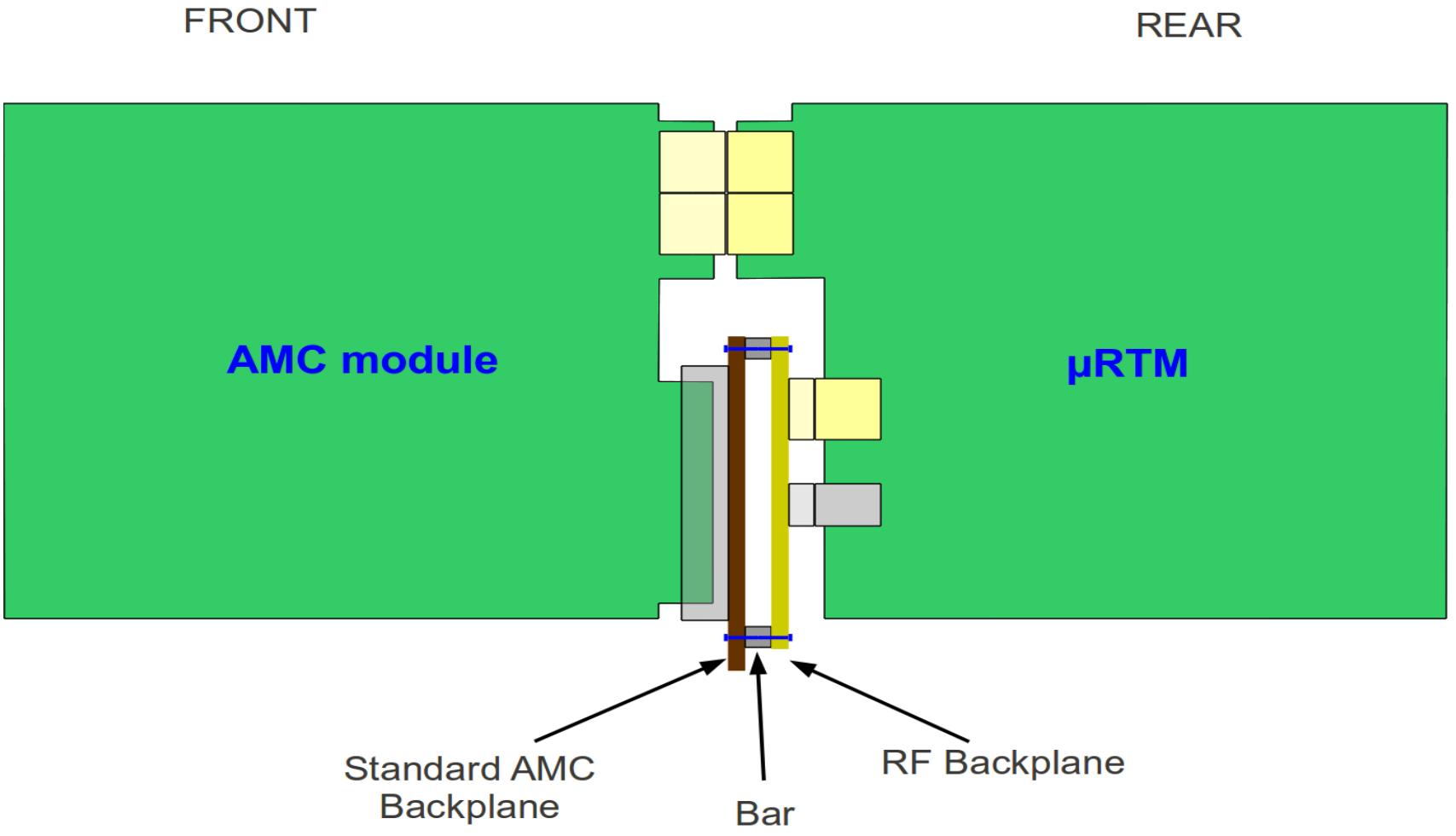
Fibers between boards in the crate

xTCA Crate - LLRF Backplane

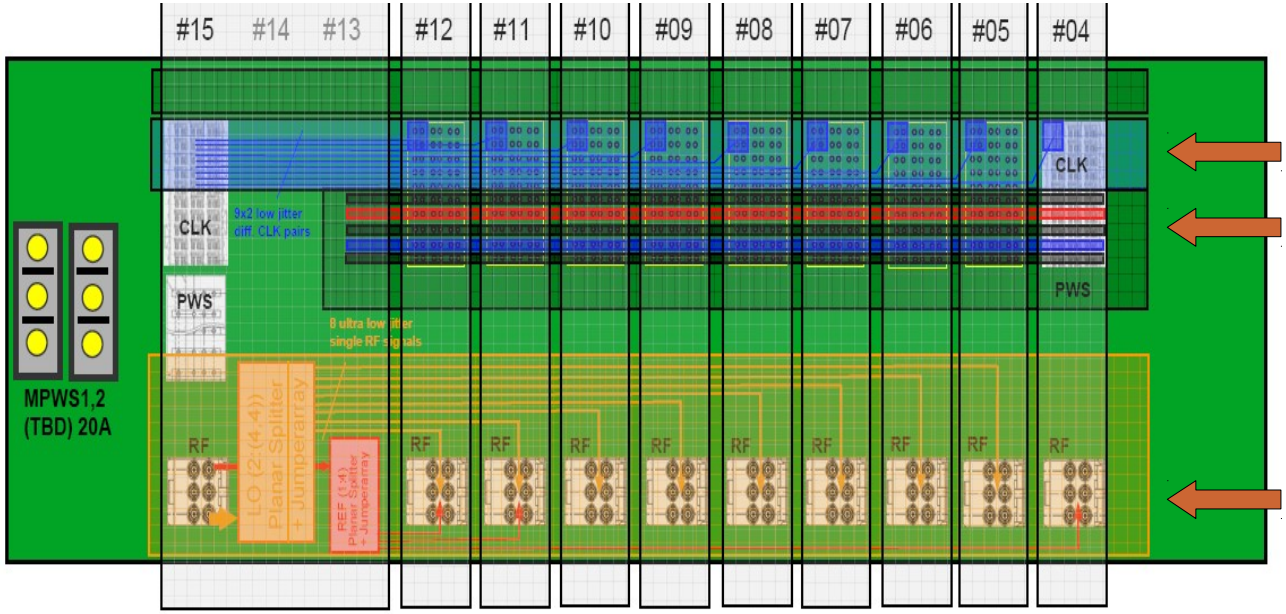


Star configuration : Controller to IQ detectors

xTCA Crate – RF Backplane



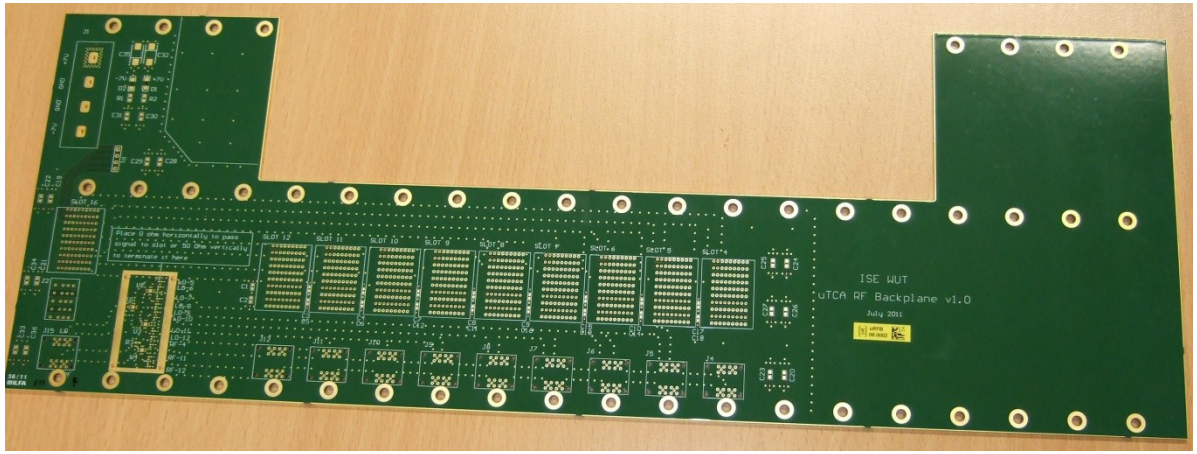
xTCA Crate – RF backplane

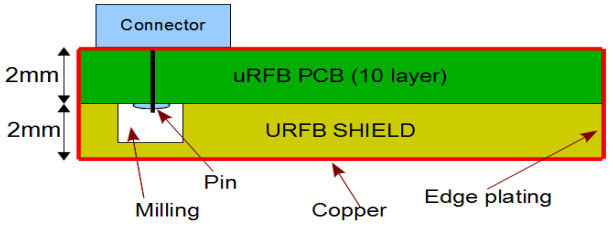


Low jitter clock distribution
< 200fs
(e.g. ADC-Clocks)

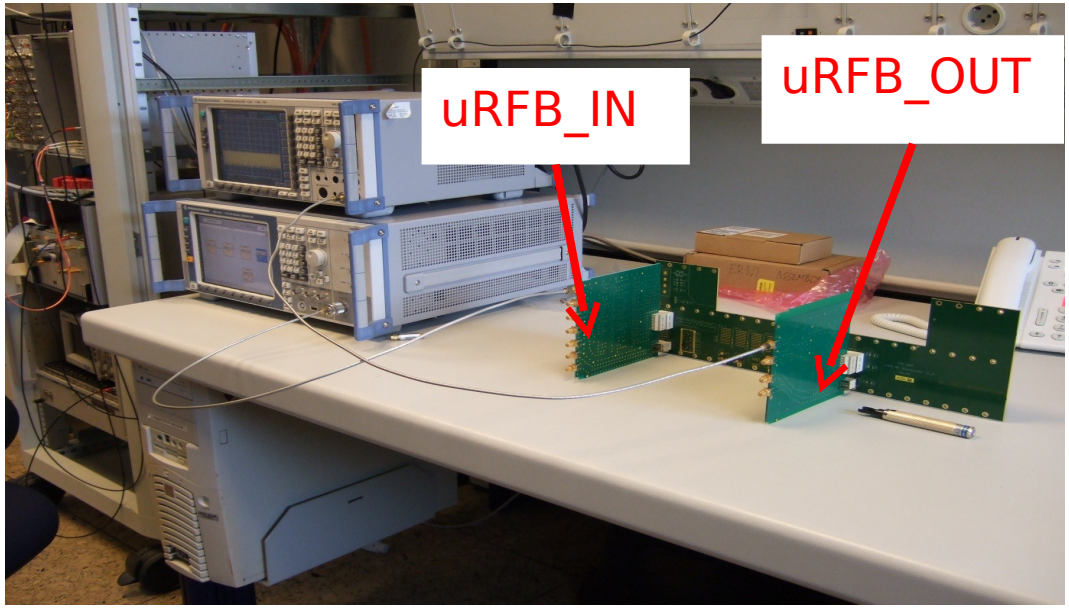
Independent redundant power supplies
(e.g. +15V, -15V)

Low jitter RF-signals
<10fs
(e.g. LO-Distribution)





RF Backplane Test Setup



RF loss (worst case):

- LO distribution, 14 dB (11.1 dB splitter)
- RF distribution, 9.6 dB (7.4 dB splitter)

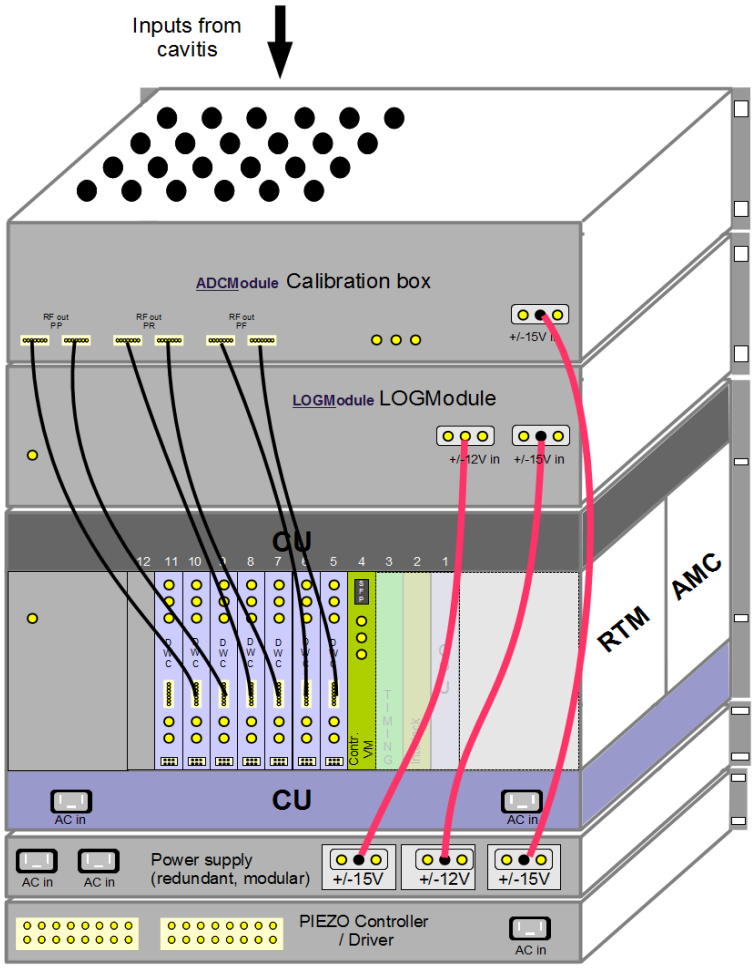
Clock jitter:

- 80-110fs (significant loss in uRFB_IN test board)

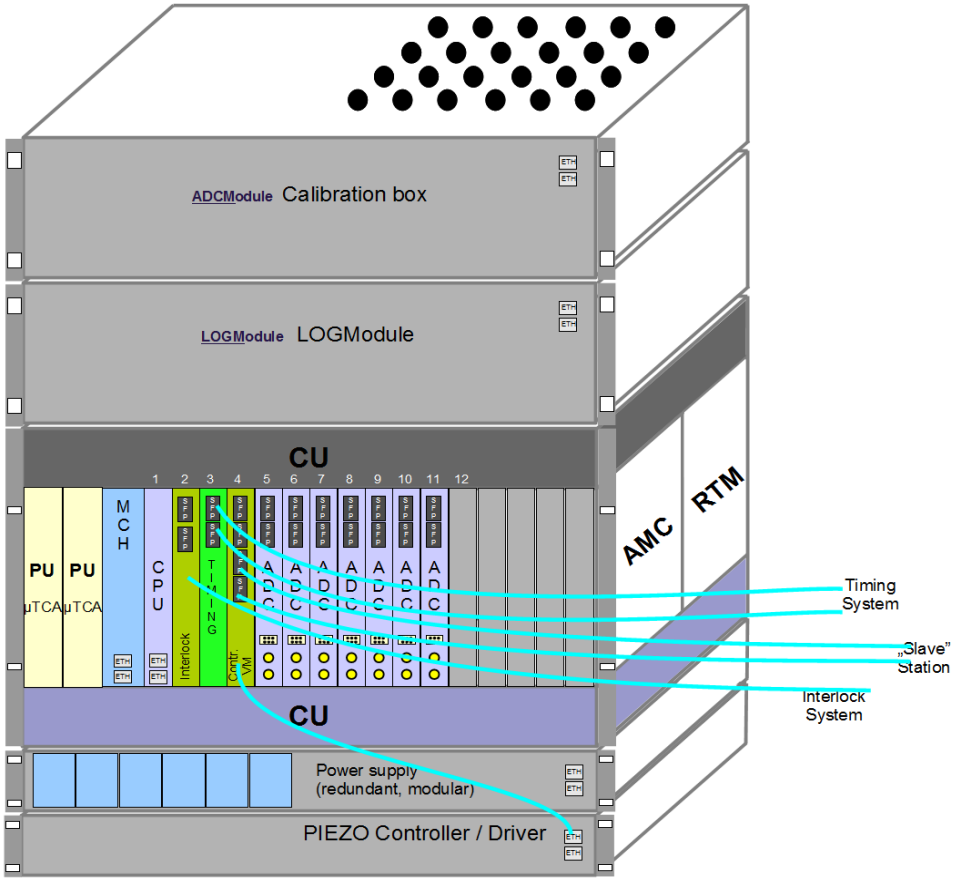
Crosstalks:

- no crosstalk between RF and LO lines were observed on the level of -90 dB (measurement equipment limitation)

LLRF in xTCA Crate



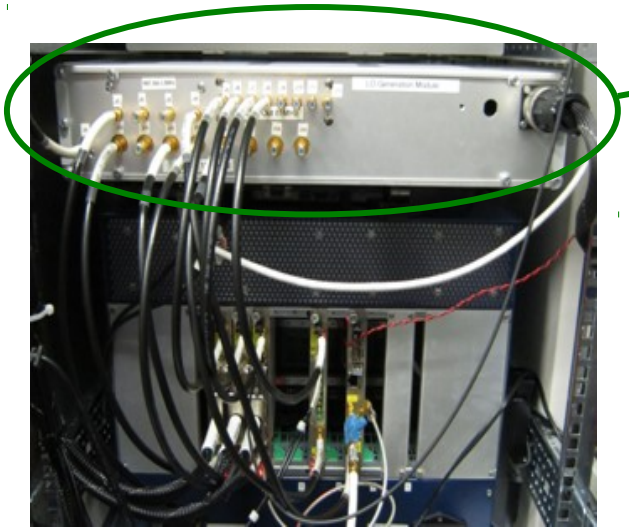
rear

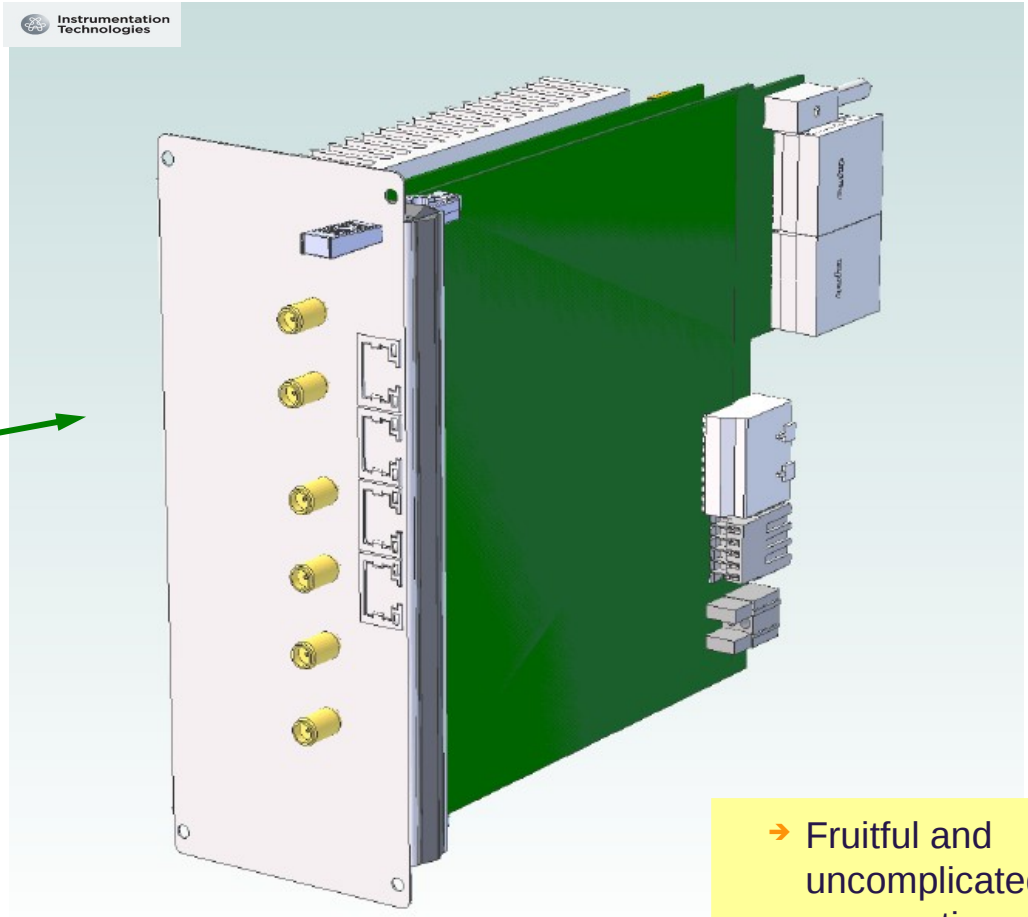


front

xTCA Crate – µLOG

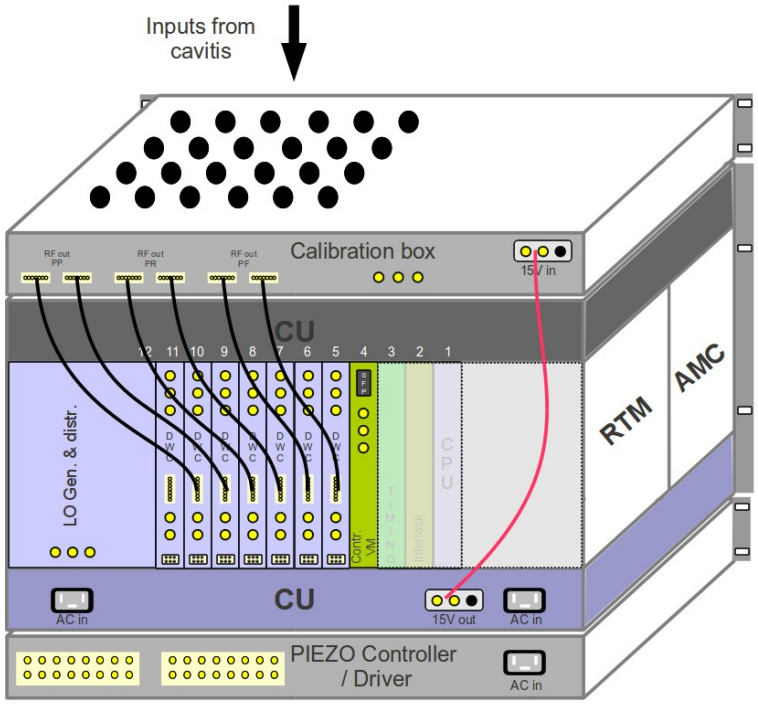
- uLOG : RTM low jitter signal generation

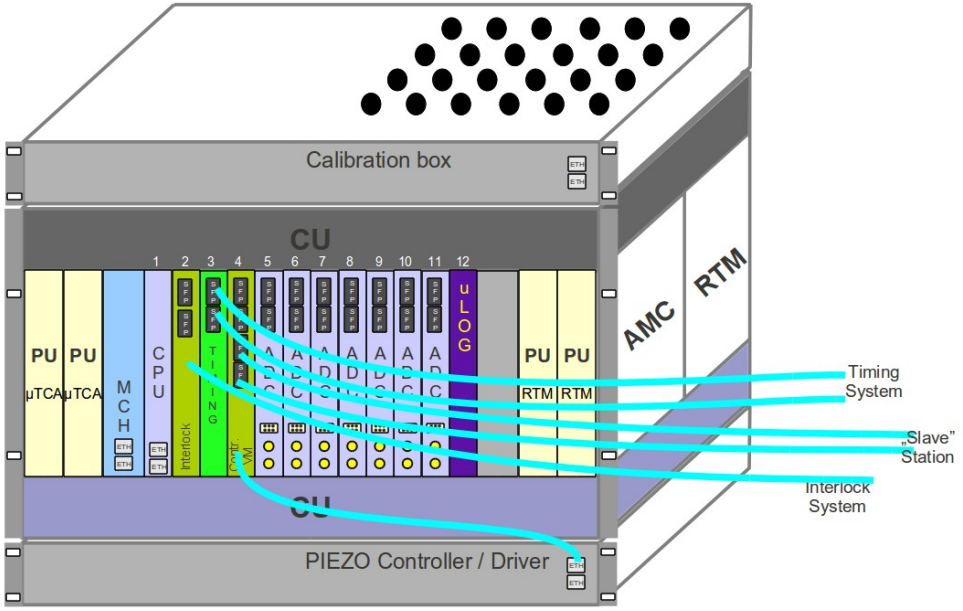




➔ Fruitful and uncomplicated cooperation.

LLRF in xTCA Crate

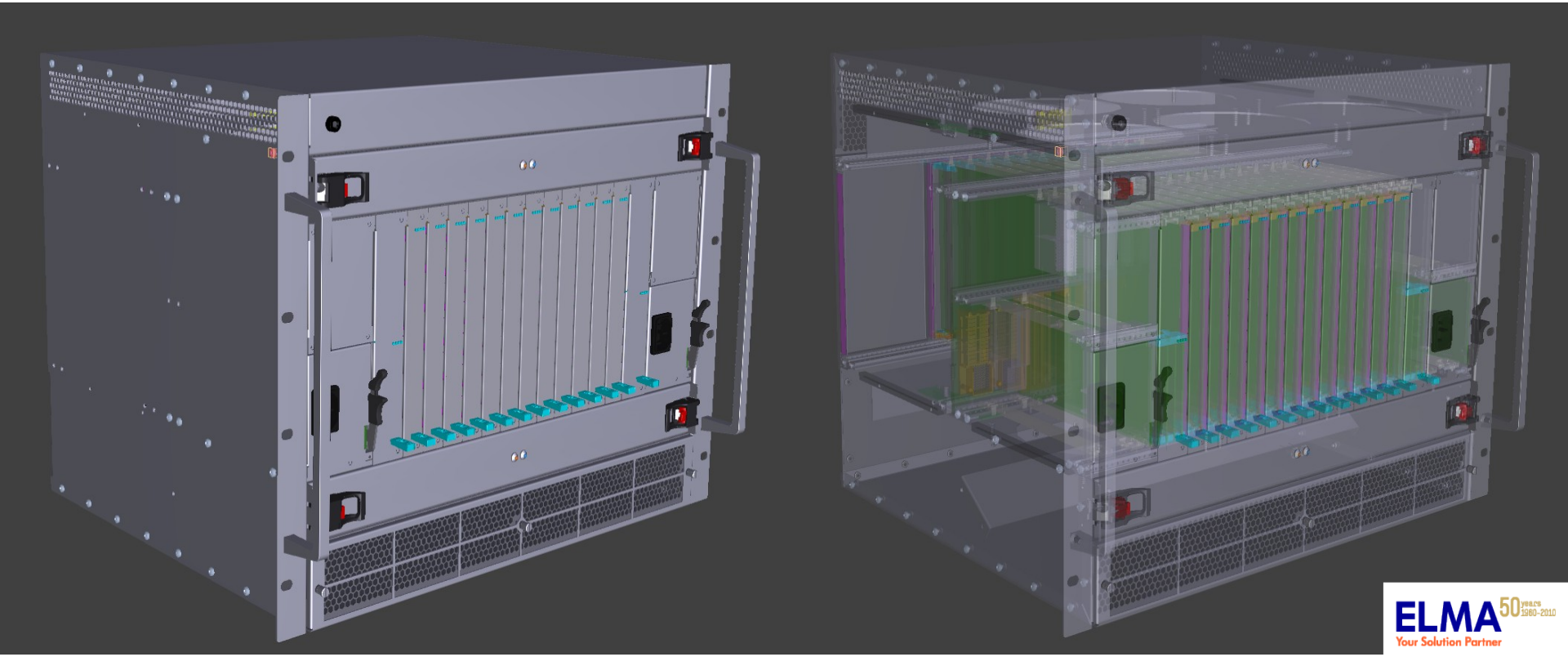




rear

front

xTCA Crate

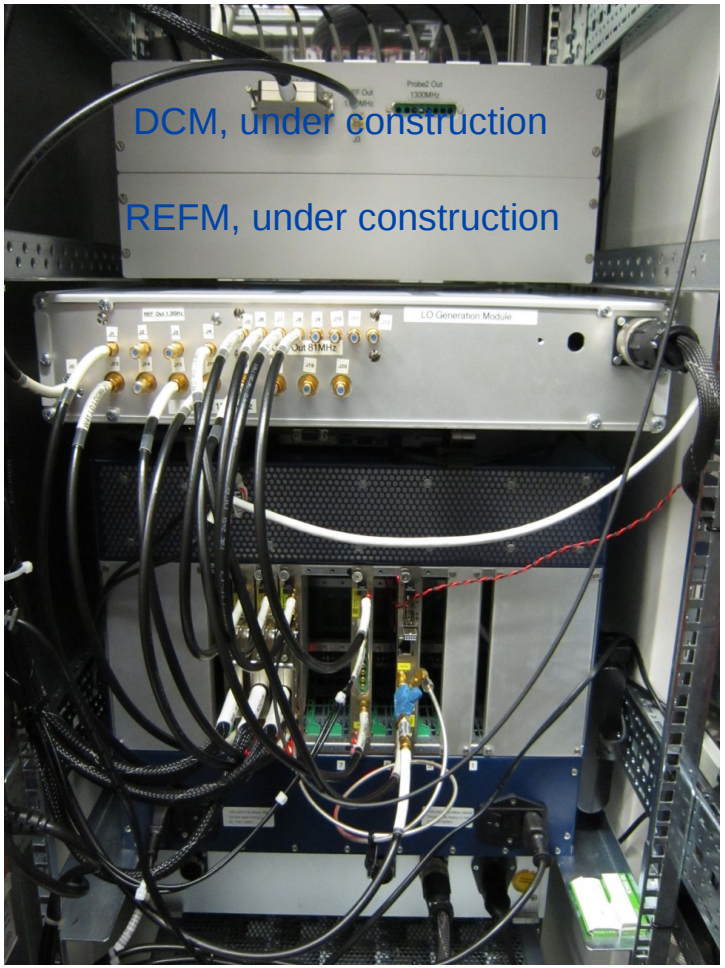


Courtesy: ELMA

Status 2011: FLASH injector prototype system

- uTCA Prototype Front view

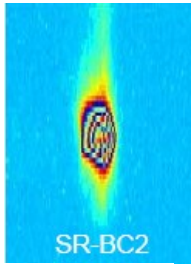
- uTCA Prototype Rear view

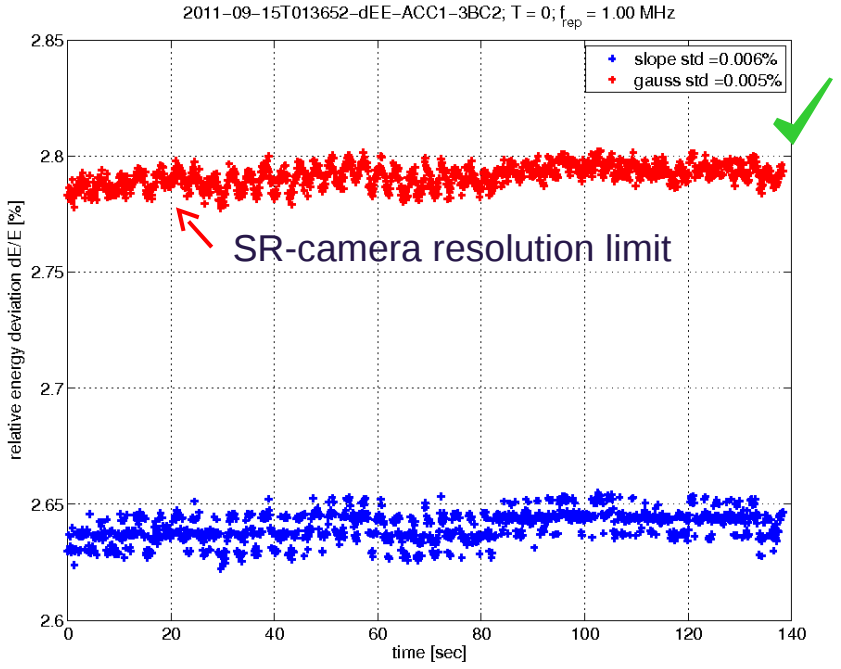


Beam operation using the uTCA-platform

- FLASH operation :

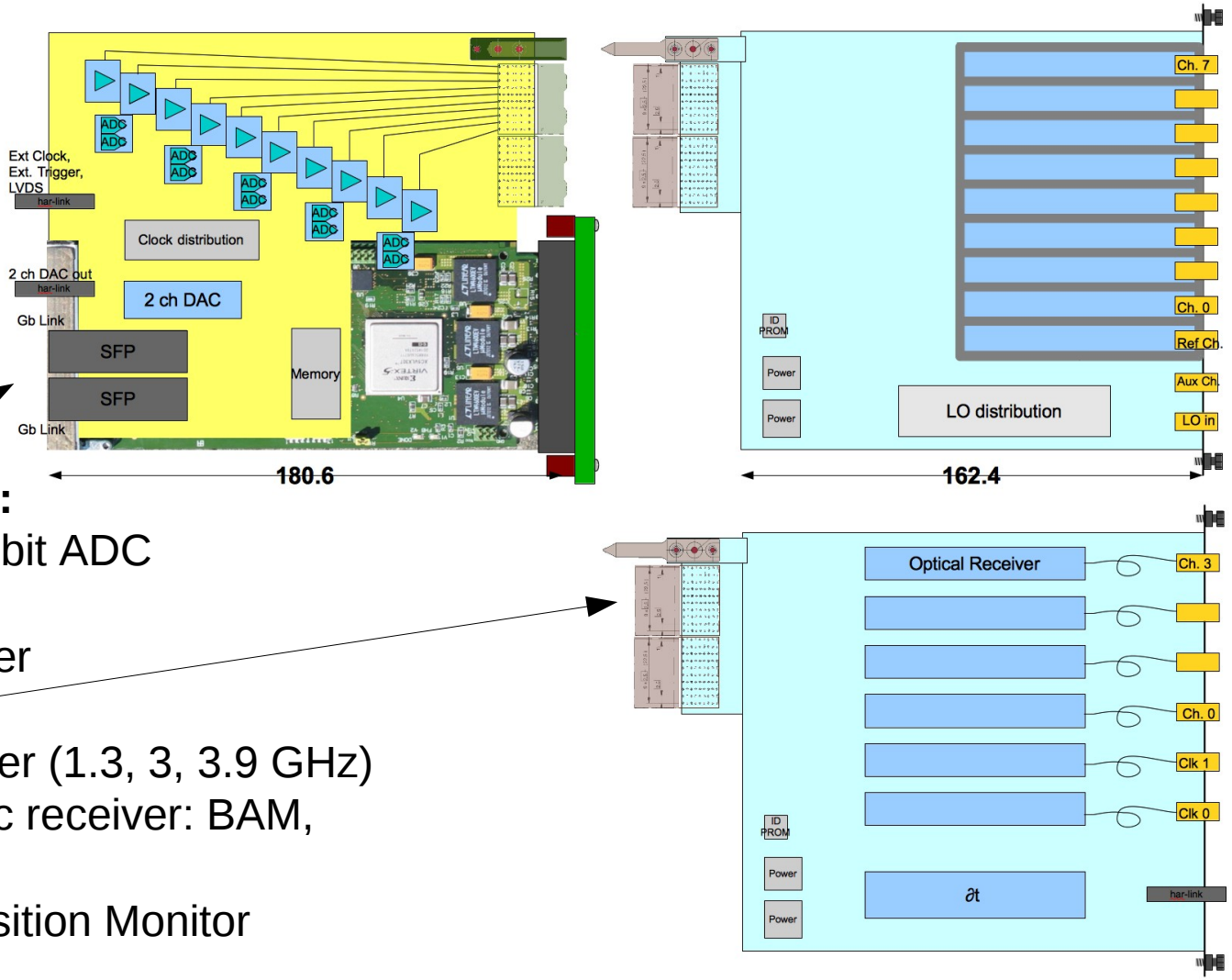
- On-crest energy stability :





→ Energy stability dE/E=5E-5.

uTCA LLRF hardware platform



Struck SIS8300:

10 Channels 16 bit ADC

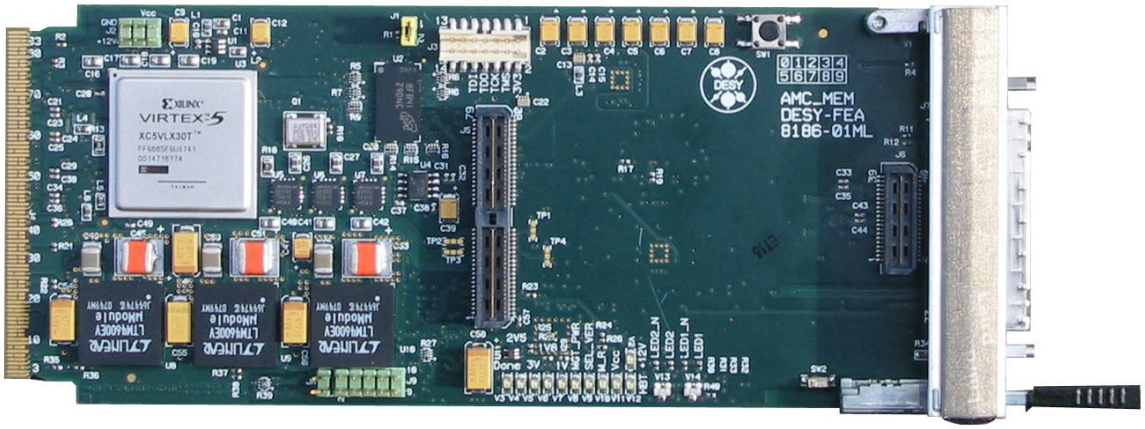
125 MSPS

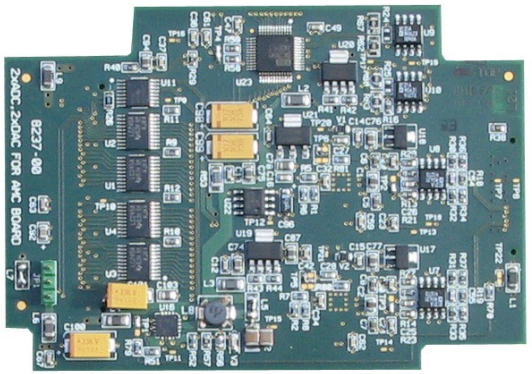
~200fs Clock jitter

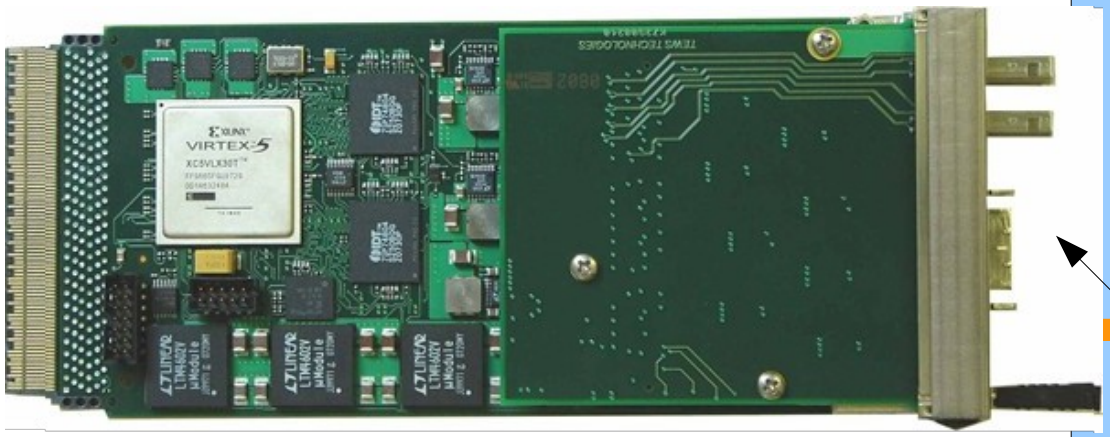
µRTM for:

- RF receiver (1.3, 3, 3.9 GHz)
- Fiber optic receiver: BAM, eBPM
- Beam Position Monitor

uTCA LLRF hardware platform

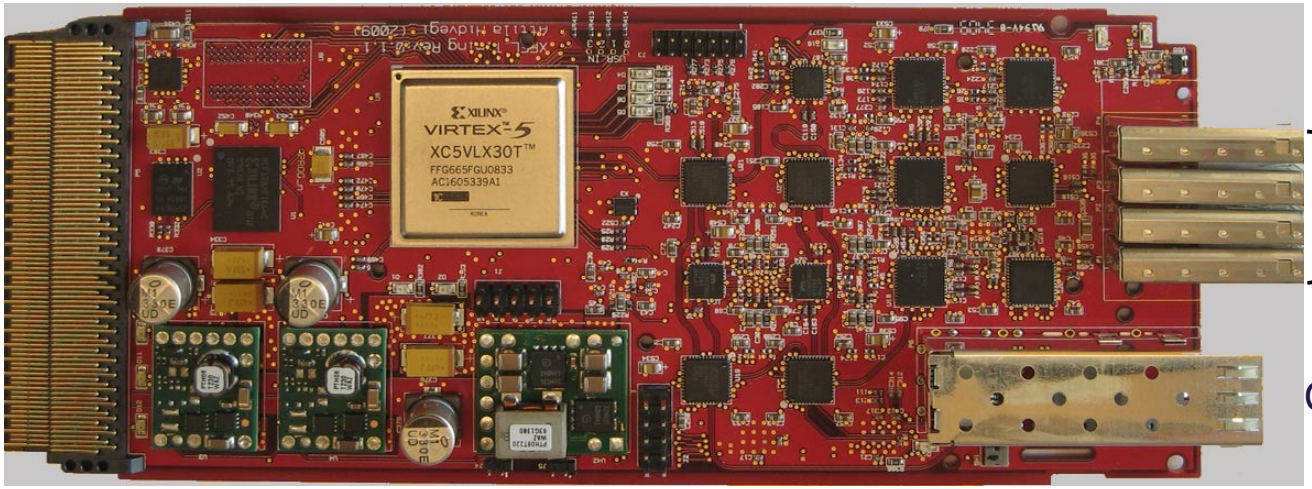






- DESY AMC 1
  - Virtex5, 256MB
  - 2ch ADC, 125 MSPS, 2ch DAC
  - Tested: BPM and Toroid readout with 81 Mhz
- TAMC900 (Tews)
  - 8ch ADC, 125MSPS
  - Tested: LLRF ATCA

uTCA LLRF hardware platform



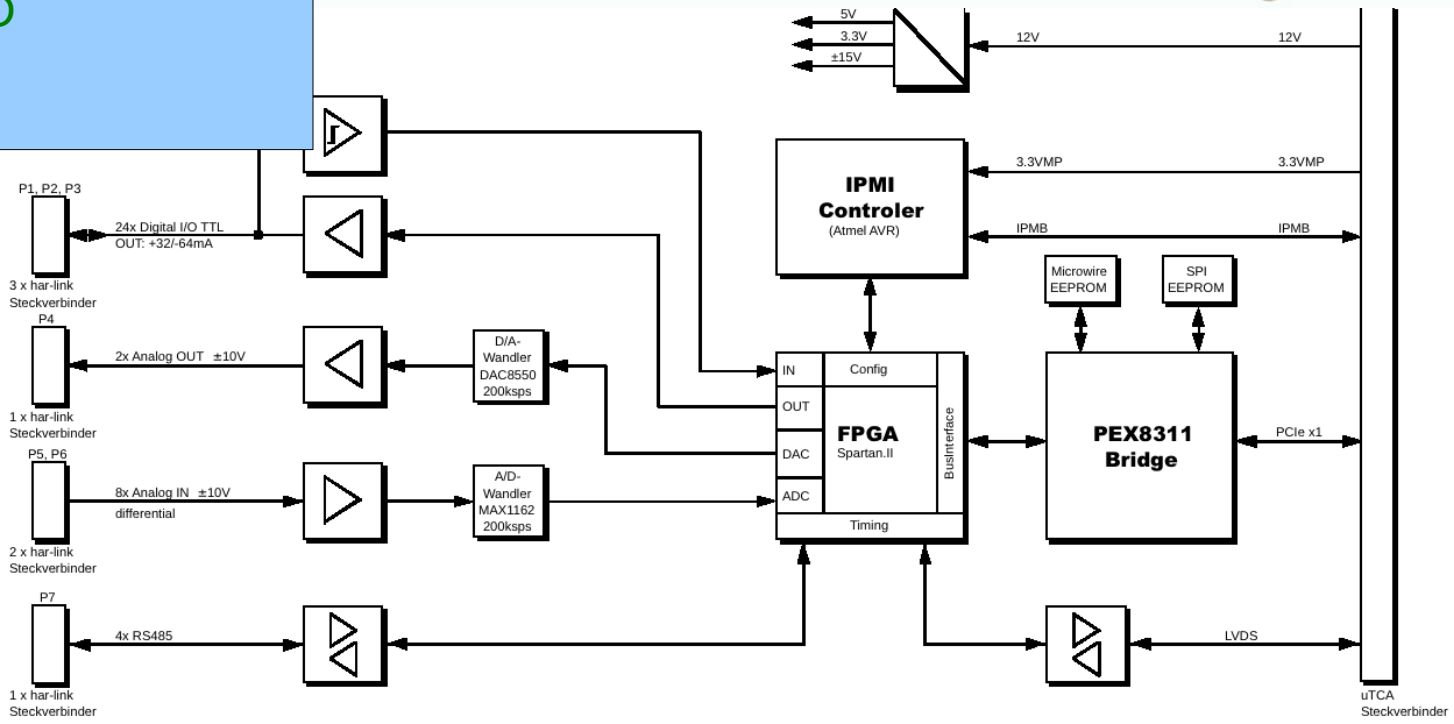
- Development of a ps stable timing system
  - Clock, trigger, interlock and event distribution
  - Fiber optic links (3.5 km), 1.3 GHz telegrams
  - Goal: < 5 ps jitter, 1.54 ns trigger resolution
  - Drift compensation on ps level

UNIVERSITET STOCKHOLMS
FYSIKUM

uTCA LLRF hardware platform

- A,D I/O
  - 8 ch ADC 200kHz
  - 2ch DAC
  - 24 I/O
  - 4 RS485
  - 1 lane PCIe

Available from ESD



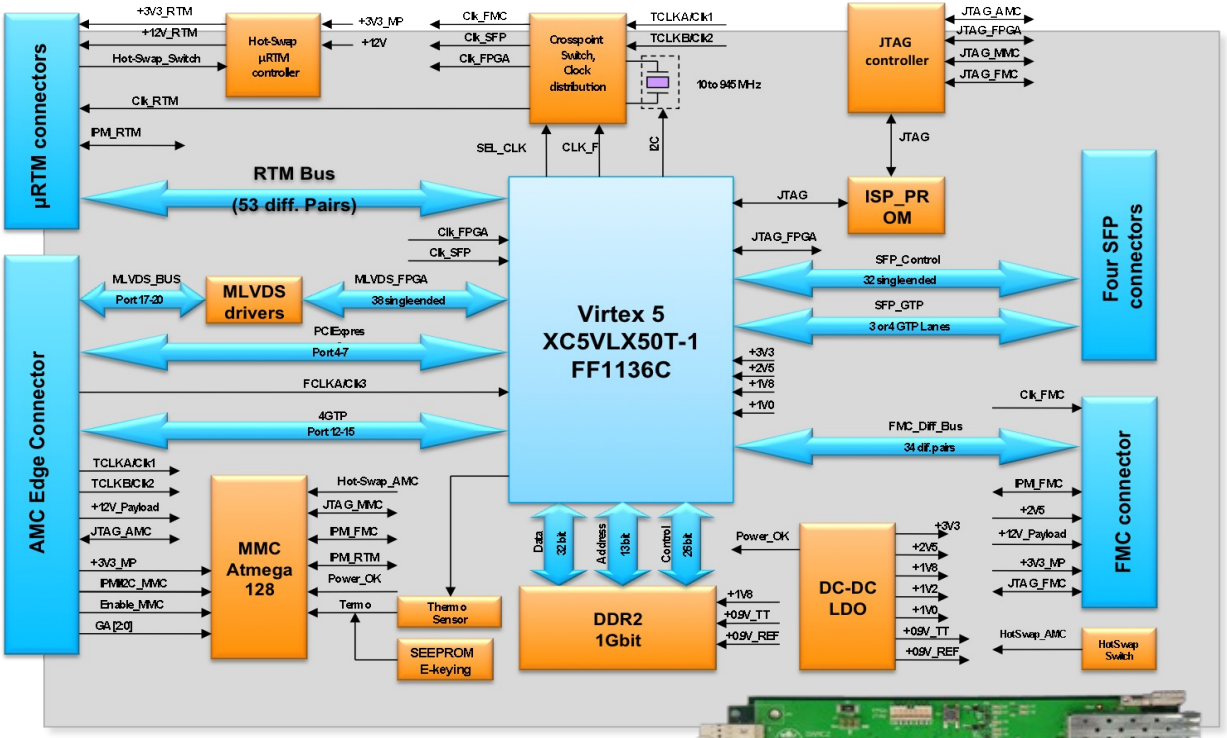
uTCA LLRF hardware platform

Digital I/O AMC with a Virtex 5 FPGA, 4 fiber optical links, FMC slot, memory and clock distribution.

* MPS

(Machine Protection System)

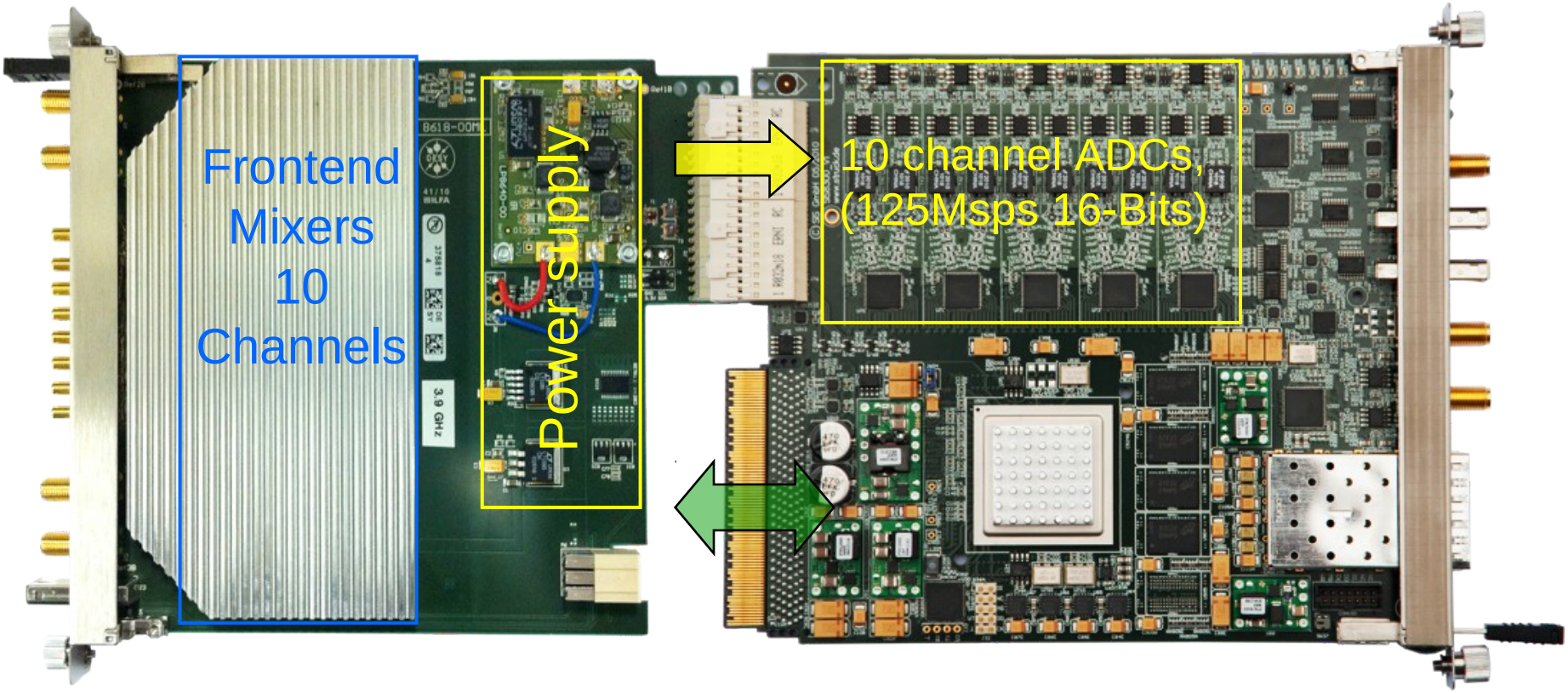
* Beam Loss Monitors
* Coupler Interlock
* Photo-diode readout



uTCA LLRF hardware platform

- 10-channel Down-Converter
- Digitizer, Partial Vector Sum

struck innovative systeme



- 10 channel field detection
  (1.3GHz, 3.0GHz, 3.9GHz)

- 10 channel ADCs (125Msps, 16-Bits)
- FPGA partial cavity vector sum
- Low latency links via uTCA-backplane

uTCA LLRF hardware platform

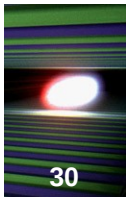
- Klystron Driver (VM)

- 2 channel vector modulator (108MHz, 216MHz, 1.3GHz…3.9GHz)
- 16-bit DAC

- µTCA Controller (µTC)

- 4xPCIe, 6 Fiber-Ports, 2 GB-Links
- FPGA(V5), DSP

Summary Conclusions



- **Prototype system has been successfully tested**
- **COTS modules available *(almost)***
- **Big interest from industry partners**
- **xTCA.4 under consideration by many labs for new project / upgrade (SLAC, CERN, ITER)**