Cornell University
Laboratory for Elementary-Particle Physics

An Overview of the Cornell ERL Injector LLRF System

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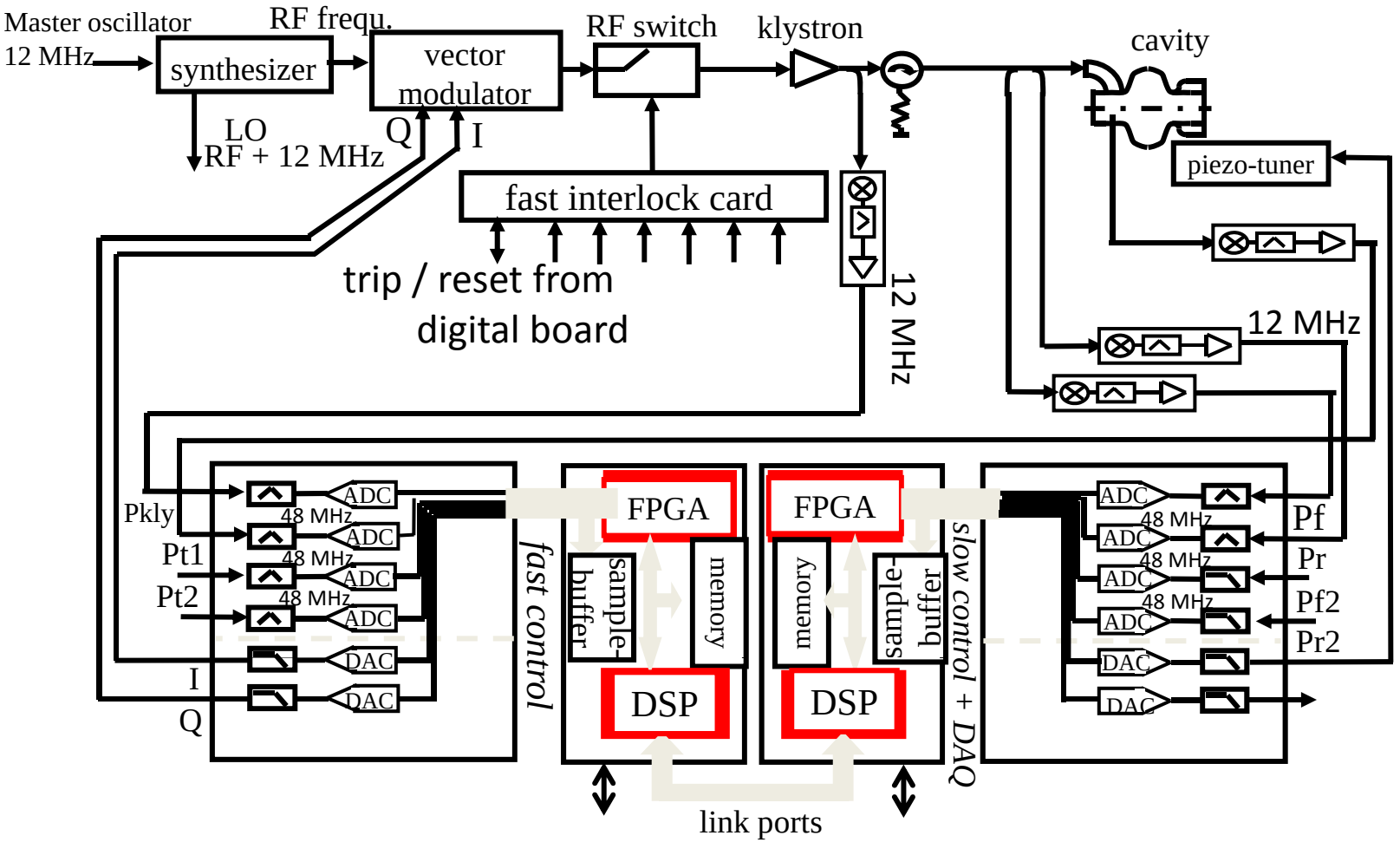
Outline

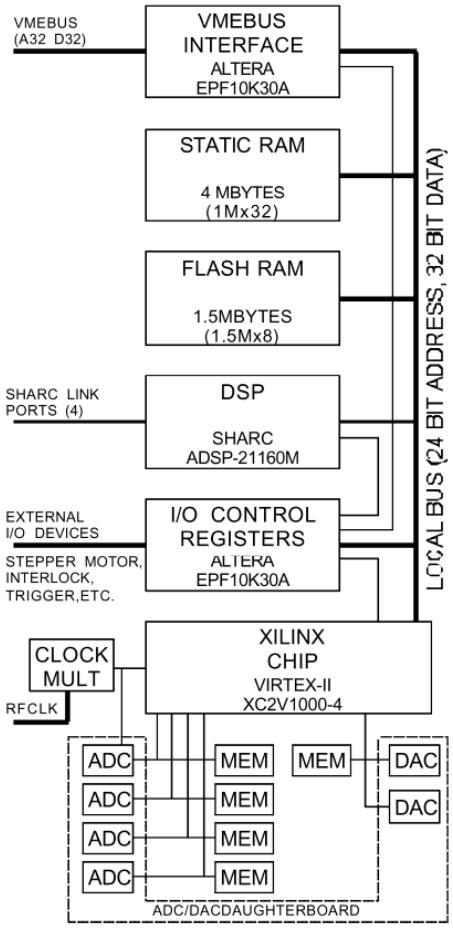
- Two Digital LLRF Systems Developed
  - Gen 1: 500MHz CESR LLRF Control System
    - Tested in CESR, CEBAF and JLAB FEL
  - Gen 2: ERL Phase 1a, 1.3 GHz ERL Injector LLRF Control System
    - Tested in Cornell ERL Injector and at HZB
- Future Plans
  - Production version for the Cornell ERL

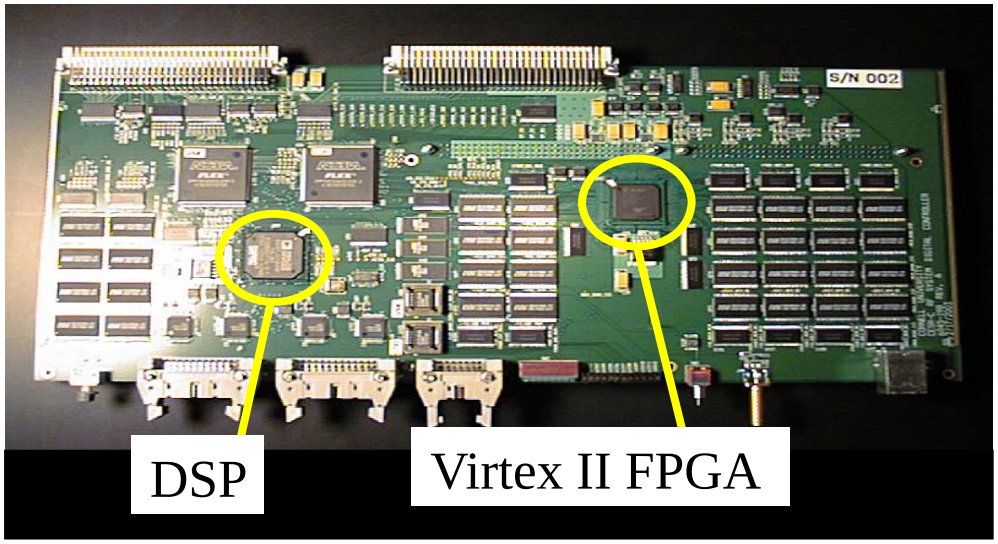
Gen 1: 500MHz CESR LLRF Control System

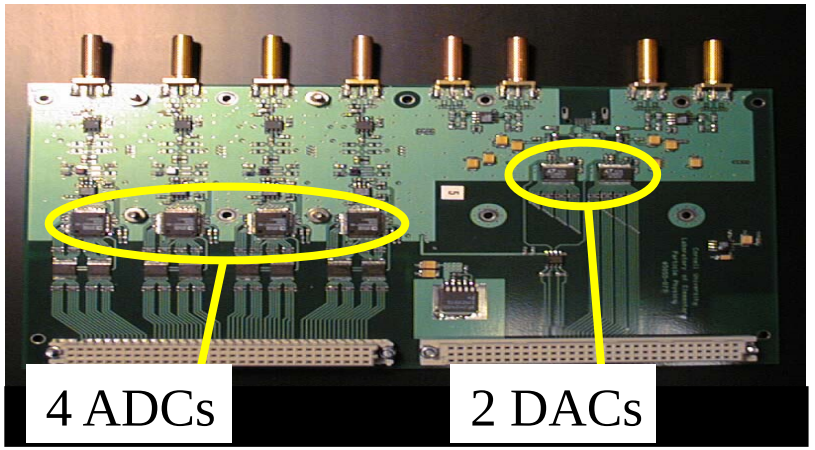
Gen 1: CESR LLRF Control System



Gen 1: CESR LLRF Control System







Gen 1: CESR LLRF Control System

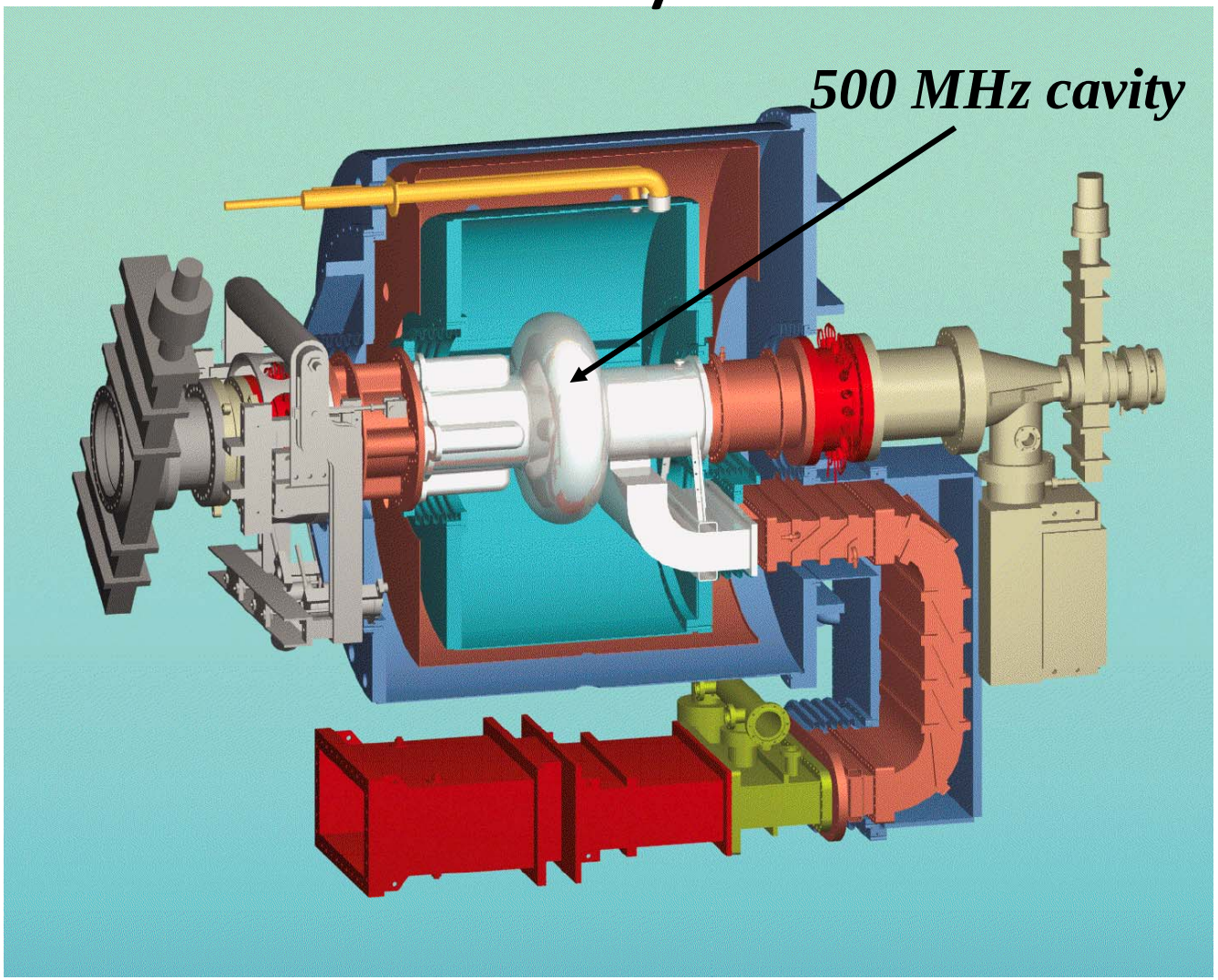
ADC daughter board:

- Four 14-bit 65 MHz analog to digital converters (ADCs) and two 16 bit 50 MHz digital to analog converters (DACs).
- High (74 dB) signal to noise ratio.

Processor board:

- 4 Mbytes of fast static RAM and 1.5 Mbytes of FLASH memory.
- The DSP is an Analog Devices ADSP-22160M. Four of the six DSP link ports are routed to connectors on the front panel (for connections between RF-DSP boards).
- The XILINX chip is Virtex-II XC2V1000-4. The fast RF control loops and data acquisition control run in this chip.
- Each ADC channel is provided with 2 Mbytes of buffer memory. Incoming data from the ADC are stored in this ring-buffer (1 Msample each).
- A separate memory buffer is provided for the dual functions of storing data directed to the DACs and for a Look-Up Table for feed-forward constants.

CESR Cryostat

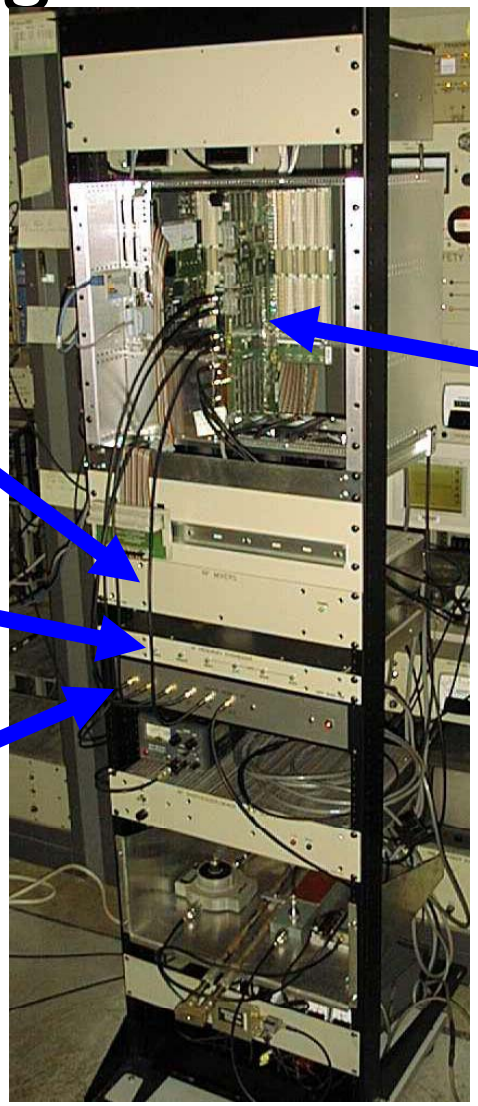


CESR Digital LLRF Control System

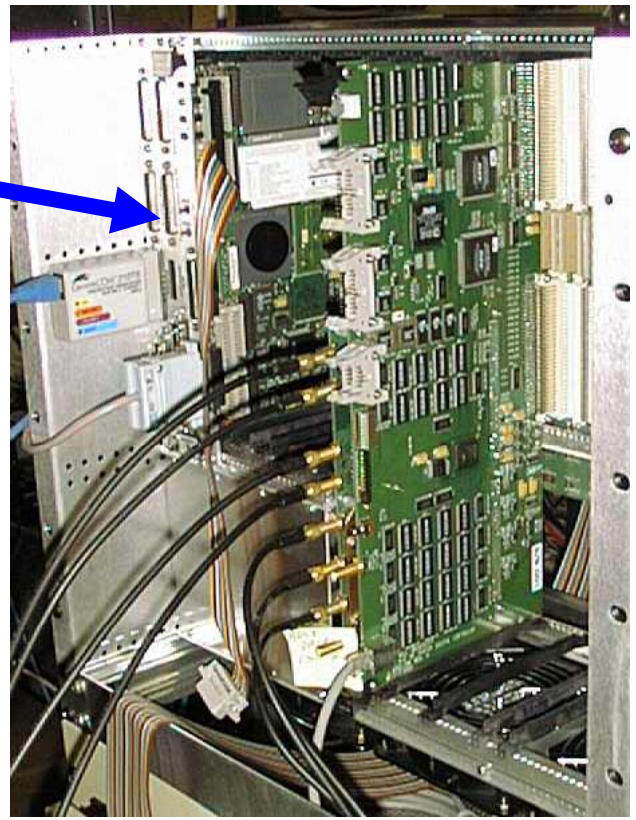
RF Down-Converters

500 MHz frequency synthesizer

vector modulator



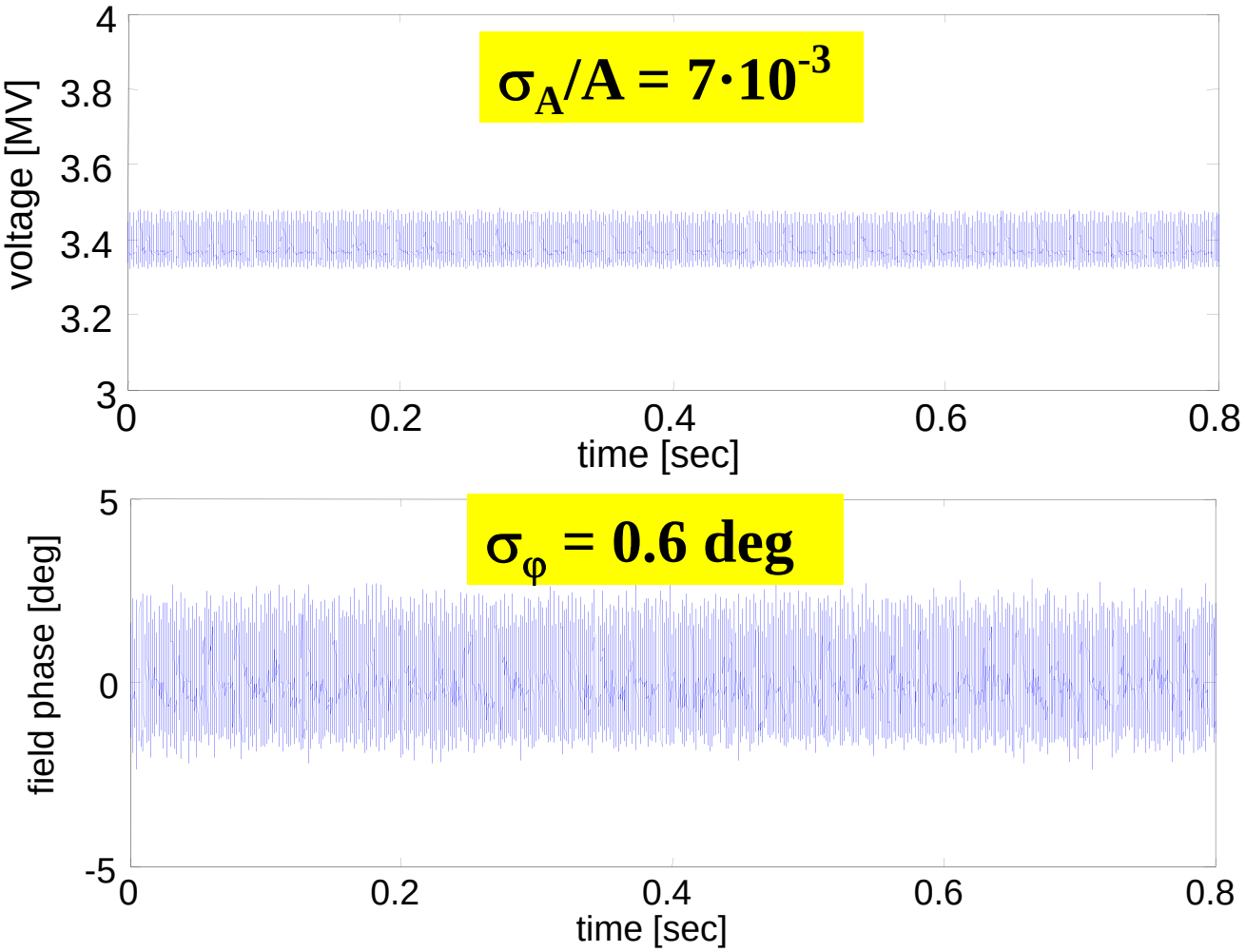
Digital Boards:



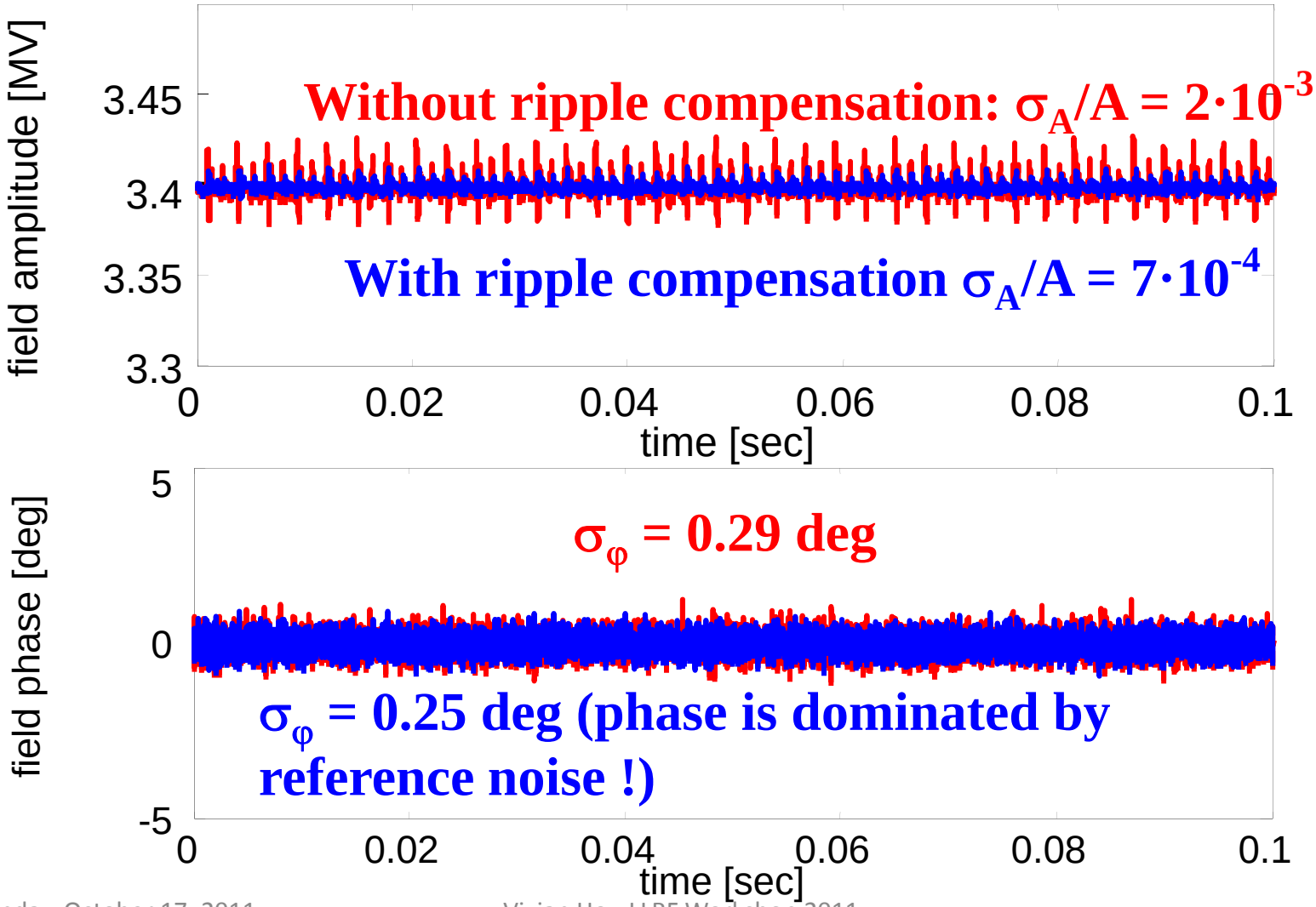
CESR RF Control System Features

- ✓ True vector sum control of the fields of the cavities W1 and W2 (proportional-integral gain cavity loop)
- ✓ PI control loop for the klystron output
- ✓ trip and quench detection
- ✓ state machine with auto-setup, auto-calibration and trip recovery
- ✓ tuner control (position and tuning angle mode)
- ✓ pulsed operation for cavity processing (incl. frequency synthesizer control, feedback loop on vacuum signal for pulse height or pulse length, flexible pulse rep.-rate)
- ✓ operation with adjustable klystron HV: power demand signal for klystron HV and klystron phase compensation
- ✓ klystron HV ripple compensation (feedforward)

Vector-Sum Field Stability with old analog System



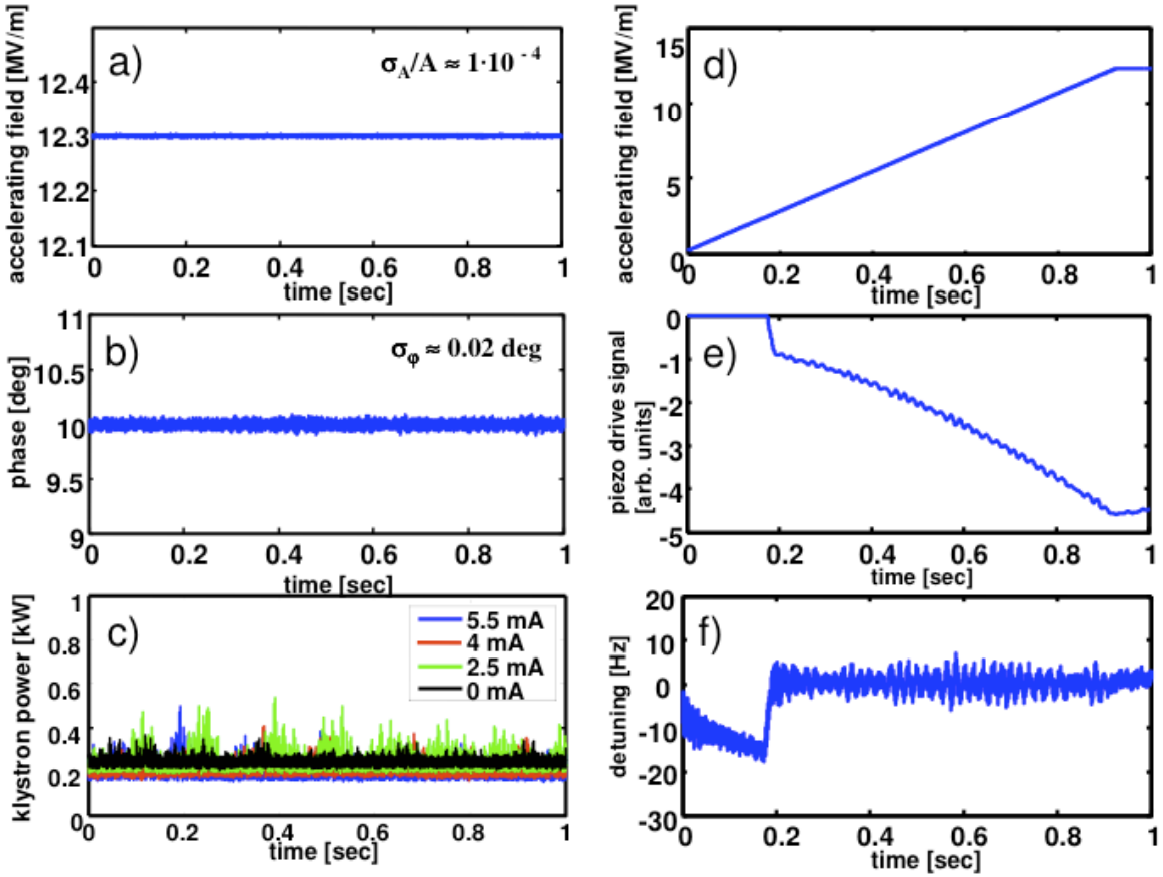
Vector-Sum Field Stability with new digital System



RF Control Test at the JLAB FEL

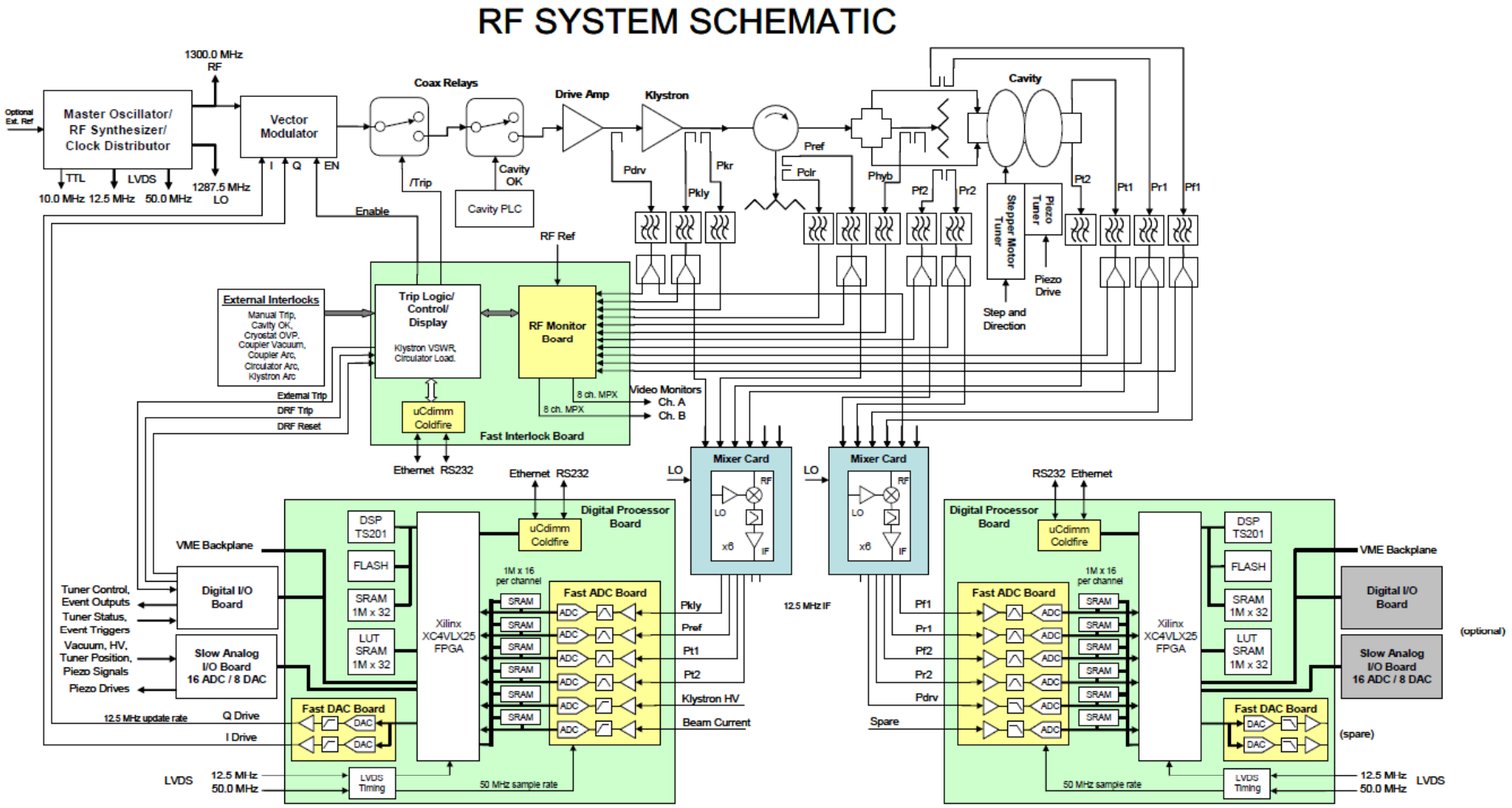
- Operated cavity at $Q_L=2\cdot10^7$ with 5 mA energy recovered beam.
- Operated cavity at $Q_L=1.2\cdot10^8$ with 5 mA energy recovered beam.
- Had the following control loops active:
  - PI loops for cavity field (I and Q component)
  - Stepping motor feedback for frequency control
  - Piezo tuner feedback for frequency control

Test Results – 7-Cell Cavity with a high loaded $Q_L = 1.2 \times 10^8$ at the TJNAF-FEL-ERL

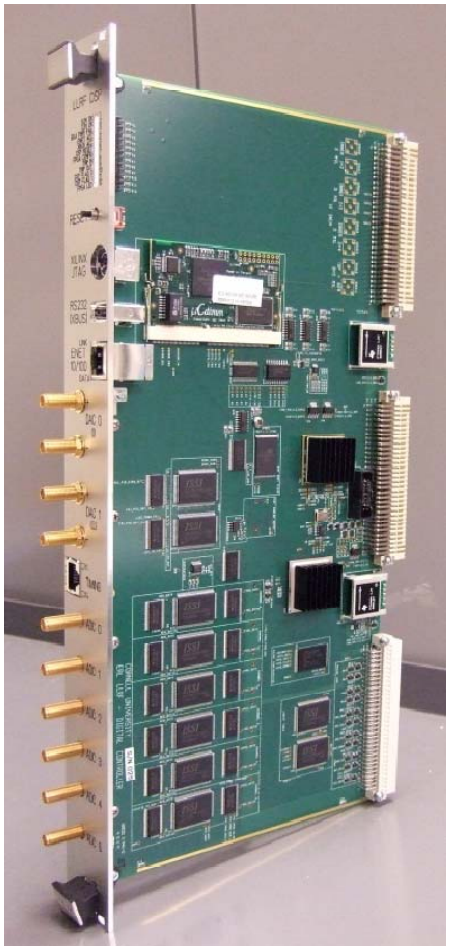


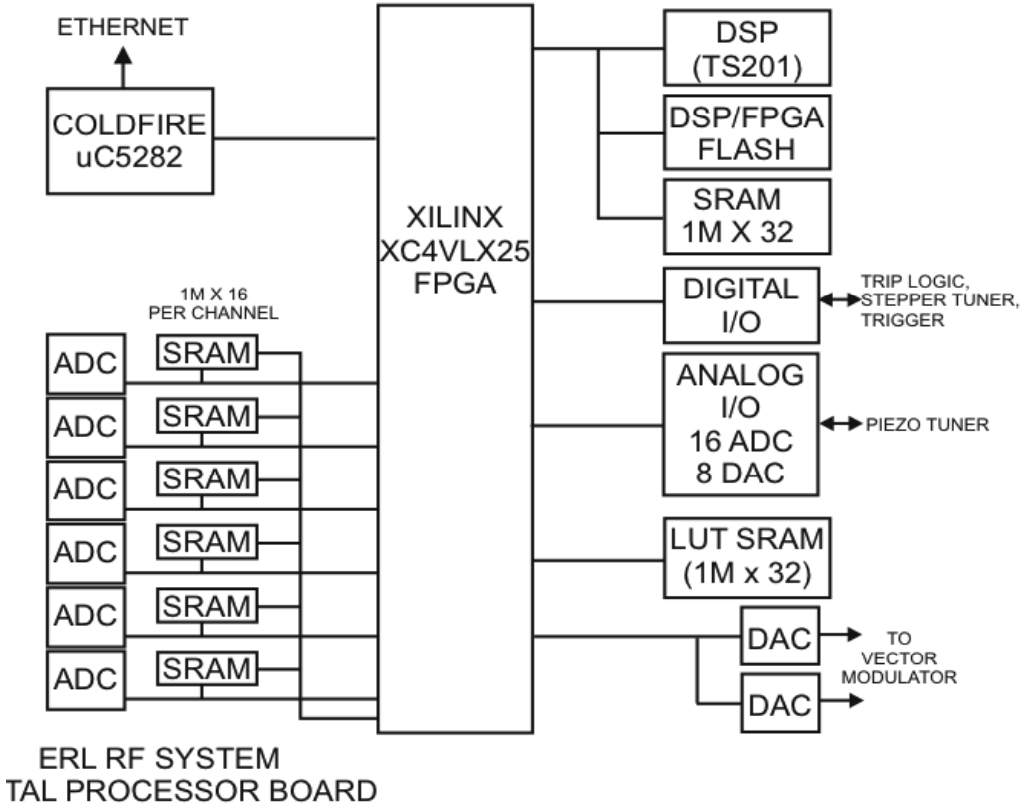
Gen 2: ERL Phase 1a, 1.3 GHz ERL Injector LLRF Control System

Cornell's ERL Injector LLRF Control System



Cornell's LLRF Control System





Cornell's LLRF Control System

Fast DAC board:

- 2 Channels – Differential Outputs
- Uses a Linear Technology LTC 1688 16-Bit DAC @ 12 Msps

Fast ADC board:

- 6 Channels
- Uses Linear Technology LTC2205 16-Bit ADC @ 50 Msps
- TI THS4271 Input Amplifier
- THS4511 Differential Amplifier ADC Driver
- Bandpass or Lowpass Filter

Cornell's LLRF Control System

Digital Processor Board:

- Xilinx XC4VLX25 Virtex-4 FPGA @ 100 MHz
- Analog Devices ADSP-TS201 TigerSHARC DSP @ 528 MHz
- 6 x 1M x 16 SRAM input channel memory
- 1M x 32 SRAM general purpose memory – ring and log buffers
- 1M x 32 SRAM lookup table storage
- 2M x 8 FLASH DSP boot memory
- 2M x 8 FLASH Xilinx configuration memory – JTAG interface
- Backplane interprocessor signaling
- uCdimm Coldfire 5282 board control and network interface
- 3U VME x 2 size – motherboard

System Features

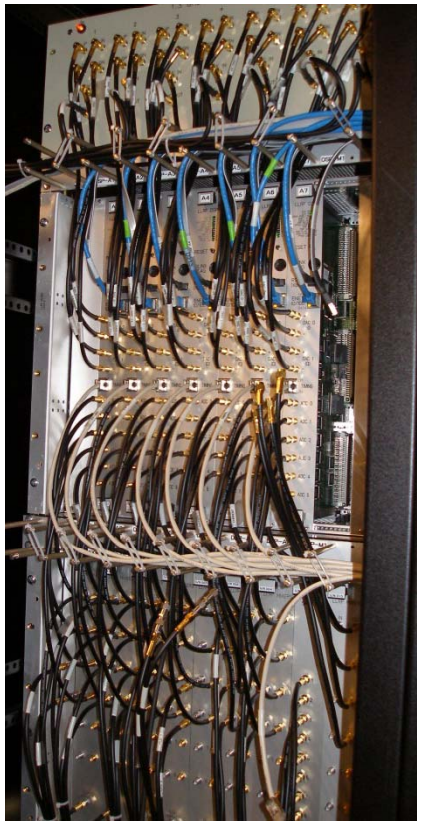
FPGA:

- Data transfer, filtering and down-sampling.
- Fast PI loops (cavity and klystron)
- Fast feedforward (ripple and klystron phase)

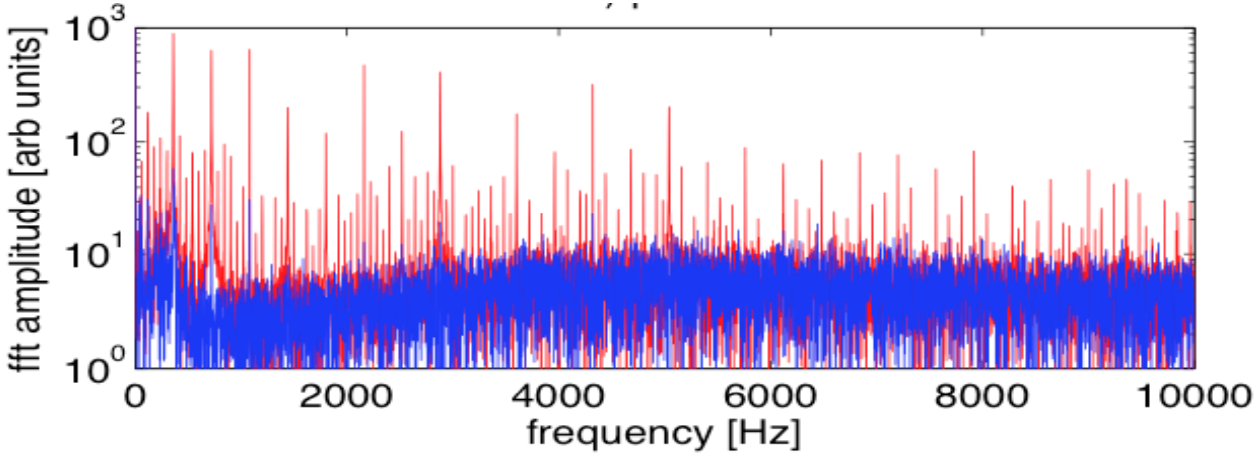
DSP:

- State machine: auto-turn on, auto-calibration, trip recovery,…
- Trip/quench detection
- Pulsed mode operation
- Cavity frequency feedback loop (tuner and piezo control)

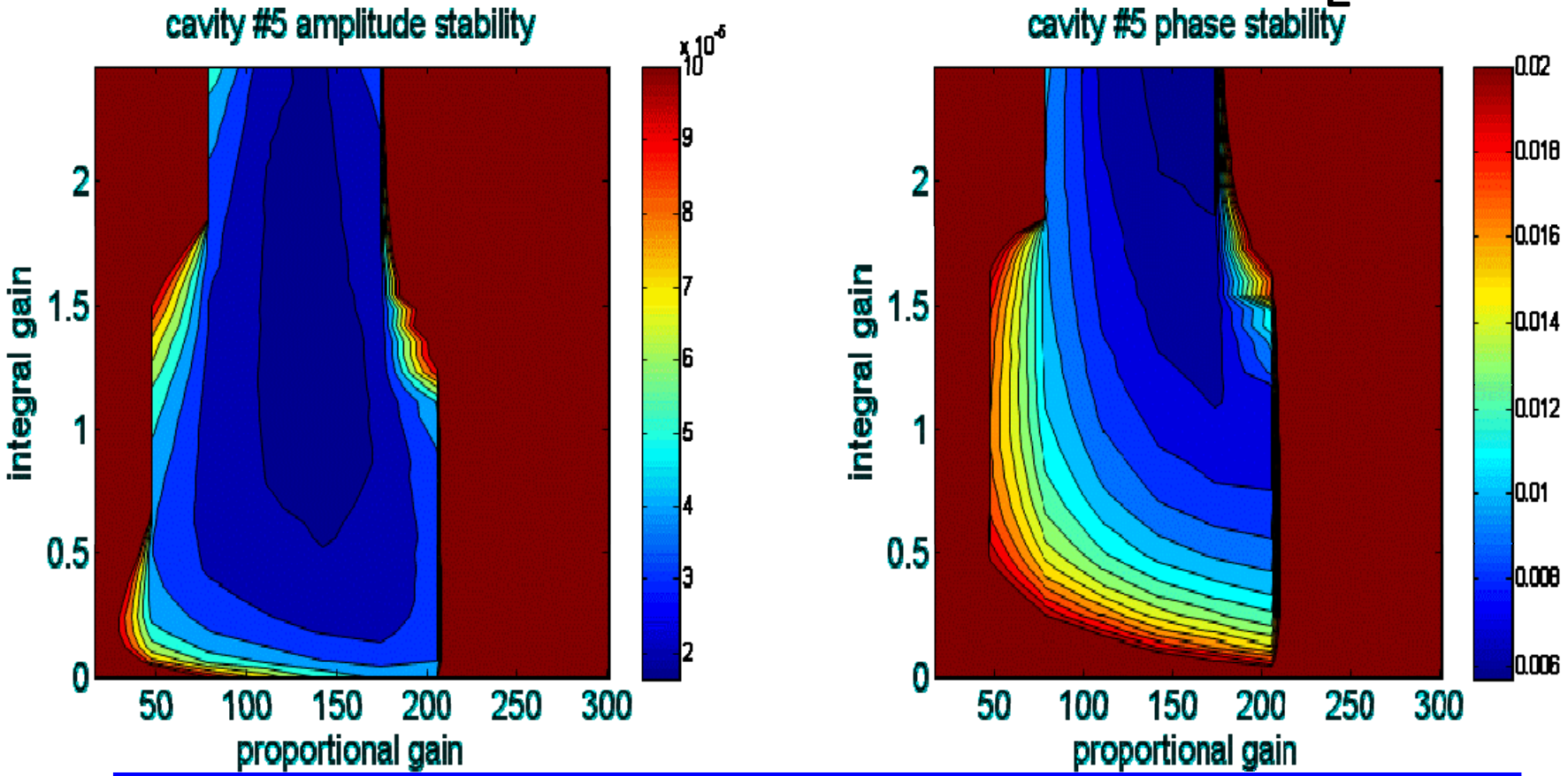
ERL Injector LLRF System Highlights



- LLRF electronics for the ERL injector is a new, improved generation of LLRF system previously developed for CESR
  - <1 μs latency feedback loop
  - Beam current feedforward
  - Klystron HV ripple feedforward
  - Fast tuner loops for microphonics compensation
  - Built in state machine
- Performs well with excellent field stability



RF Field Stability Test at low Q_L

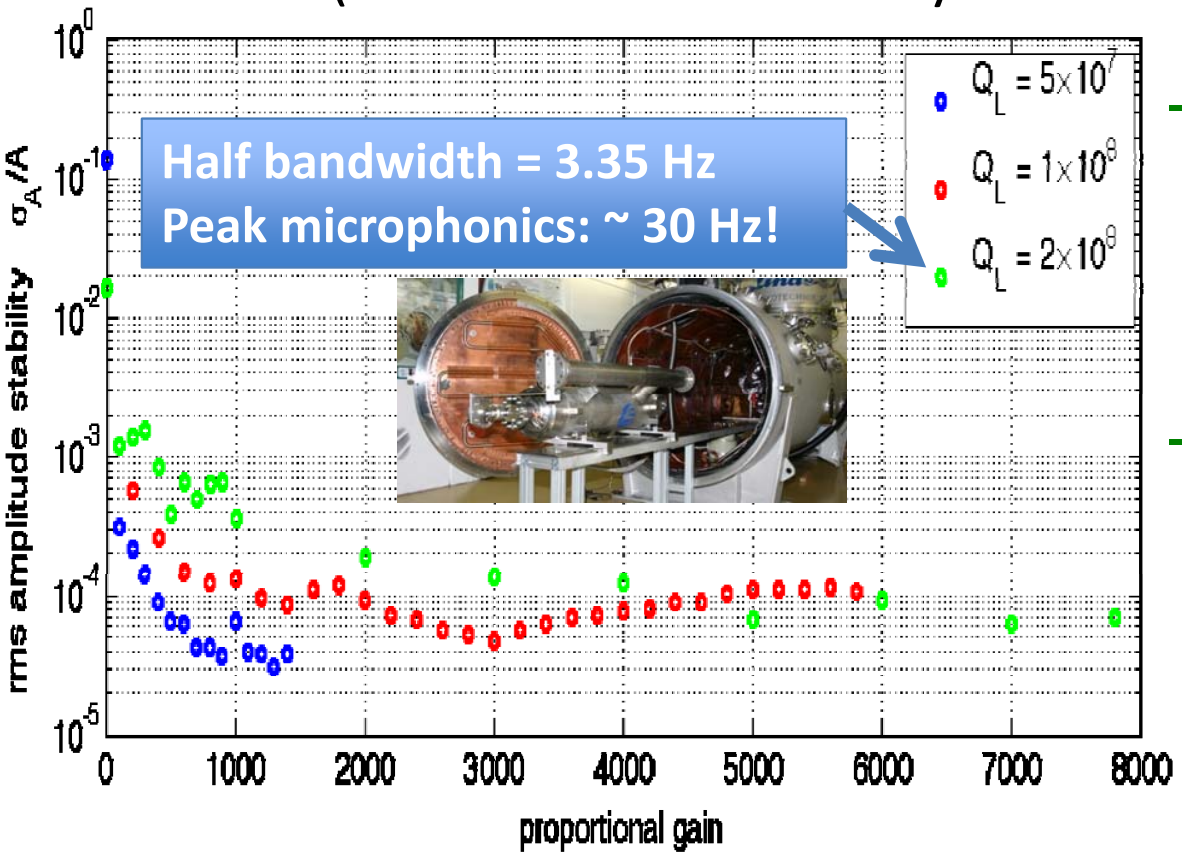


Excellent field stability achieved: amplitude: $\sigma_A/A < 2 \cdot 10^{-5}$

phase: $\sigma_P < 0.01$ deg

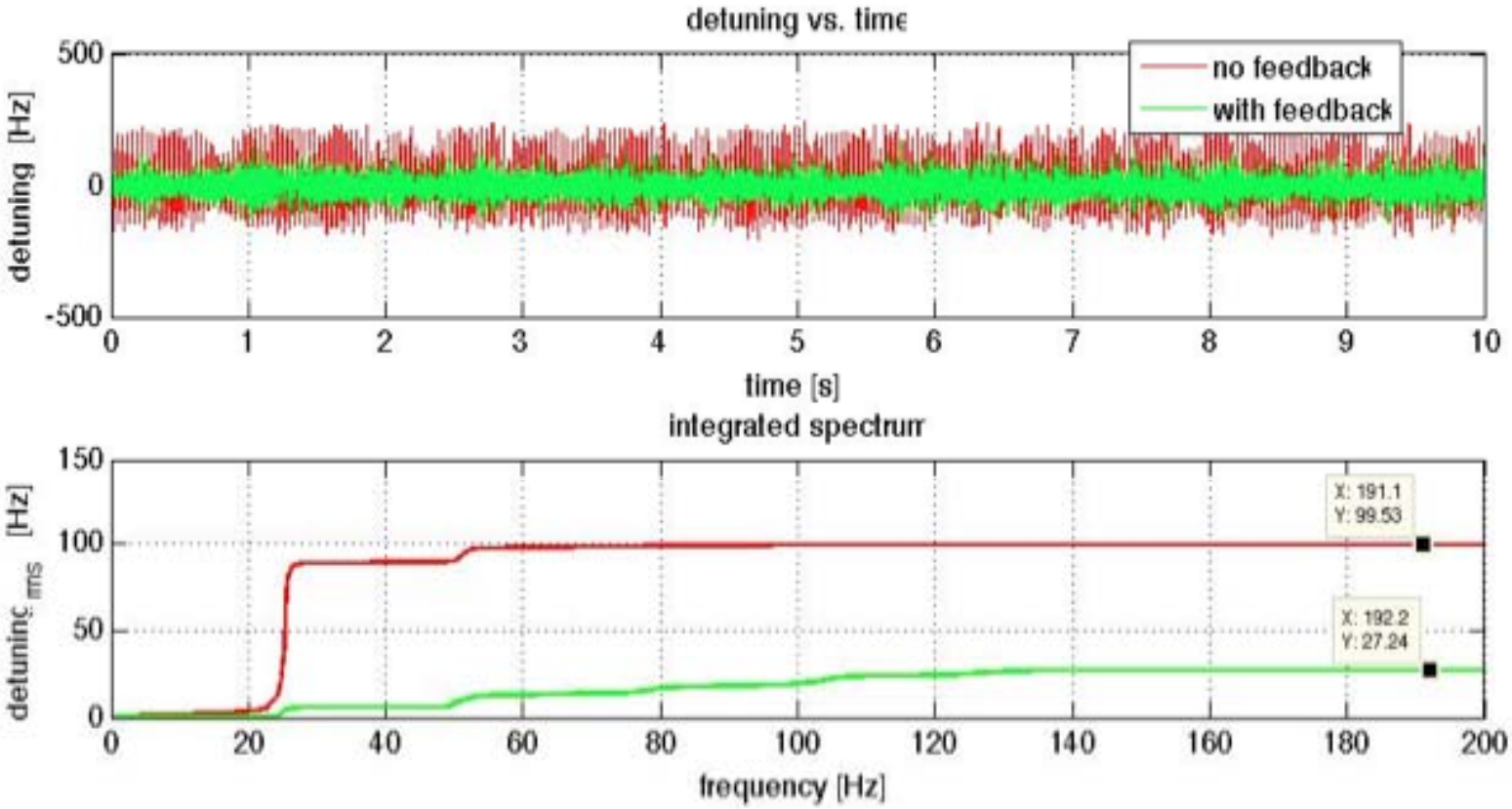
LLRF Field Control and Operation at Very High Loaded Q

- **Demonstrated highly efficient operation of a full 9-cell cavity at very high loaded quality factors up to $2 \cdot 10^8$** (Test of Cornell's LLRF system at HoBiCaT at HZB)



- **Exceptional field stability: σ_A/A <$1 \cdot 10^{-4}$, σ_φ ~ 0.01°**
- **Fast RF field ramp up in 0.5 s to high fields with piezo tuner**

Microphonics compensation by a fast piezo-electric tuner in feedback mode



Future Plans

Future Plans

- R&D phase completed:
  - Meet field stability specs for ERL injector (high current) and main linac (high loaded Q)
- Next: Design of final LLRF system for full scale ERL
  - Design for high reliability
  - Design for radiation hardness and radiation management
  - Design for tunnel: remote diagnostics, fast replacement

Conclusions

- The generation 2 ERL Phase 1 a LLRF digital system was tested very successfully in the Cornell ERL injector, the TJNAF-FEL-ERL, and HoBiCaT at HZB
  - Exceeds ERL field stability specs
  - Operates well for wide rage of loaded Q (<1e5 to >1e8)