Contribution ID: **2** Type: **not specified**

A method for removal of the measurement noise caused by clock jitter in RF digital demodulation techniques.

Thursday 20 October 2011 10:20 (20 minutes)

Modern LLRF systems make use of RF sampling techniques (I/Q or non-I/Q) to feed digital processing circuits with amplitude and phase measurements of the RF signals of interest. The control of RF accelerator fields must often be performed with a high degree of precision, and the control algorithms must react with low latencies (microseconds). For these reasons, the raw measurement precision is crucial. One of the main limitations of the measurement precision in I/Q or non-I/Q sampling techniques, is the noise generated by the sampling clock jitter. To limit its effect, a high purity sampling clock generation hardware is commonly involved, in conjunction with frequency down-conversion stages.
This paper discloses an easy-to-implement method which allows lowering or cancelling the contribution of the sampling clock jitter to the measurement noise. It shows modeling results, as well as experimental results obtained with the direct sampling of 700 MHz signals.

Primary author: Mr GALDEMARD, Philippe (C.E.A. / Saclay , DSM/Irfu/SIS)

Presenter: Mr GALDEMARD, Philippe (C.E.A. / Saclay , DSM/Irfu/SIS)

Session Classification: Session 10