Experimental results and last improvements for the LLRF superconducting cavity control system at IPNO

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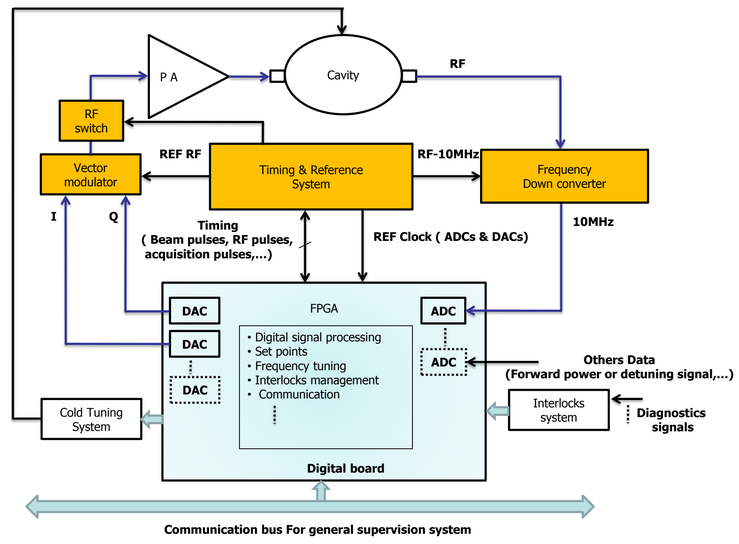
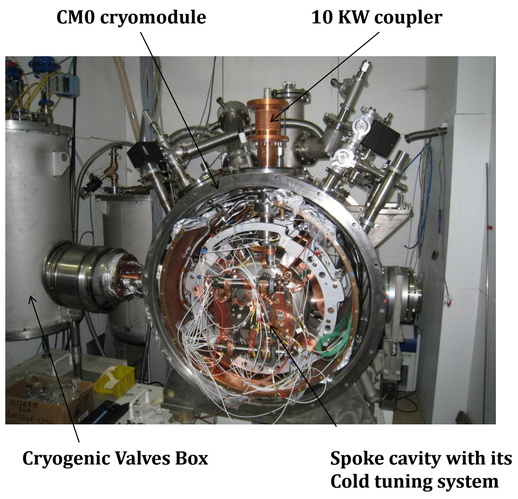
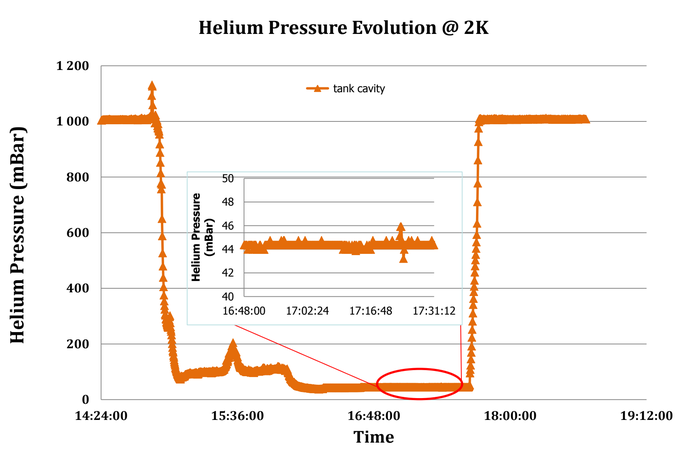
Within the framework of the R&D on superconducting SPOKE cavities, a Digital Low Level Radio Frequency system was developed at IPN Orsay in association with LPNHE Paris, two IN2P3-CNRS laboratories. The work presented focuses on the complete system tests of the two versions for a comparison, at high power (until 10kW) by using the SPOKE cryomodule (352MHz@2K).
Concurrently, we shall present the last developments, a new version of the RF system based on SMD components and RF PCB instead of coaxial components as well as a new version of the analogue mezzanine board allowing to test "Clock cleaner" and new ADC's front-end.

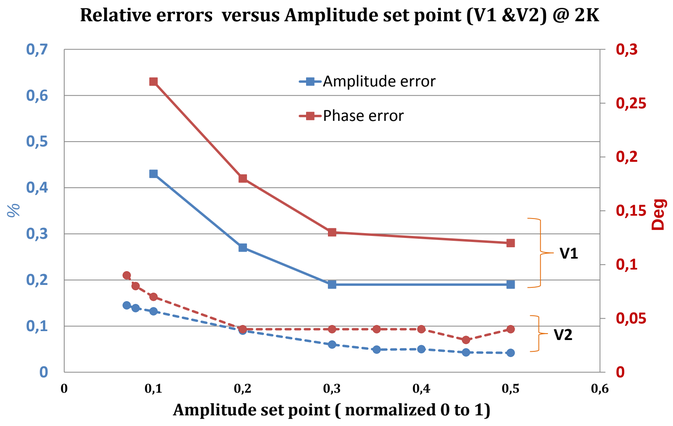


COLD TESTS RESULTS



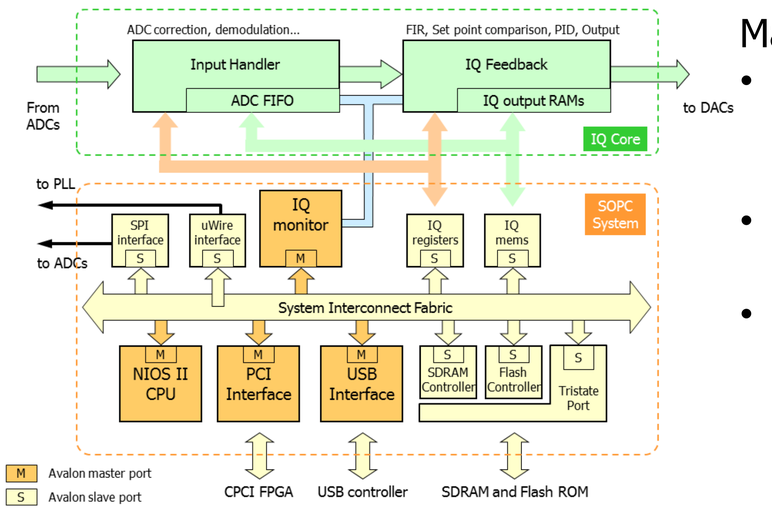


Regulation with both version boards was evaluated in realistic conditions on CM0 cryomodule. The 352 MHz SPOKE cavity was subject to disturbances but limited @2K. Moreover the Cold Tuning System guaranteed a frequency regulation of ±5 Hz.



The obtained results validate by comparison the second version of our LLRF system with performance better than 0.5% in amplitude and 0.5 degrees in phase. But the performances are perhaps limited by the phase noise of 80MHz Clock

VHDL ARCHITECTURE



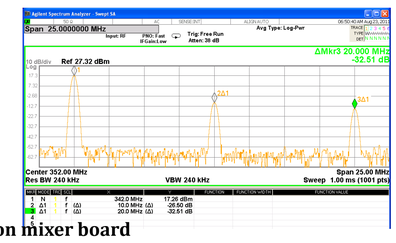
Main FPGA key features:

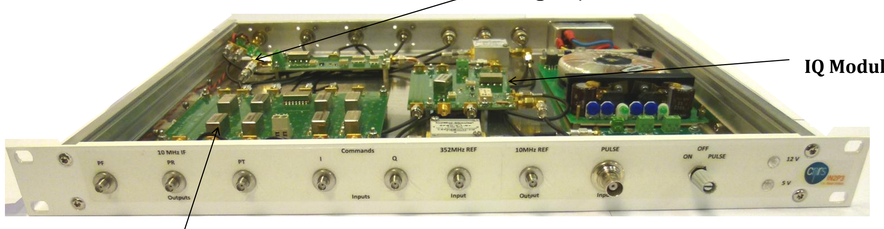
- IQ control loop: IQ demodulation, FIR and PID filtering
- Online monitoring via SDRAM
- Slow control and automated tasks via an embedded NIOS II softcore processor

NEW 352MHz RF SYSTEM

Features :

- 4 down- converter channels board
- Image rejection mixer board
- IQ Modulator board
- RF switch

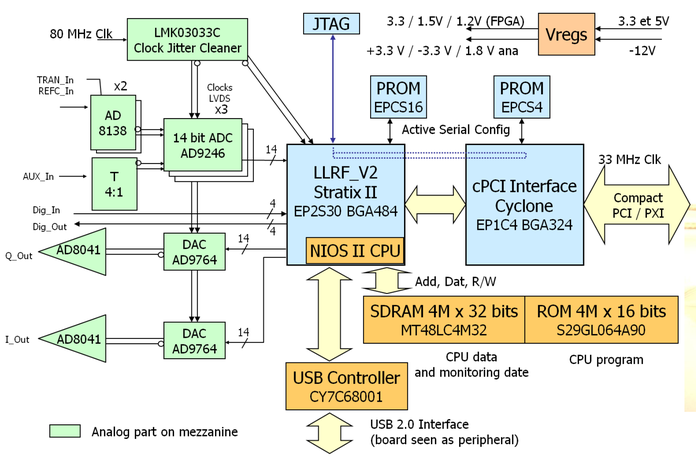


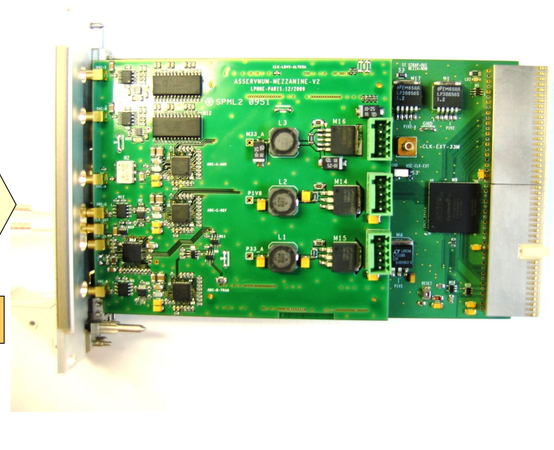


All the printed circuits were developed with the aim of using them with various frequencies (88MHz , 176MHz,352MHz and 704MHz) thanks to the use of narrow band components having the same layout.

The preliminary results show a good image frequency rejection of the LO signal and a jitter value near the reference jitter value. Other measurements are in progress.

NEW FRONT-END BOARD





Digital mother board: CPCI interface, main FPGA board, memories and peripheral USB 2 interface.
New analog daughter board:

- 3 ADC + 2 DAC (14 bits @ 80 MHz)
- better clock distribution from clock jitter cleaner (< 800 fs)
- better power supply distribution

FUTURE

- Complete validation of the new two developments (Front-end board and RF system).
- Development of a low phase noise timing system and two Cavity simulators for testing fault tolerance performances within the framework of the European project MAX.
- Development of a complete LLRF system integrating a Cold tuning system (low and fast tuning) interface, interlocks for RF source, RF power coupler and ...