LLRF system for the X-band high power test stand at CERN

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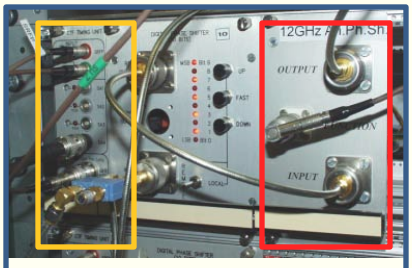
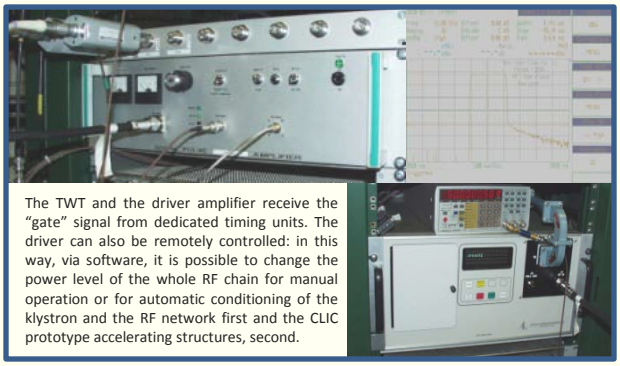
Abstract: The CLIC study at CERN is constructing a new 12 GHz high power test stand dedicated to condition and to test CLIC prototype accelerating structures. The test stand is based on a 50 MW X-band klystron developed by SLAC and a solid state high voltage modulator. The system should complement the beam based power production with CTF3.

A sophisticated LLRF system has been developed for the test stand allowing flexible and fast changes of power levels, pulse length and phase. The system has to be fully remote controlled by an automated conditioning software allowing around the clock operation. The electronics, inspired by the CTF3 LLRF system working at 3 GHz, has been developed for controlling and measuring the RF signals including the phase programming and tuning control for exploiting the novel SLED-I type pulse compression system. Results from the first part of commissioning are reported.

The SIMATIC S7 is the interface between the control system and the installed hardware. It also manages the interlock signals and drives the motors which allow for changes to the pulse compressor tuning.

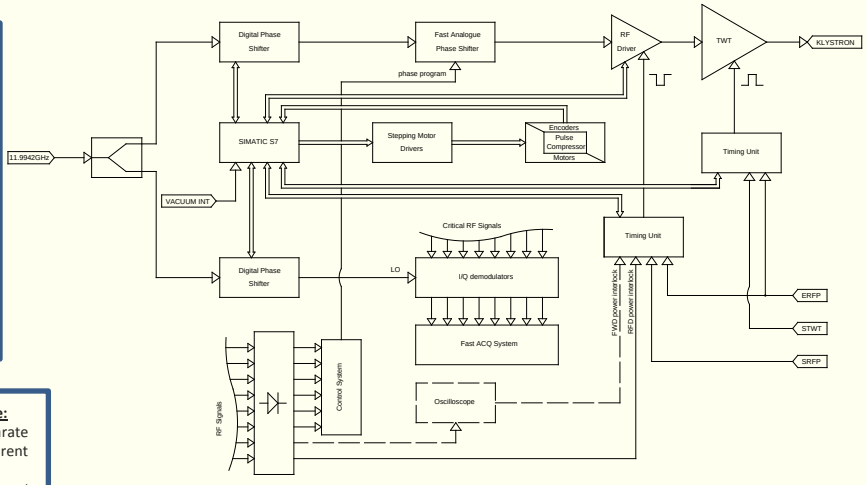


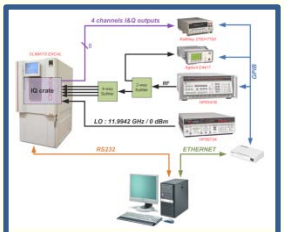
In the orange frame: the timing unit which allows for the shaping of the pulse length and manages the reflected and forward power interlocks.
In the red frame: the fast analogue phase shifter, core of the pulse compression system.



The TWT and the driver amplifier receive the "gate" signal from dedicated timing units. The driver can also be remotely controlled: in this way, via software, it is possible to change the power level of the whole RF chain for manual operation or for automatic conditioning of the klystron and the RF network first and the CLIC prototype accelerating structures, second.

The pulse compressor, combined with an optimized phase program which drives the fast analogue phase shifter, can double the power delivered by the klystron.

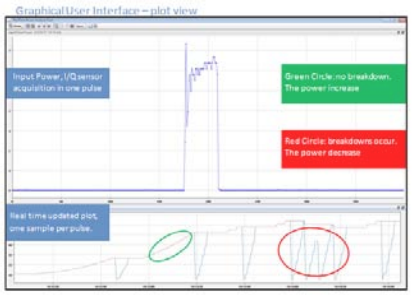




RF measurements calibration:
Cable calibration has been performed via a sophisticated method based on the Time Domain Reflectometry (TDR), while the characterization of diodes and I/Q demodulators has been achieved using a dedicated test stand, remotely controlled by a PC.

Some word about the software:
It is composed by two separate programs which have different objectives:
- handling acquisitions and controlling the hardware;
- giving feedback to the user, plotting chars or providing significant values.

The first is performed by the conditioning algorithm, which has to be fast: it is written in C++, which is used for the FESA (Front-End Software Architecture) as well. This part of software runs in the same crate where the acquisition cards are installed, in order to minimize the network delays.
The second is realized by a GUI (graphical user interface): it is written in JAVA and runs on a Linux PC.



Protecting the equipment during conditioning:
During the conditioning of the klystron and the waveguide network connected to it, breakdowns and out-gassing can occur in both, therefore stopping the RF drive input is required. For this reason, an interlock on the high power RF signals has to be put in place. This system consists of a high power directional coupler with -50dB coupling in the waveguide path right after the klystron, waveguide to coaxial transitions, attenuators and diodes with preamplifiers. Two failure modes exist which have to be captured within two consecutive RF pulses: first, if the reflected power exceeds a VSWR of 1.15, indicating a breakdown in the waveguide network; second, if the forward pulse contains less energy than expected which indicates a breakdown inside the klystron. The first failure is captured by a comparator on the diode signal which is gated to eliminate influence of noise created by the HV modulator. The second failure is handled by the mask test option of an oscilloscope, triggering an inhibit signal in the case of failure. An increase in power level therefore requires a new test mask each time, thus an FPGA based option is under development which will trigger an inhibit, if the most recent waveform deviates by a given percentage from the average of a programmable number previous pulses.

Conclusions and outlooks:
The LLRF allowed us to start-up the power test stand successfully. The next step is the improvement of the S/N ratio of the forward power measurement. This will guarantee a more reliable intervention of the interlock, also during the beginning of the conditioning, where demodulated signals are weak, but the power is already enough to damage the equipment.

Many thanks to:
We wish to thank Jean Mourier for having given the guidelines of this development, before retiring; Thierry Wiszniowski for his precious collaboration and flexibility during the installation; Jean-Luis "le Maître" Capy for having shown that electronics is sometimes more art than technique and Daniel W. Ventura for having reviewed the English.