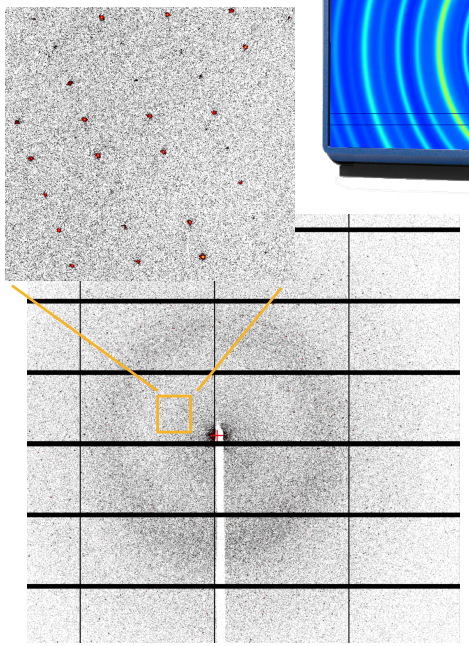
MAX IV activities
LEAPS-Innov WP7: Data reduction and compression

Zdenek Matej, May 2022

MAX IV synchrotron lab

Scattering detector data

Credit: Dectris



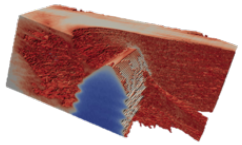
Installing
User Operation
Commissioning

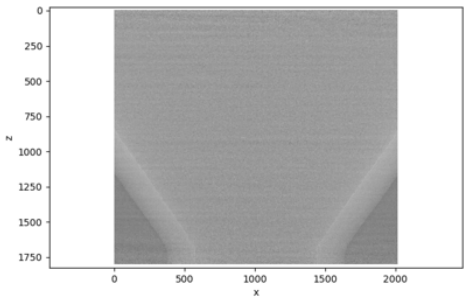
8 beamlines with high data rate hybrid pixel detectors

MAX IV synchrotron lab

Full-field imaging data

Credit: Hamamatsu





Installing
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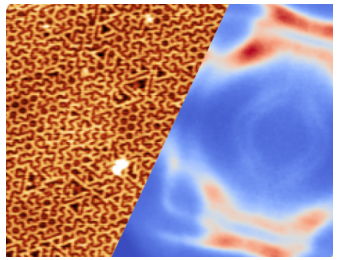
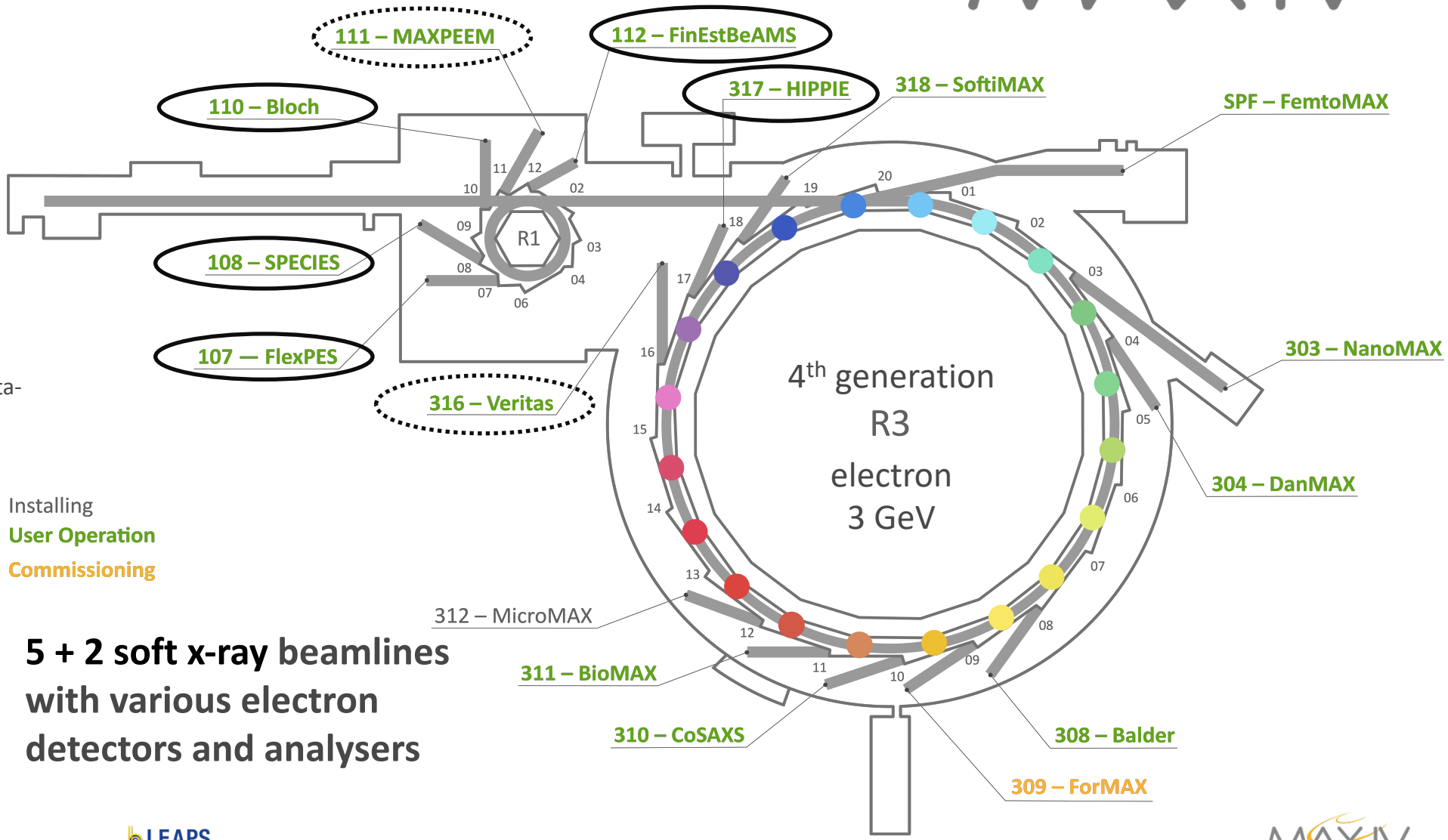
2 + 3 beamlines with high data rate imaging (CMOS) cameras

MAX IV synchrotron lab

Electron analysers& detectors

Credit: Scienta-Omicron





Installing
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5 + 2 soft x-ray beamlines with various electron detectors and analysers

MAX IV participants

Clemens – background in physics and XFEL; detectors. And pipelines for hard X-ray scattering beamlines

Michele –background in detectors at XFELs, expertise in CMOS cameras

Samuel – (former) student

Isak – junior member, machine learning & AI

Soft X-ray contact – new hire, background in physics and high perforce computing

Paul – background in particle physics and detectors. Deployment and control of detectors.

Zdenek – x-ray diffraction and scattering, imaging, scientific sw for FPGAs

2y position (?) – compression, DaTaSTAMP project

Darren – coordination and organization

Activities

in brief

- hybrid-pixel scattering detectors
  - covered by bslz4
  - from beginning HDF5
  - DAQ systems evolving from filewriters, Lima[1], ZMQ-receivers, k8s infrastructure
  - on-the-fly data processing: simple TOT to energy conversions etc.
  - special FPGA based DAQ for JungFRAU – project from PSI
  - prototyping data reduction on FPGAs – AZINT
  - cpu-AZINT for scattering beamlines (by Clemens)
  - XPCS pipeline (Clemens)
- imaging (CMOS) cameras
- electron spectroscopy detectors
- decompression on hardware compute accelerators

Activities

in brief

- hybrid-pixel scattering detectors
- imaging (CMOS) cameras
  - no compression solution in place (?) for non-full-field imaging techniques (~ detectors at 4 beamlines)
  - 2 beamlines (0.75b full-field tomography)
    - coming this summer/autumn
    - data reduction: requirements for on the fly tomography reconstructions (talk by Christian (PSI))
    - interest in general compression
- electron spectroscopy detectors
- decompression on hardware compute accelerators

Activities

in brief

- hybrid-pixel scattering detectors
- imaging (CMOS) cameras
- electron spectroscopy detectors
  - HDF5-project for Scienta detectors
  - new contact in Scientific sw
- decompression on hardware compute accelerators

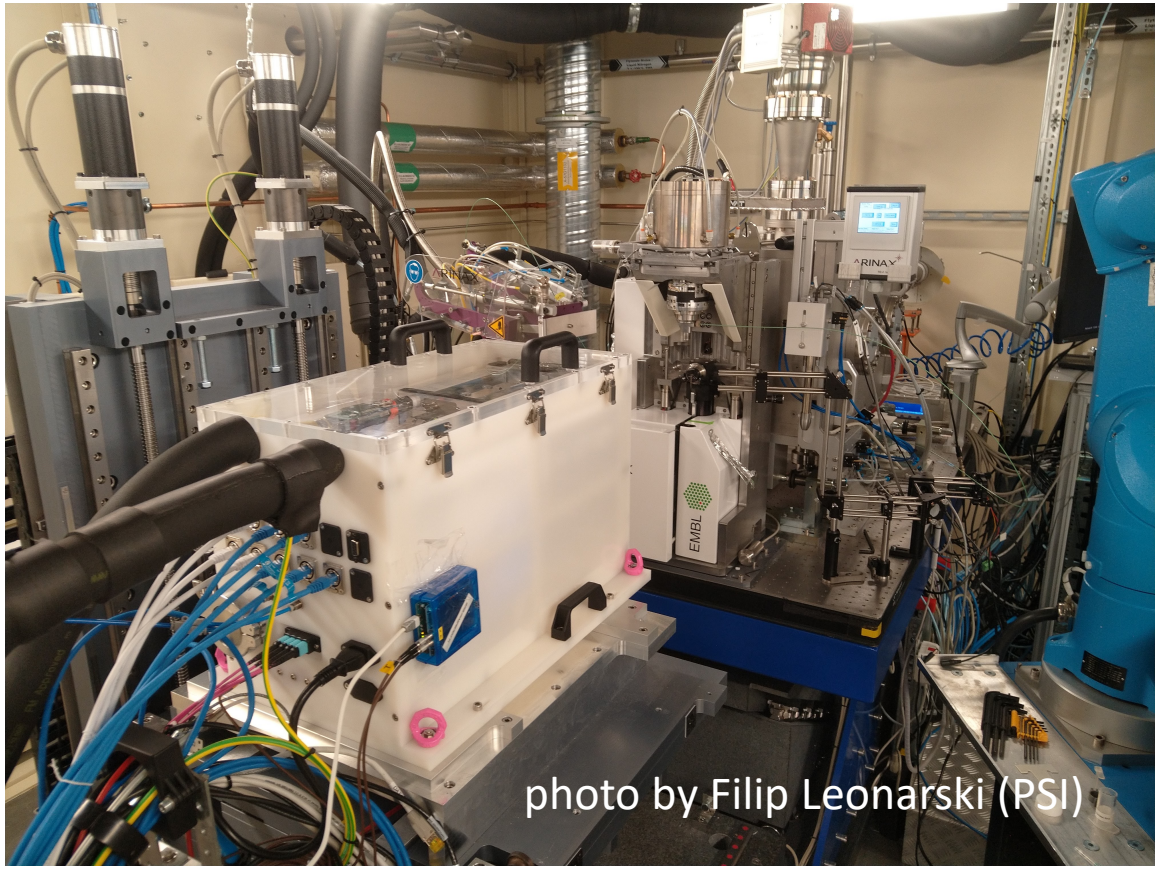
Activities

in brief

- hybrid-pixel scattering detectors
- imaging (CMOS) cameras
- electron spectroscopy detectors
- decompression on hardware compute accelerators
  - on GPUs/lz4: Samuel was trying to follow the development at ESRF
  - on FPGAs/lz4: investigation of possibilities

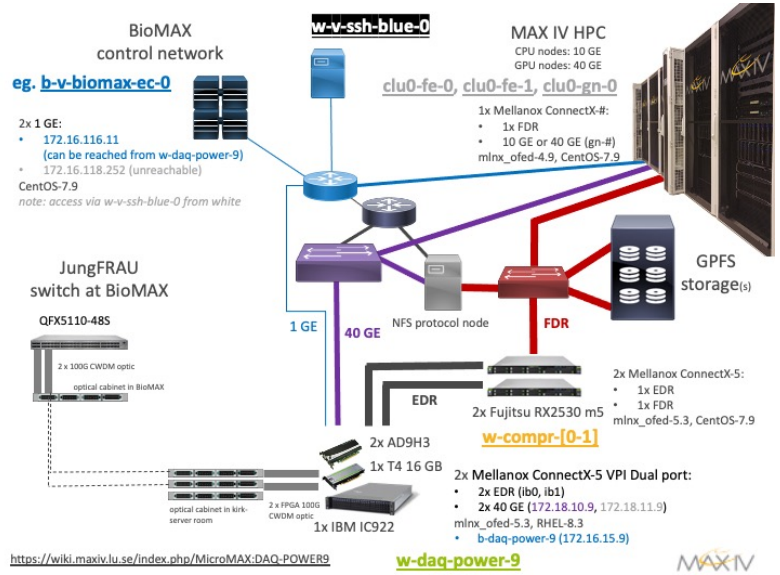
Jungfraujoch (PSI) at MAX IV

BioMAX beamline



4 Mpix at 2kHz

- FPGA & GPU & CPU data processing
- bs on FPGA and lz4 at CPU



Data reduction on FPGAs

AZINT bincount – on Intel FPGAs with OpenCL

	385A	520N-MX	comment
size	medium	large	
FPGA	Aria 10 GX	Stratix 10 MX	Bittware / Nallatech
process	20 nm	14 nm	
memory	2xDDR3	2xHBM2	
QSPF	2x10/40 Gbs	4x100 Gbs	
framework	OpenCL	OpenCL	
processing pipelines	32	32	gitlab.com/MAXIV-SCISW/compute-fpgas/bincount
ALUTs utilization	**45%**	**40%**	
RAMs utilization	60%	25%	fp32 (fp64 possible), 8k bins
frequency / ideal (MHz)	**205** / 240	**360** / 480	
host-to-device bandwidth	4.7 GB/s	5.6 GB/s	x8 PCIe Gen3, can handle 4.5M x 500 Hz ✅
processing (virtual) pixel rate	**5.7 Gpix/s***	**8.9 Gpix/s**	allows pixel-splitting = 3 ✅

Credit: Bittware

*comparable to NVIDIA V100 (~ 6 Gpix/s, 12 nm process)

Activities

summary/interest

- hybrid-pixel scattering detectors
  - quality of results of AZINT pipelines
  - XPCS pipelines
- decompression on hardware compute accelerators
  - lz4 on GPUs and FPGAs
- imaging (CMOS) cameras
  - data reduction: on the fly tomography reconstructions