The x3timer

Development of a new timing AMC hardware for PETRA IV

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Hamburg 07.09.2022

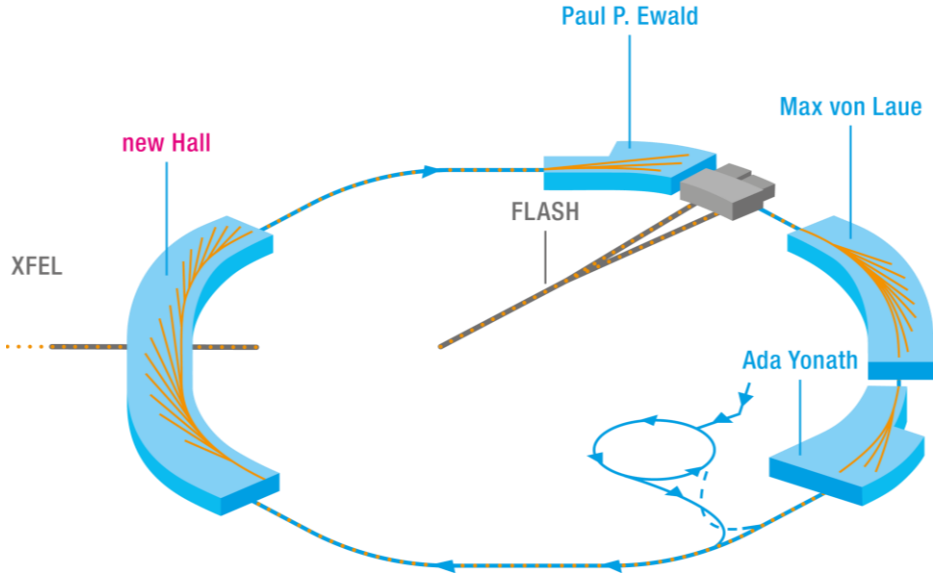
HELMHOLTZ

ARD-ST3 LLRF Satellite Workshop

DESY.

Accelerator facilities at DESY HH

Facility	Timing system
• FLASH	x2timer (e.g. upgrade to x3timer)
• European XFEL	
• PETRA III	VME-based timing
• PETRA IV (upcoming)	x3timer



X3timer development for PETRA IV

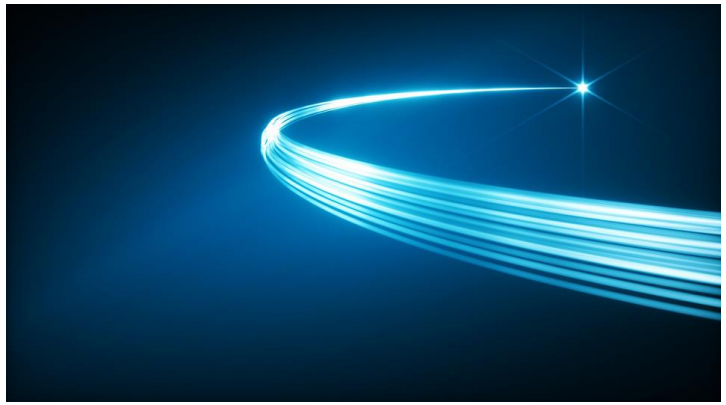
- **MicroTCA.4 components will replace existing PETRA III hardware** for controls and diagnostics
- **Make use of experience from well-established Timing System concepts** as utilized at the FLASH and European XFEL facility
- **Keep the design flexible** to enhance functionality during life-cycle of PETRA IV

PETRA IV overview

- 4th Generation Light source
- 6 GeV Storage Ring
- Circumference 2304 m
- low emittance: hor. 10-30 pm rad, vert. < 10 pm rad
- 500 MHz RF
- timing / brightness mode: 80 / 1600 Bunches
- also new Booster Synchrotron DESY IV
- 30 Beamlines in 4 Experimental Halls

Challenges for the Timing system

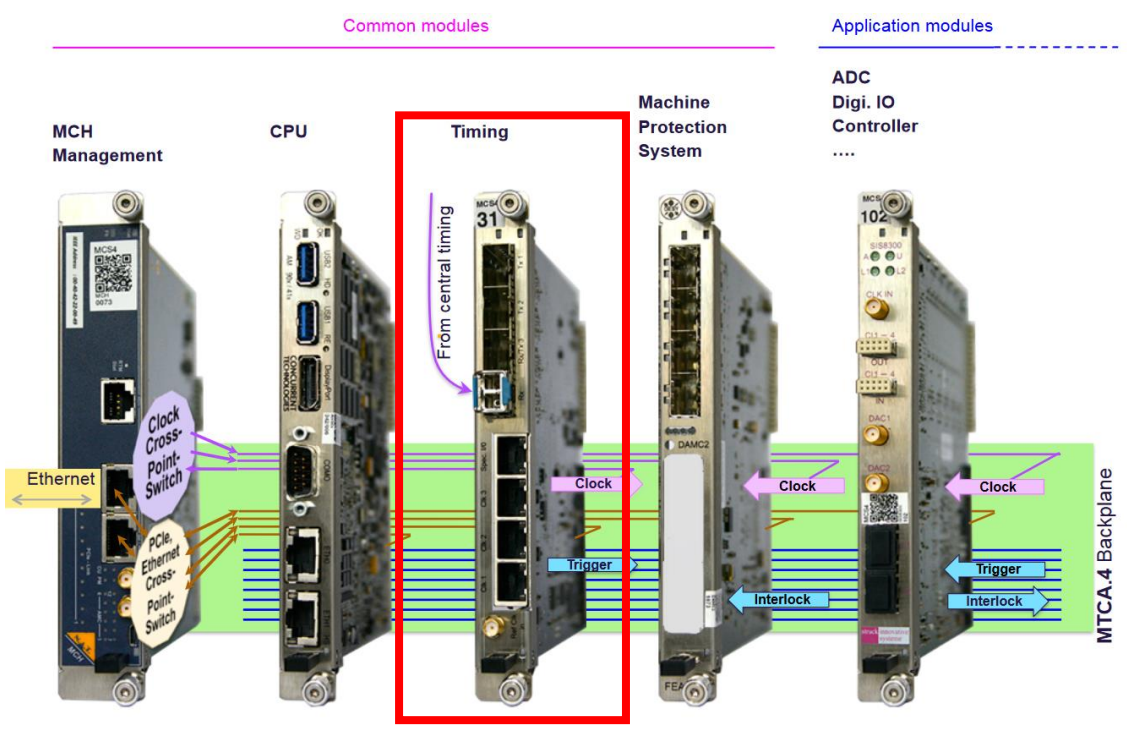
- EuXFEL
  - 3.4Km total length
  - 2Km accelerator section with synchronized LLRF control
  - RF stability in fs regime required
- PETRA III
  - 2.3 Km circumference
  - Separate timing systems for pre-accelerator and storage ring
    - Needs to be synchronised in normal operation
    - Option to run independently during dispersion measure
  - Each timing fault can result in a dump of all bunches
- PETRA IV
  - Increased timing accuracy required (compared to PETRA III)
    - Injection kickers
    - Multibunch-Feedback
    - Experiments
  - Additional 1.5GHz RF system



The X2Timer

Well experienced MTCA based Timing Hardware

- Developed together with DESY
- Can act as Transmitter and Receiver
- Provide continuous timing signals & trigger events
  - Internal on Backplane port 17-20 (MLVDS)
  - TCLK A/B
  - external on Front panel (LVDS)
  - TTL (LEMO) Trigger via RTM or converter box
- Provide bunch meta-information
- Dedicated fiber network with optional drift compensation
- Successful in operation at FLASH and European XFEL

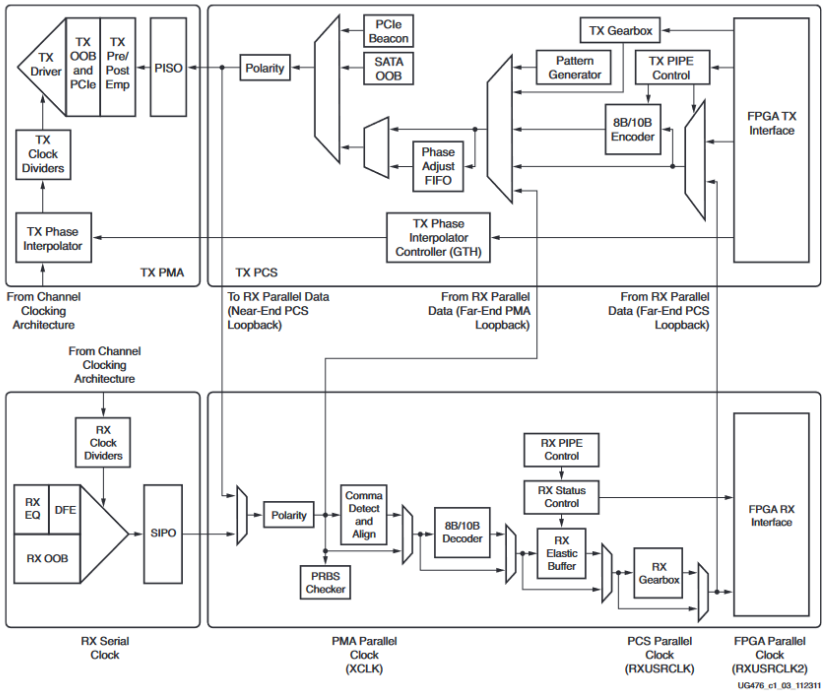


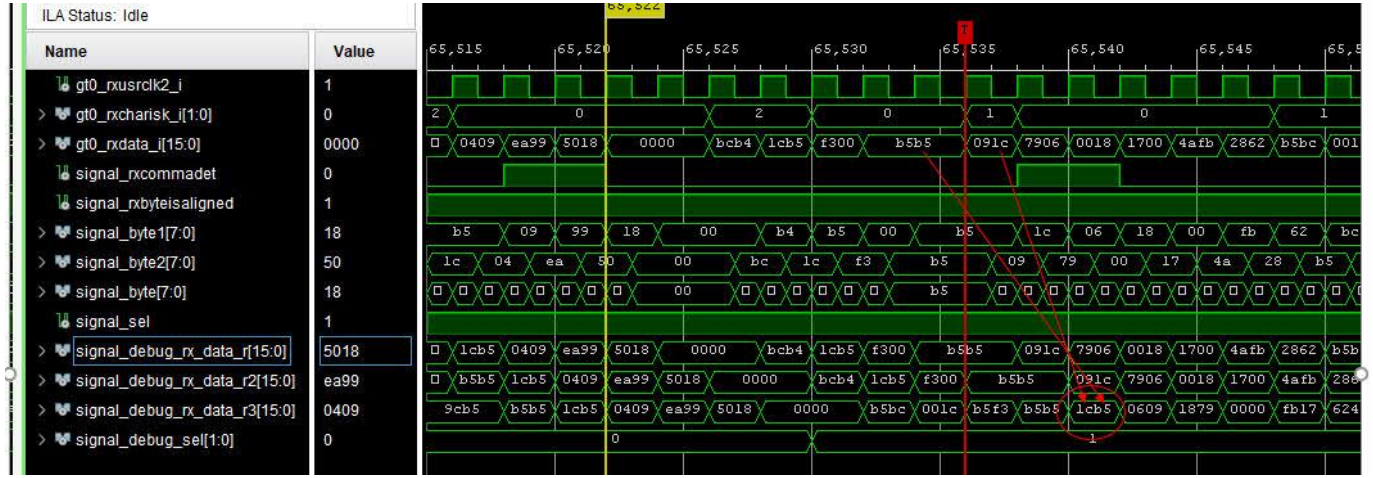
Design changes needed for PETRA IV

- Many components of the X2Timer are going end of life
- Output jitter can be improved
- CPU core for
  - real-time calculation of advance delays
  - Configuration and monitoring of peripherals
- Bunch-Metainformation differ from XFEL
- Front panel design?
- RTM interface design by class recommendation

The X2Timer – Data transmission

- Fast (multi gigabit) serial transceiver
- Receiver and Transmitter part
- Data rate derived from RF-Input
- Clock data recovery (CDR) in the receivers
- Encoding 8b10b





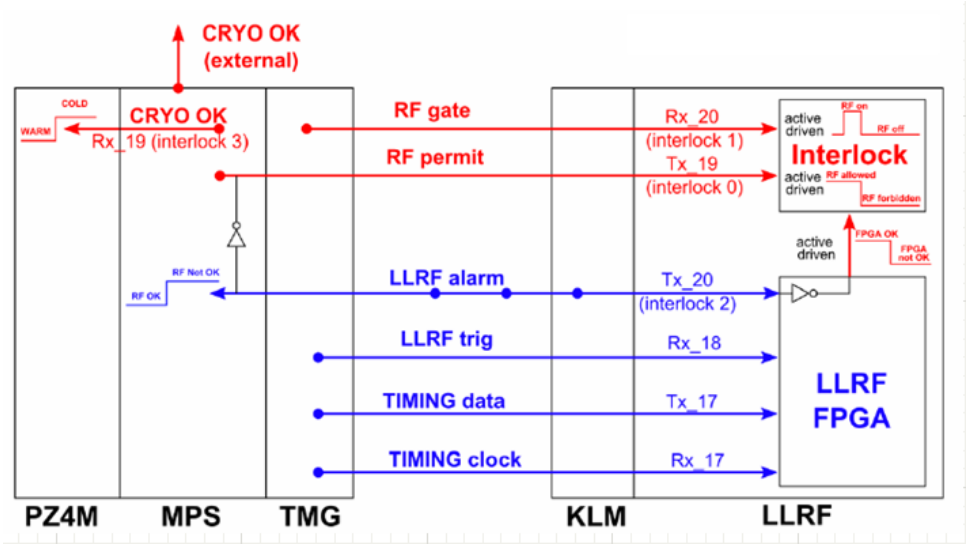
- 8b10b protocol uses comma characters for
  - Datastream alignment
  - Synchronisation
  - Start of data transmission
  - Probe for link delay measurement

Special comma characters used in the protocol

Character	Name	Function	8b Data	10b Data	
D21.5	FILL	Idle filler	0xB5	101010 1010	101010 1010
K28.0	START	Start of a message packet	0x1C	001111 0100	110000 1011
K28.1	SYNC	Synchronisation	0x3C	001111 1001	110000 0110
K28.4	PROBE	Link delay measurement	0x9C	001111 0010	110000 1101
K28.5	ALIGN	GTP comma alignment	0xBC	001111 1010	110000 0101
K28.7	RES	Reserved	0xFC	001111 1000	110000 0111

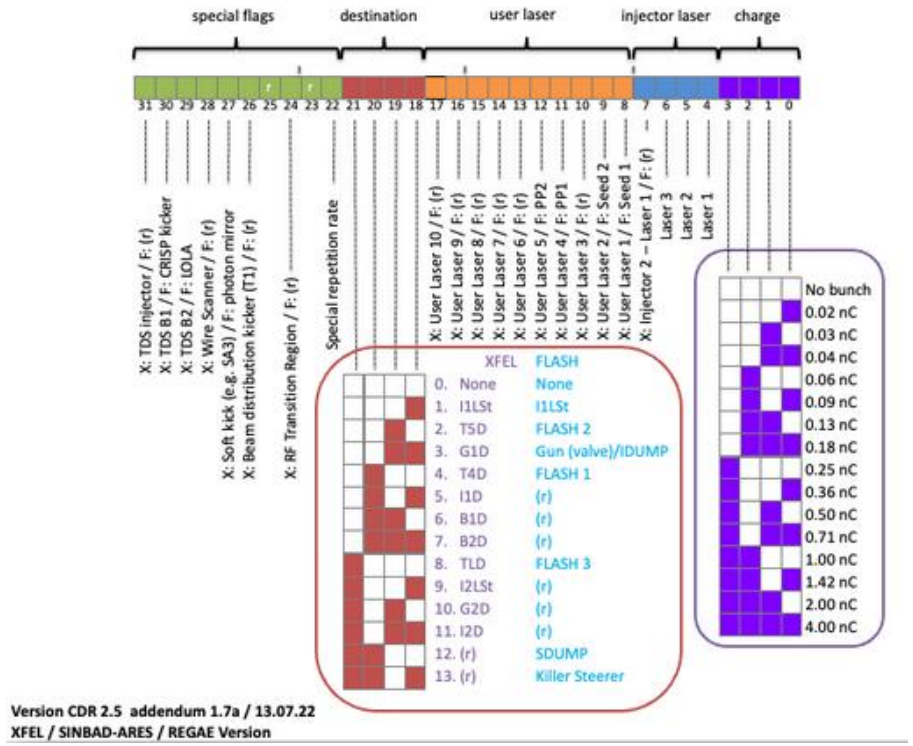
Timing information used in LLRF

- AMC backplane triggers for ADC and piezo - 10 Hz rep rate (synched from 1.3 GHz from main oscillator)
- AMC RF gate - optical synchronization between x2timer Transmitter and x2timer receiver
- Bunch pattern information for beam loading compensation
- Software interrupt for all DOOCS servers

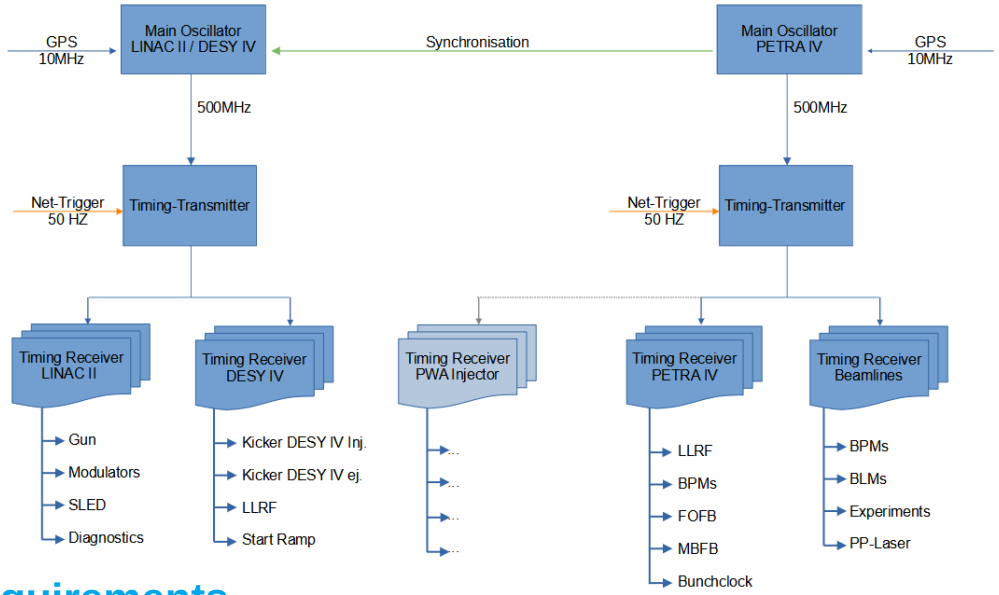


<START><LENGTH><COMMAND><DATA bytes><CRC>

Description	Command	Length	Frequency
Macro Pulse Number	4	9	
Absolute Time	6	9	
Delayed Event	2	6	
Immediate Event	10	2	
Word	3	6	
Table	5	3-131	
Shot-ID	8	2	
Set Flag	16	5	
Bunch pattern changed	9	2	
ID Request	12	1	
ID Response	13	129	

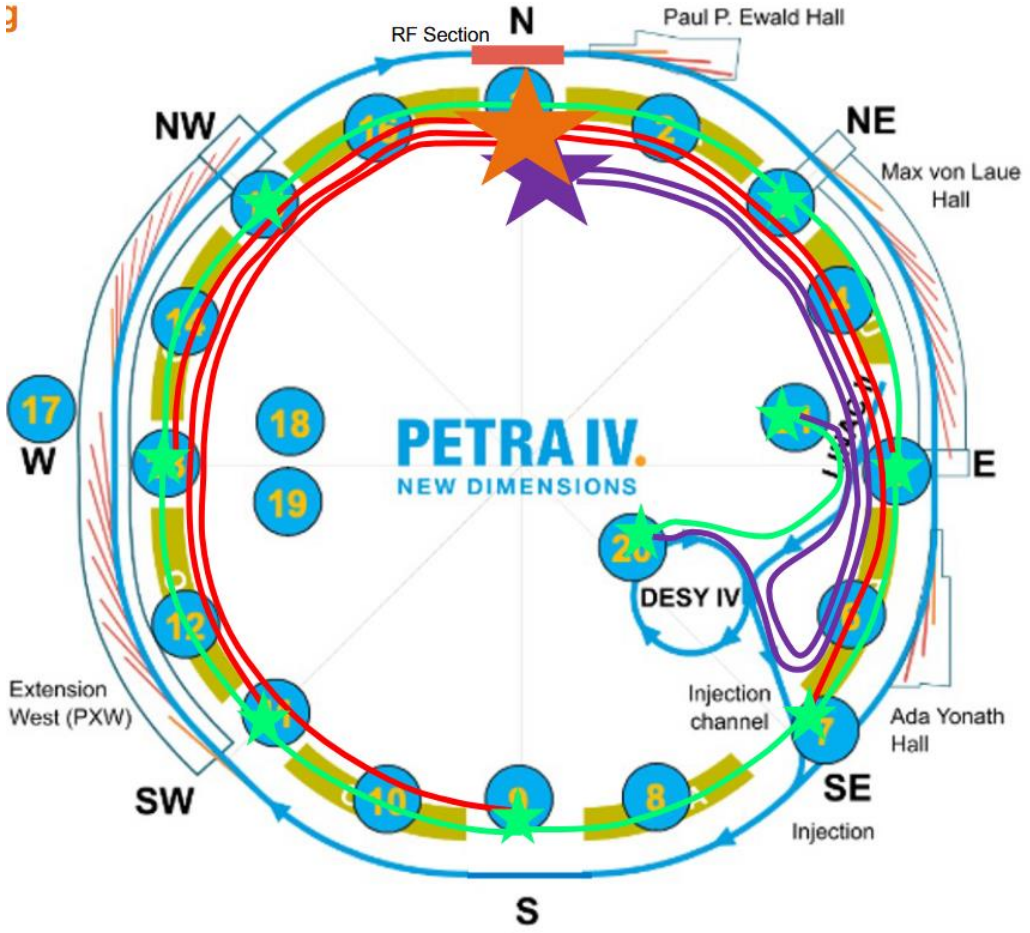


Timing System Design for PETRA IV



Key Requirements

- Distributing a continuous RF reference signal
- Provide low jitter clocks for ADC sampling
- Provide continuous timing signals & trigger events
- Provide beam-synchronous data as:
  - Timestamp / revolution counter
  - Beam mode / bunch pattern
  - Table of last measured bunch currents
- Common hardware for timing transmitter and receiver
- Dedicated fiber network with drift compensation
- Common timing system for accelerator and beamlines



Jitter stability test setup

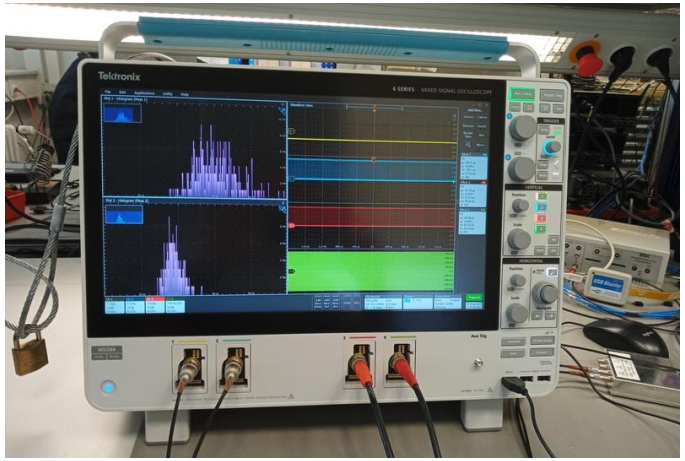
Test Setup

- RF-Generator (R&S SMA100A)
  - 10MHz GPS stabilized
- MTCA 7-Slot Crate
  - MCH
  - CPU
  - 2 * X2Timer (Transmitter, Receiver)
- Jitter cleaner Eval-Board (LMK04832)
- measurement adapters
  - RJ45->SMA
  - SFP-> SMA

Measurement equipment

Tektronix MSO64B

- Sample rate 50GS/s
- Bandwidth 8GHz
- vertical resolution 12 Bit



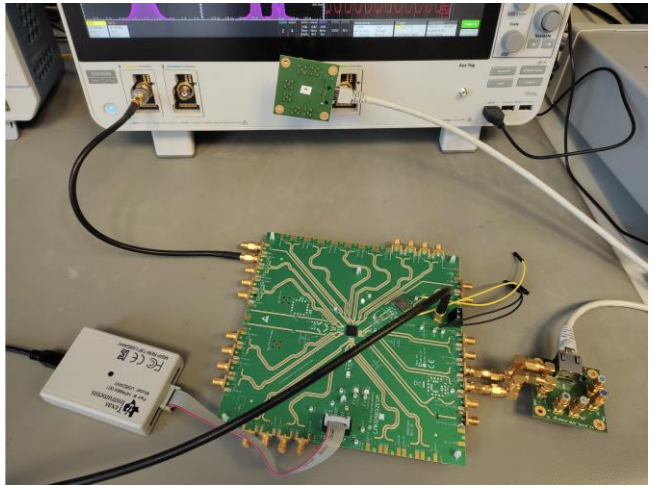
Goals

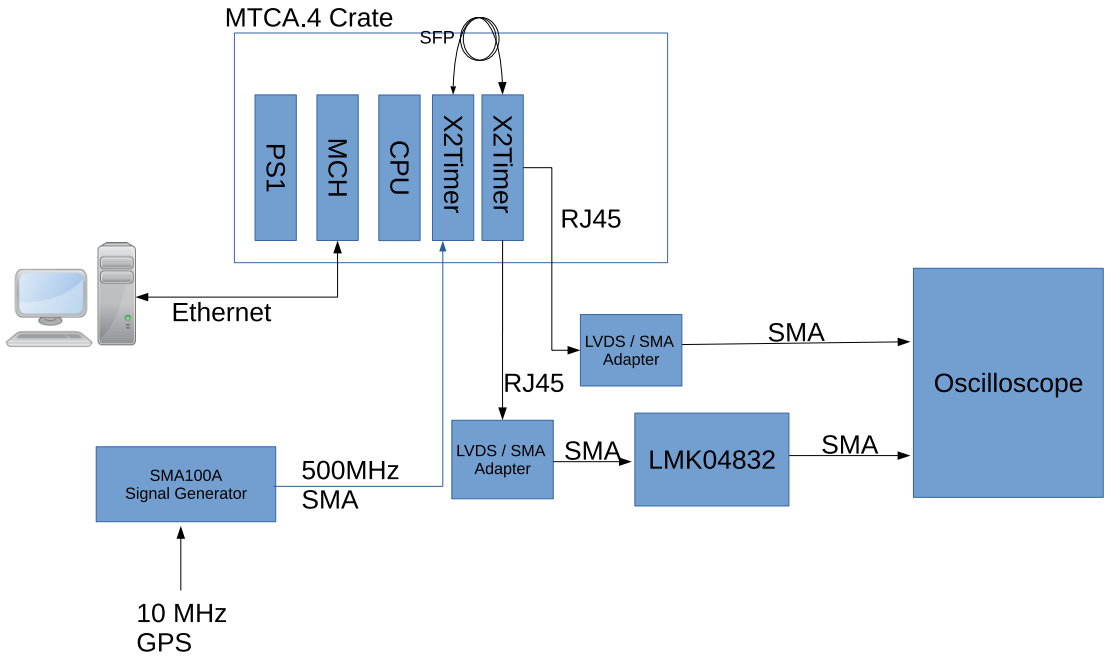
- Test concepts for the new timing card
- Qualify components for their usability
- Create test platforms for firmware and software development

Clock jitter cleanup

Dual loop PLL Jitter cleaner

- Created noisy clock by sending through 2 X2timers
- Feed noisy Clock to the LMK04832 jitter cleaner board
- Jitter can differentiated between
  - Random Jitter RJ
  - Deterministic Jitter DJ
  - Periodic Jitter PJ





Option	Description	Jitter
No jitter cleaner	Clock used direct from CDR (like X2Timer)	10-30ps
Single loop	Use LMK04832 and internal VCO loop only	1-3ps
Dual loop	Use custom VCXO and internal VCXO	< 1ps

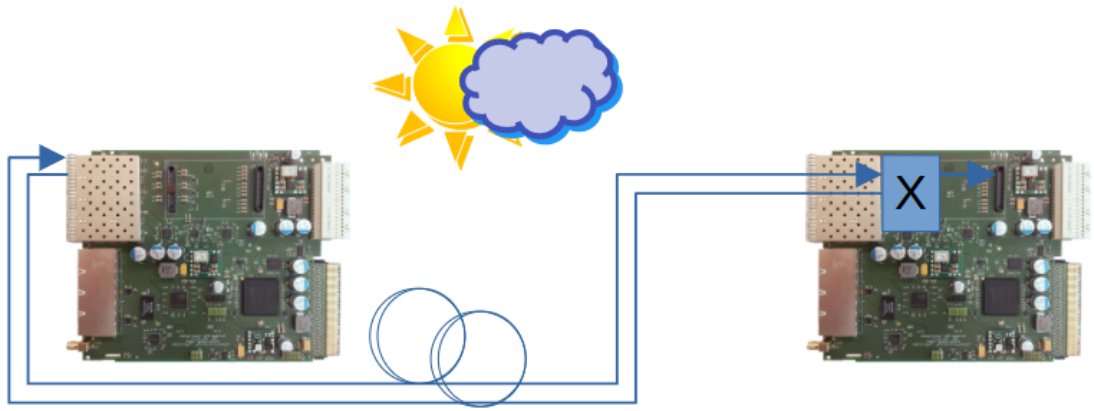
Next steps

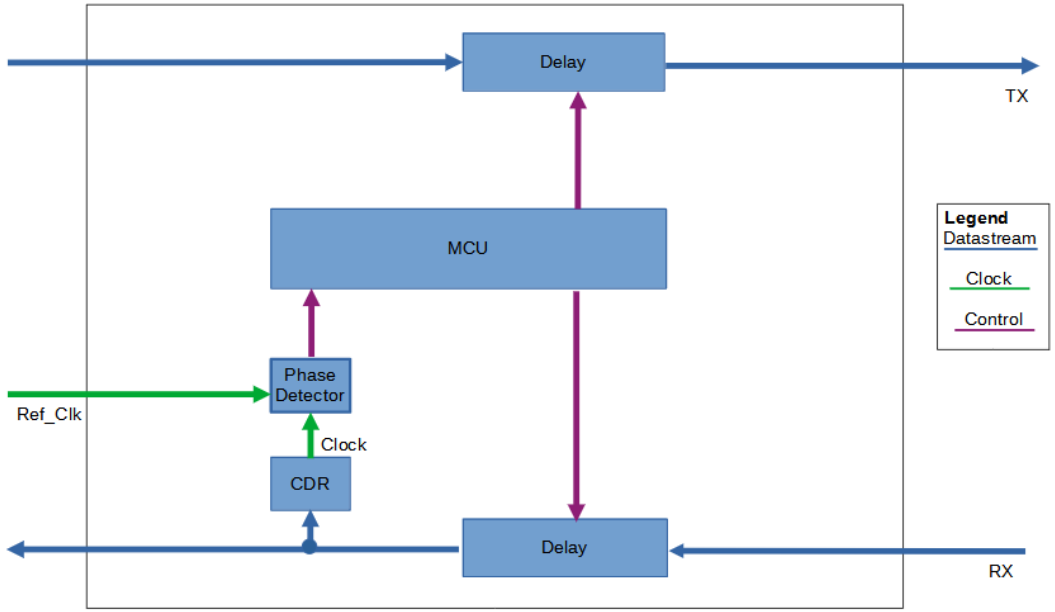
- Compare Jitter of different RF frequencies
- Tests with longer optical cable
- Parallel test on phase noise analyzer

Drift compensation

All transmitting SFP connectors shall have an adaptive drift compensation which:

- Detects phase differences between Ref_CLK and recovered clock (looped back on receiver)
- Sets delays to keep the phase relation between TX and RX path
- Is able to read back the phase difference between direct and delayed path (for RX and TX)
- actively monitors the phase and adapts the delay by an module internal MCU
- Has the option to be bypassed
- Configurable from the control system through the FPGA
- For cost optimization separate module or equip option





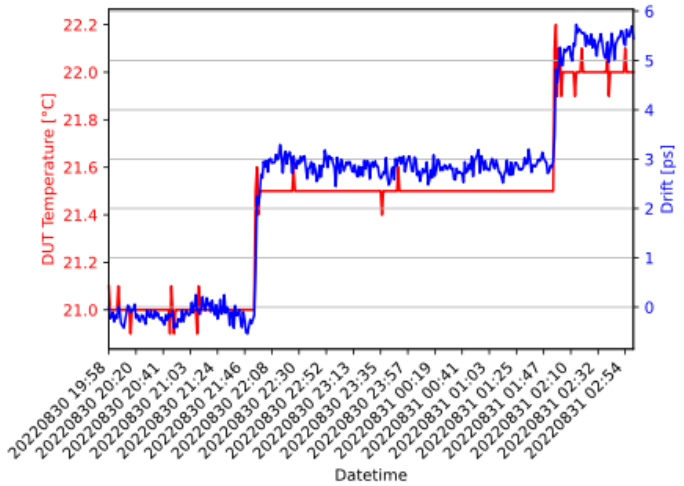
Drift stability and compensation tests

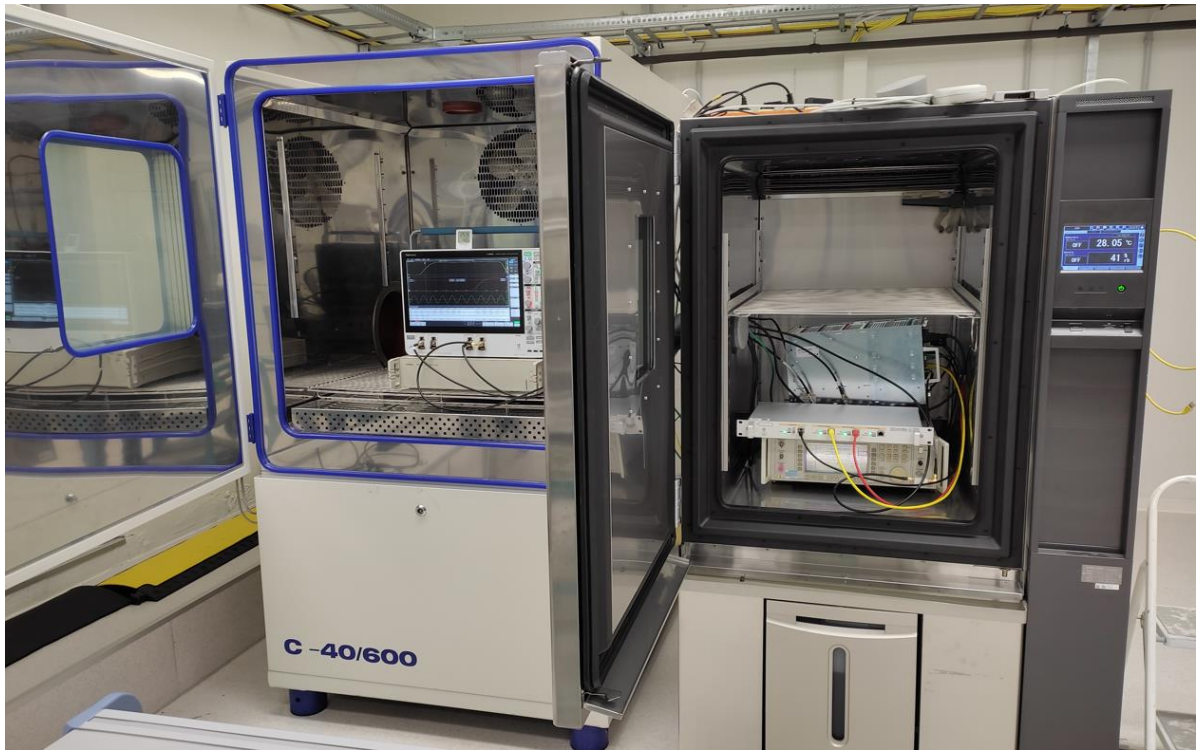
Test Setup

- 2 climate chambers
- MTCA 7-Slot Crate
  - 2 * X2Timer (Transmitter, Receiver)
- RF-Source
- Rubidium standard reference

Goals

- Measure drift of the x2timer
- Calculate termperature coefficient
- Test drift compensation board





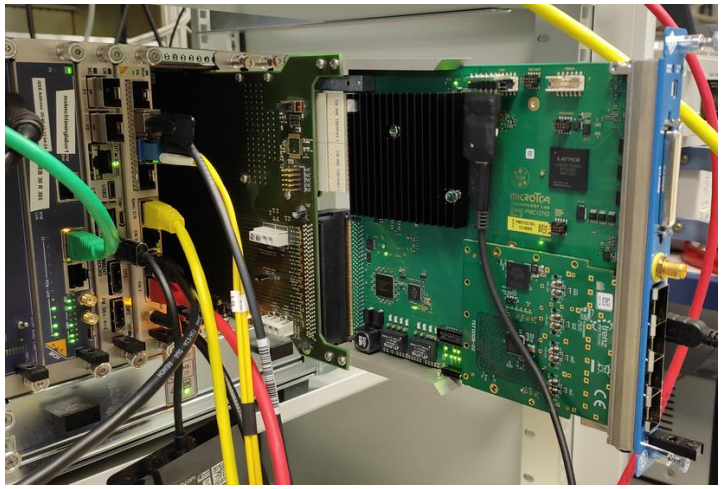
First results

- Crate fan activity has influence on internal drift
- When constant airflow
  - Internal temperature correlates to chamber temperature
  - Drift ~5ps/°C (without compensation)

next tests

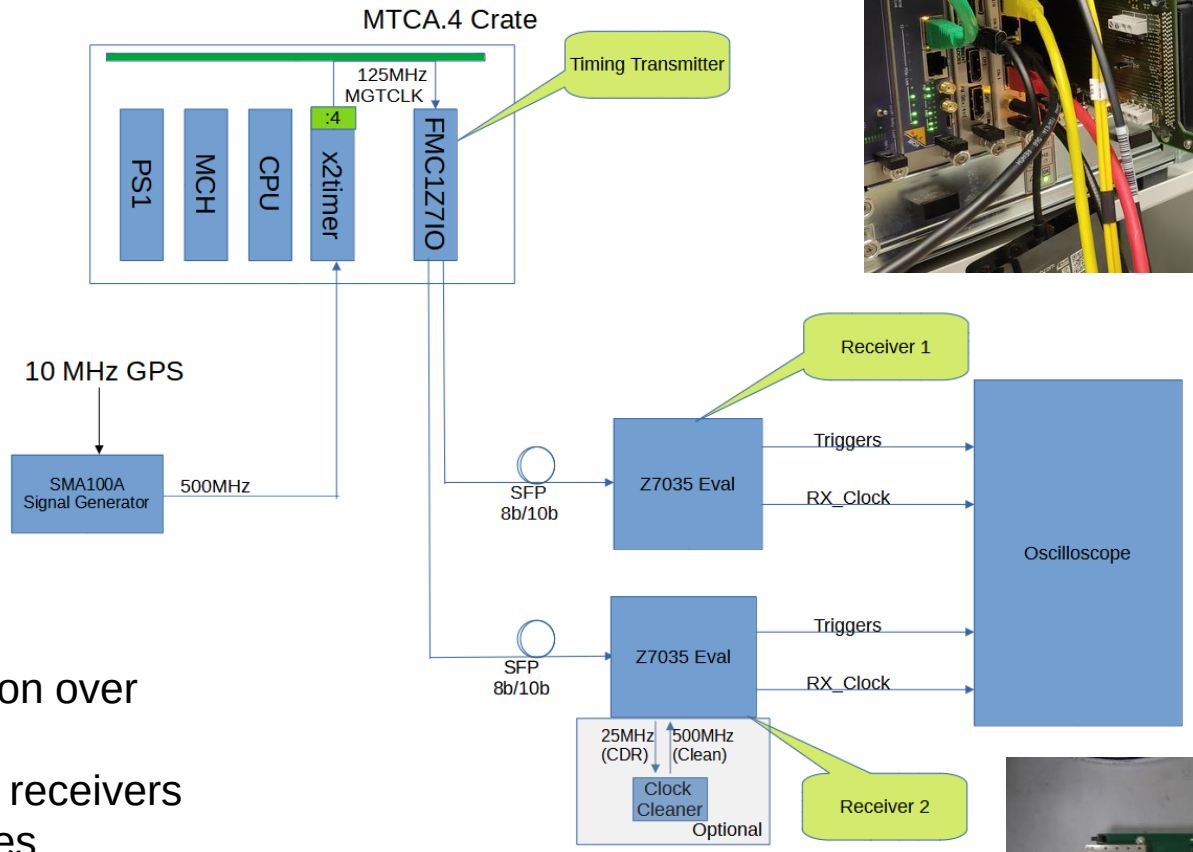
- Different Cable length (up to 1Km)
- Sweping cable temperature
- Data transmission over single fiber
  - Two wavelength 1310/1490nm
- Influence of RF frequency
  - 1.3GHz/500MHz, …

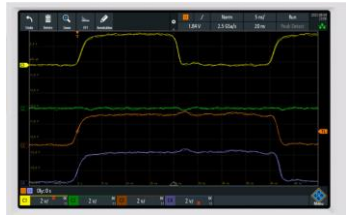
Timing distribution - lab setup



Distributed Test setup

- MTCA-Crate (Transmitter)
  - DAMC-FMC1Z7IO Board
    - FMC-Card with SFP-Interfaces
  - x2timer for RF to TCLK bypass
- 2 Zynq 7035 Evalboards (Receiver)

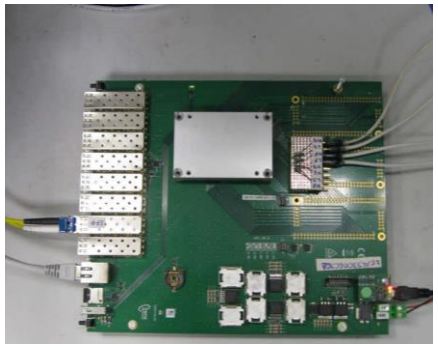




Integration into DAMC-FMC1Z7IO

(by DESY MTCA Technology Lab)

- Firmware integration into Xilinx Zynq SoC
- Test transmitter/receiver data communication over SFP fiber link
- Test trigger and clock stability with multiple receivers
- Test-Platform for MTCA (software) interfaces
- Clock cleaner can optionally be integrated to the receivers for more accurate clock and trigger output



Interfaces of the X3Timer

Front Panel

- (Q)SFP – for timing signal distribution
- RF-Input/Output (SMA)
- LVDS Output (RJ45)
- TTL Output (LEMO)
- Synchronous RS232 Output
- LVDS Input (Sync signal, Trigger)
- USB (Debug)

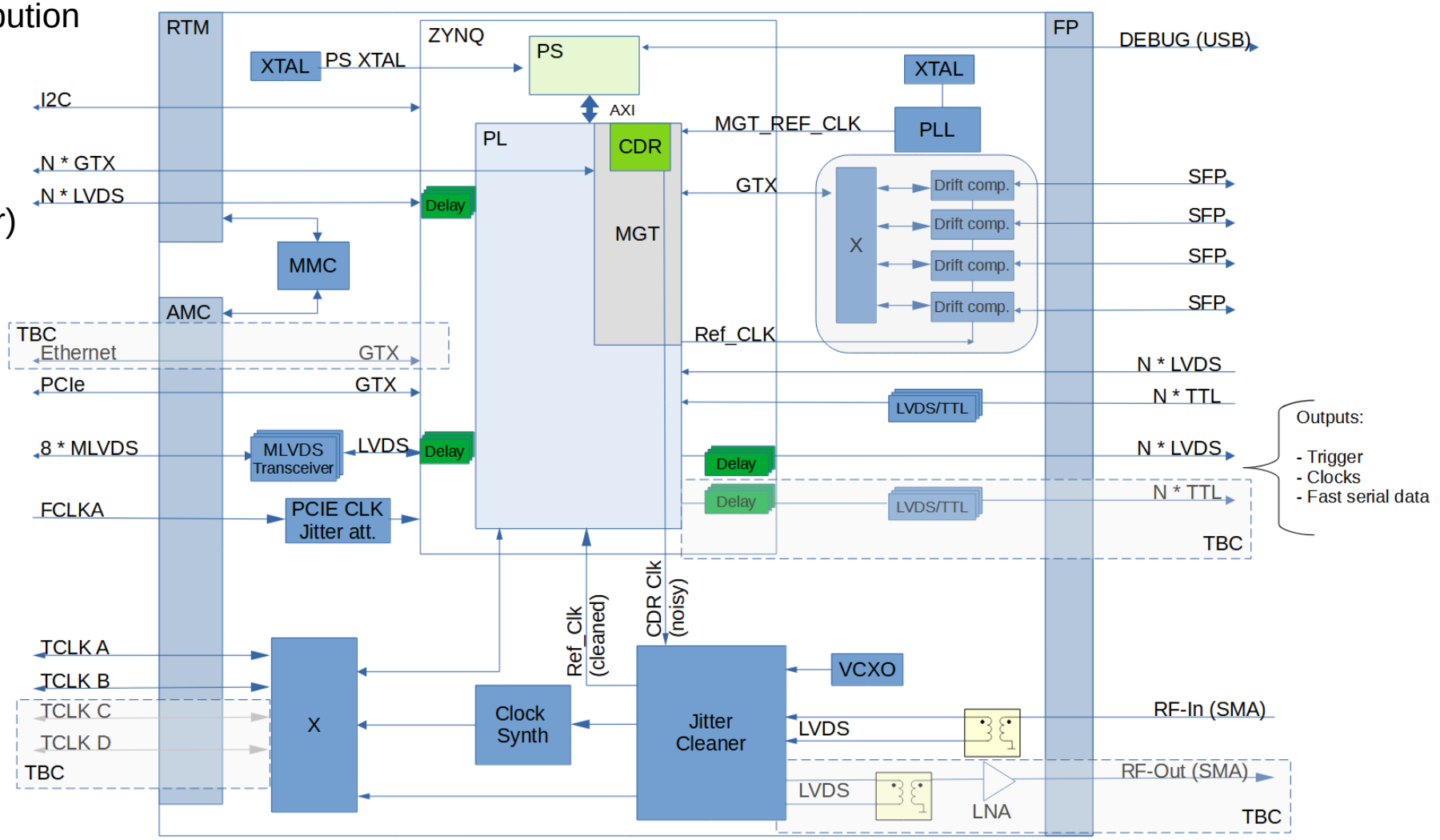
AMC - Backplane

- PCIe
  - Control
  - Software Trigger
- Ethernet
- TCLK A/B (C/D tbd.)
- Port 17-20 Trigger/Clock
- IPMI to MMC

RTM Zone 3

- MGT lanes
- LVDS Trigger / Clocks
- I2C to MMC
- I2C for configuration

Preliminary!



RTM modules

Zone 3 (RTM-Connector)

RTM Class D1.1 or above (depends on the amount of required High-Speed links)

Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft

http://mtca.desy.de

Class D1.0, D1.1, D1.2, D1.3, D1.4

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Digital signals in the user zone:
- Class D1.0: 48 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 38 LVDS I/O signals, 4 high-speed links
- Class D1.3: 28 LVDS I/O signals, 8 high-speed links
- Class D1.4: 8 LVDS I/O signals, 16 high-speed links

Digital signals with a fixed direction:
- 2 LVDS low phase noise clocks
- 1 LVDS timing output signal
- 3 LVDS outputs for user applications

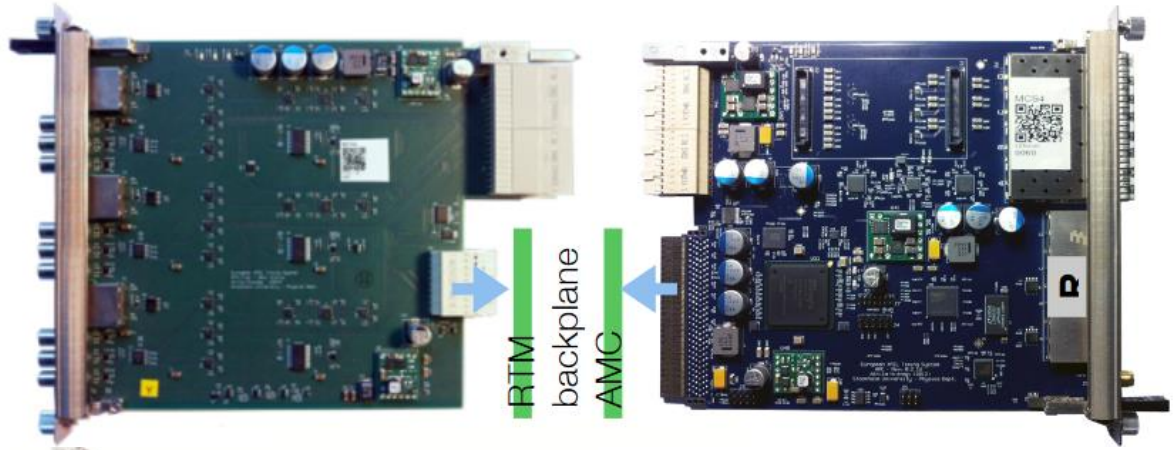
APPLICATIONS

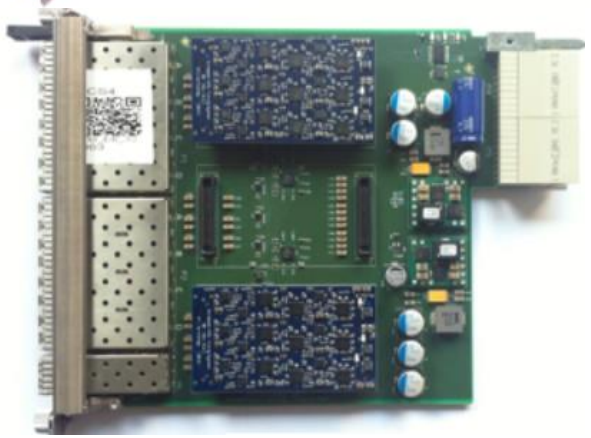
- AMC / µRTM board design in MTCA.4 standard
- High-speed data processing
- Multi-channel data-converters, sensor readout and output
- Digital signal conditioning boards

GENERAL DESCRIPTION

This Class D1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring digital signals over the Zone 3 connector. This digital class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The subclasses offers different numbers of digital input / outputs and high-speed communication links. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

https://techlab.desy.de/resources/zone_3_recommendation/index_eng.html





RTM types

- Rear panel interfaces
  - LEMO
  - LVDS
  - Optical
  - NIM?
- RF-Backplane interface
  - Clock distribution
- Functional
  - Programmable delay line
  - SFP Fanout module

Firmware framework & software interface

MSK firmware framework

- Generic framework for various (Xilinx) FPGAs
- Maintained by MSK firmware group
- Register maps for software interface
- Supports also ARM core interface for SoC devices

Application core / ChimeraTK software layer

- Middle layer to abstract hardware and control system
- Supports multiple controls systems
- Uses Xilinx xdma driver to access FPGA via PCIe
- Support to run on (Zynq) ARM cores in preparation
- Public available: https://github.com/ChimeraTK

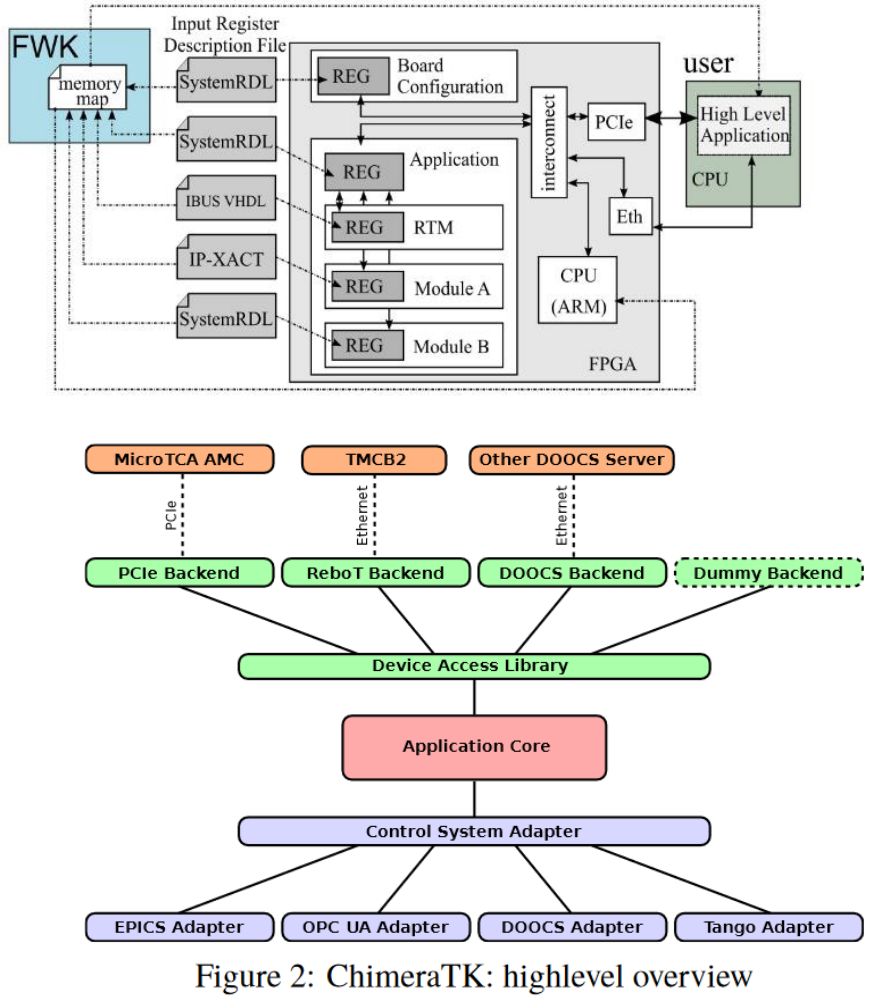
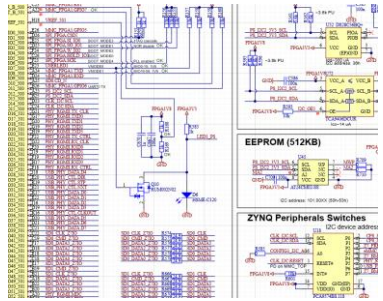
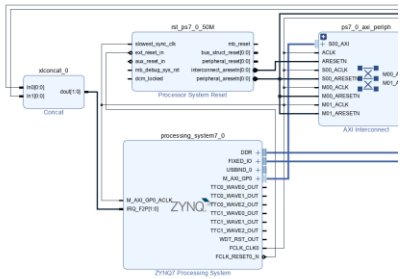


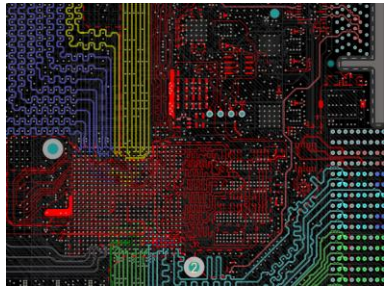
Figure 2: ChimeraTK: highlevel overview

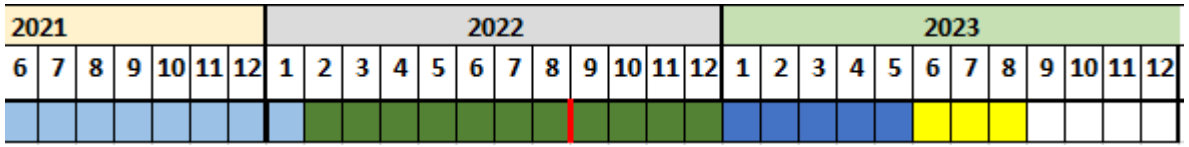
Roadmap

- Specify Requirements
- Derive MTCA.4 AMC and RTM architecture and interfaces from requirements
- Adapt existing AMC design for X3Timer demonstrator
- Hardware development and production
- Firmware development
- Server and high level controls development









Symbol Legend:	
Specification	
Design	
Design/Production External	
Production	
Test	

Conclusion

- The x2timer is a well established timing system in the DESY FEL Facilities
- For PETRA IV we will top on this development
- Improvements in the x3timer
  - **Improvement of short term jitter** by using a clock cleaner in the receiver modules
  - **Better drift stability** by thermal optimization of the boards (e.g. full sized heat spreader) and definition of Crate cooling requirements
- New possible features due the Zynq SoC architecture
  - **Realtime processing** on ARM core (e.g. delays for PETRA filling pattern)
  - Possibility to implement **control servers on Zynq SoC** and run without MTCA CPU
  - More flexibility for configuring peripherals with I2C or SPI
- More flexibility by using a Software/Firmware framework
  - Interface for **many control systems**
  - **Modular firmware** for easy portability
- Chosen components with **long term availability**

Thank you for your attention!

Contact

DESY. Deutsches Elektronen-Synchrotron

www.desy.de

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