Some thoughs about CALICE+LUXE Acquisitions

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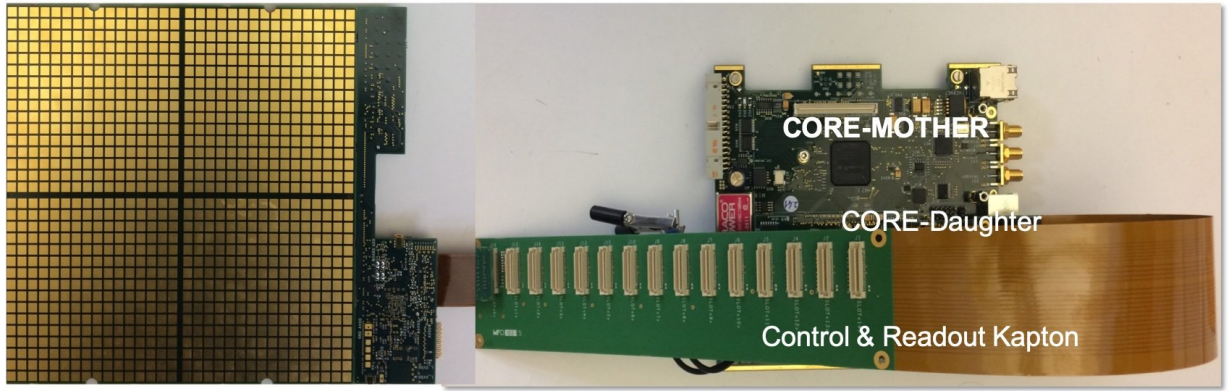
Compact DAQ readout

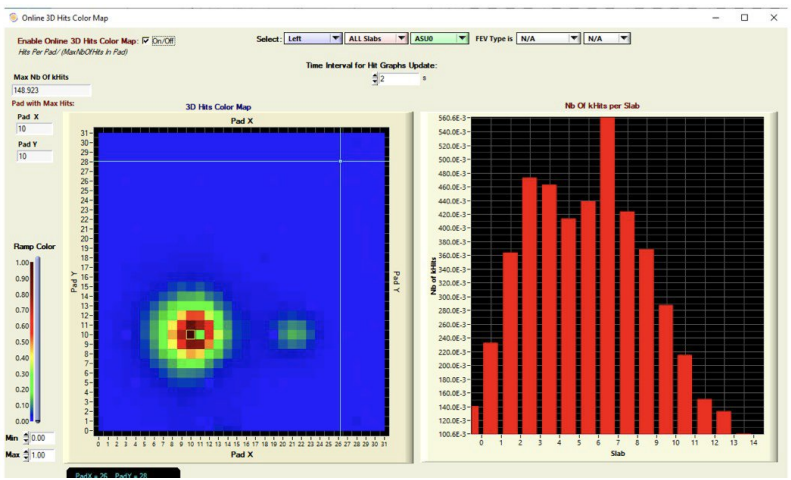
“Dead space free” granular calorimeters
➡ ~ 30 mm space ECAL–HCAL

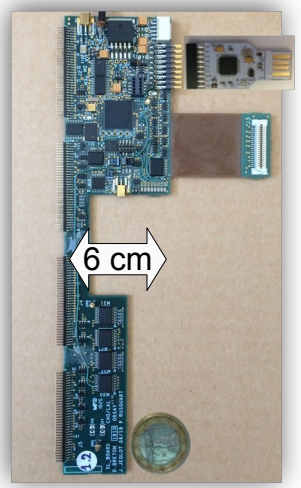
- Compact DAQ
- in use in BT since 2019

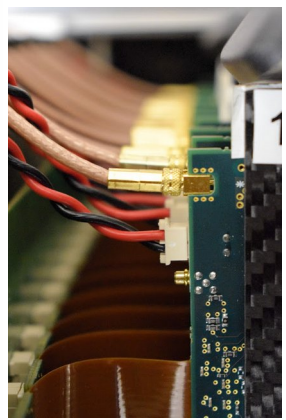
LabWindows + scriptings

- Full debug system
- ⬌ EUDAQ
  - Combined running









Requirements for DAQ at XFEL/LUXE set-up

Beams:

- **XFEL beam 10 Hz,** 1 bunch for LUXE
  - $1.6 \cdot 10^9$ e^-, $E_e \leq 17.5$ GeV
- Laser 1Hz

: 40–350 TW, 30 fs ➡ $1.5 \cdot 10^{20}$ W /cm³

CALICE Set-up:

- Number of layers ≥ 15 ?
  - 1× ASU (18×18 cm²) ?
  - 2 × ASU (18×54 cm²) ?
    - Excellent intermediate test of CALICE prototypes
    - Will require some additional ASIC production… (400/16 = 25 boards)

Composite Set-up ?

- CALICE + FCAL
  - Common Readout by EUDAQ
- Use only Half Boards (9×18 cm²) ?
  - Only ½ Wafers, or ½ Wafers and ASICs…
  - ⚠ **BUT makes reuse for CALICE difficult** ⚠

Running mode:

- Closed ➡ Pulsed operation (or not) ?
- Noise conditions…
- Charge / Mip density / cm² ?

LUXE

Physics:

- QED in High Fields:
  $e+n\gamma \rightarrow e\gamma$, $\gamma+n\gamma \rightarrow ee$
  - Schwinger's limit
- BSM: Axions Like Pseudo Scalar, …

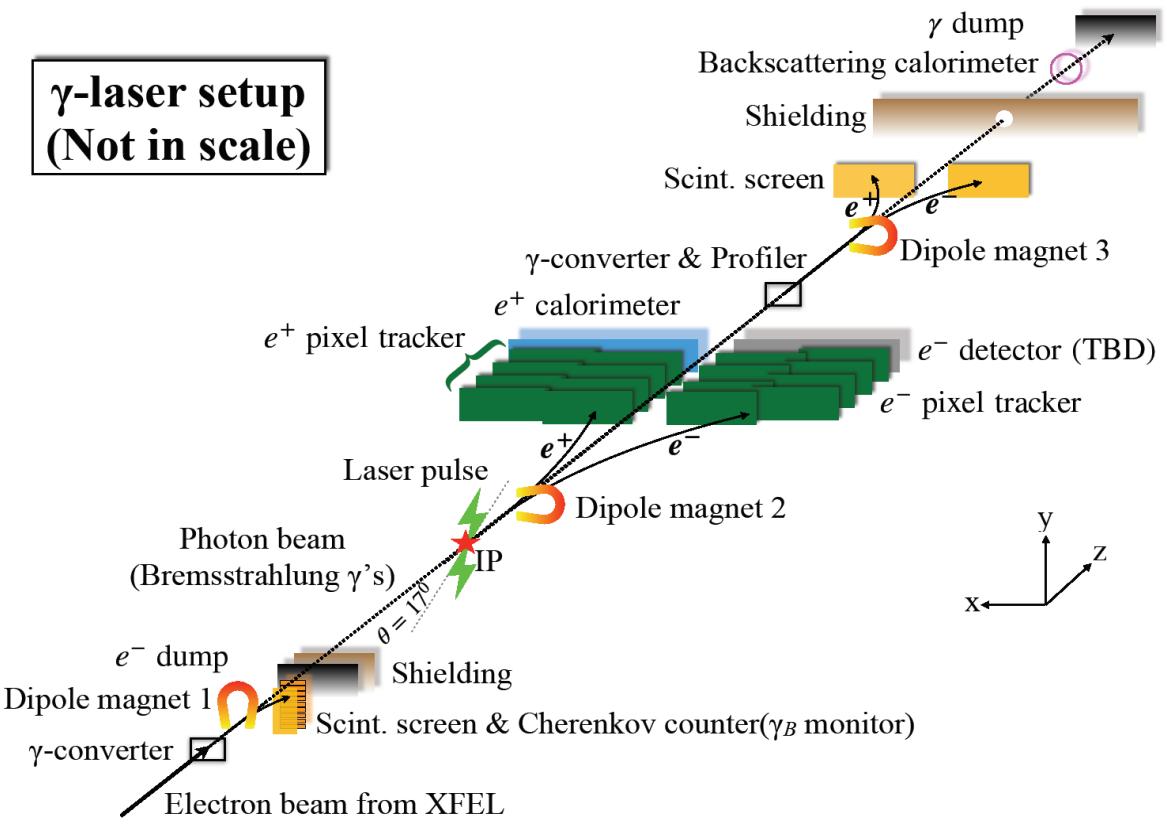
Beams:

- **XFEL beam 10 Hz,** $1.6\cdot10^9$ e^-, $E_e \leq 17.5$ GeV
- Laser : 40–350 TW, 30 fs, 1 Hz
  ➡ $1.5\cdot10^{20}$ W /cm³

ECAL:

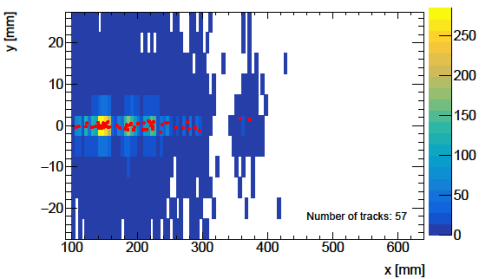
- 5×5 mm² cells, 20 X_0, 20 layers, 20 %/√E
- Si+W or GaAs+W ➡ FCAL and/or CALICE

γ-laser setup (Not in scale)



Overlap of showers

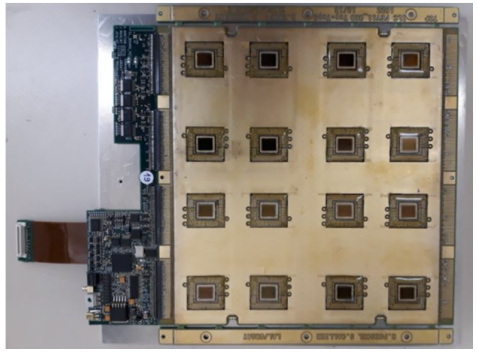
$E(x, z) \rightarrow$ Small R_M



Present ‘FEV-zoo’

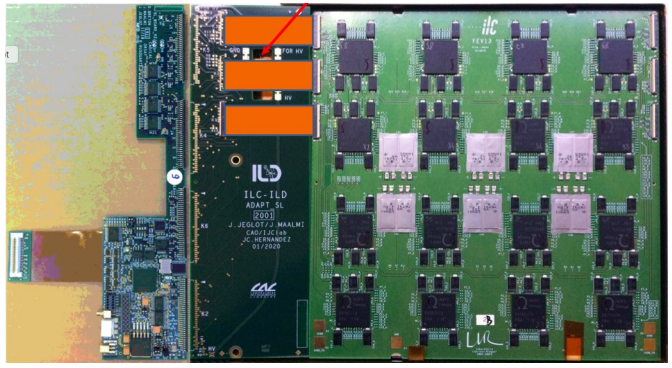
FEV10, 11, 12

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main “Working horses” since 2014



FEV-COB

- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible



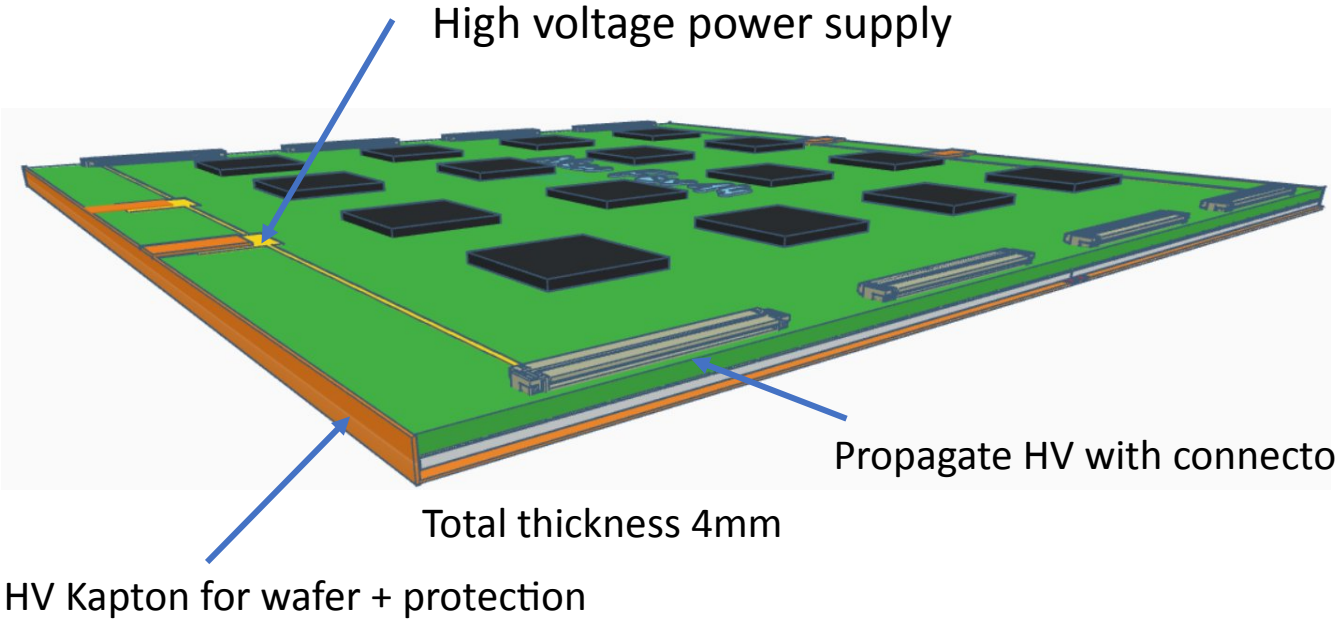
FEV13

- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

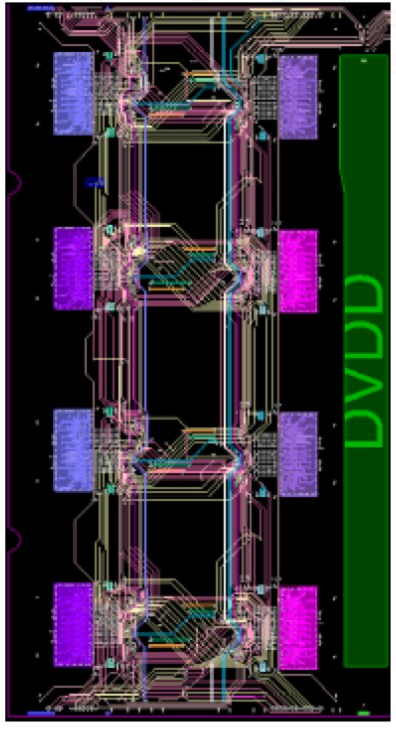
FEV2.0

Requirements

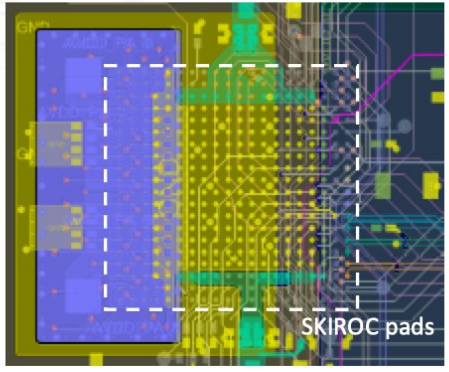
- Compatible FEV10,11,12
  - 16 ASICs
  - 4 Matrices 6”, 1024 chanels
- Improved mecanics, scalability & maintenance
  - Connectors
  - HV distribution & Filtering on PCB
  - 1 HV per card ⇒ independent test, exchangeabil
- LV Regulation on board with LDO
  - local Power-pulsing, lower currents (in B-field)
- Corrected data & clock distributions
  - Must be OK for 2,1 m (EndCaps) = 8 FEV
  - Timing ≤ 0,1 ns ? → for SK3 ?
- Compatibility new DAQ
- Improved noise & decoupling



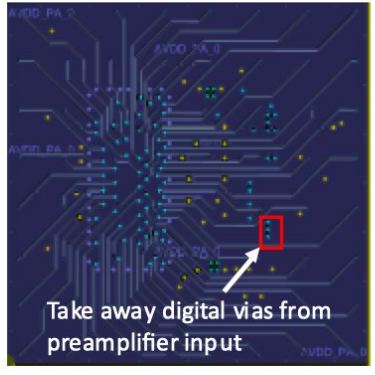
Layout optimizations



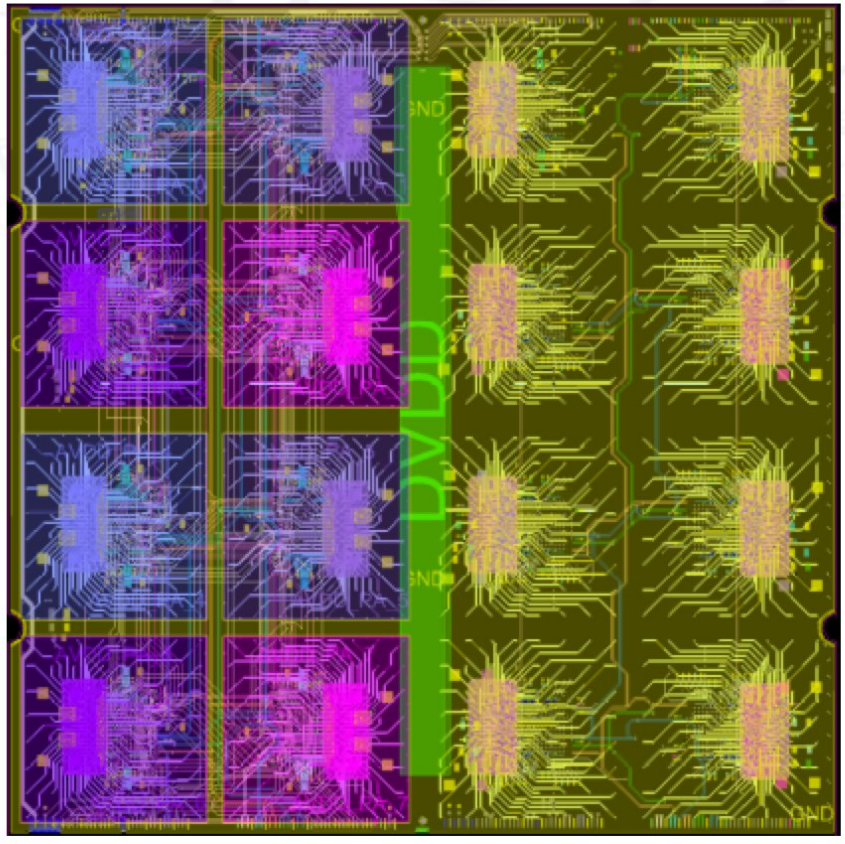
Digital lines optimized for long SLAB



Insulated input signals with GND ring



All patterns of input signal are identical



Board finished 45%

- 5% for LDO power
- 50% for partition duplication