AGH University of Science and Technology

FLAXE ASIC Readout Concept

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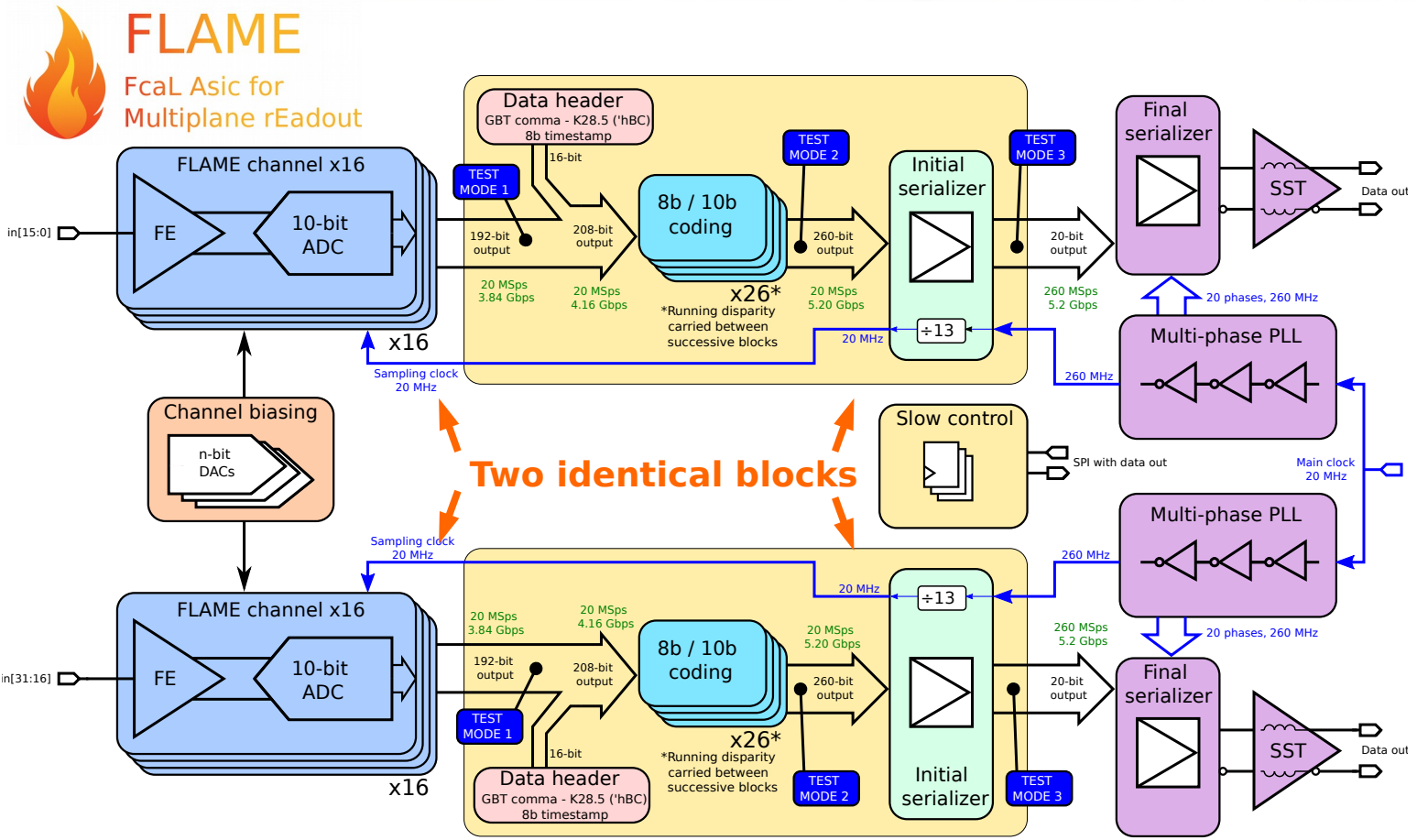
2 June 2022

Outline

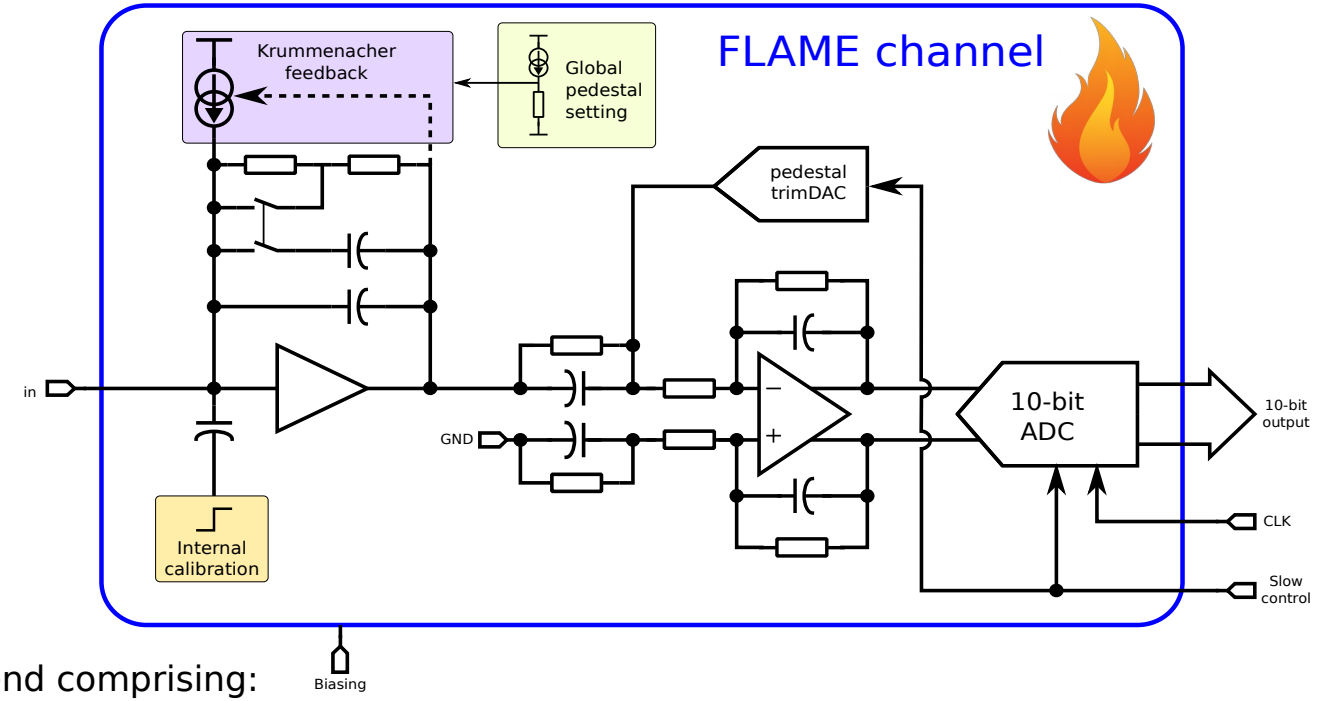
- FLAME - present ASIC for luminosity calorimeter in LC
  - FPGA-based FLAME readout
  - First Test-beam with FLAME
- FLAXE – modified version of FLAME for LUXE
- Summary and Plans

FLAME Readout ASIC Architecture



FLAME is a 32-channel ASIC, designed in CMOS 130 nm, containing FE+ADC in each channel, followed by high speed serializers and data transmission.

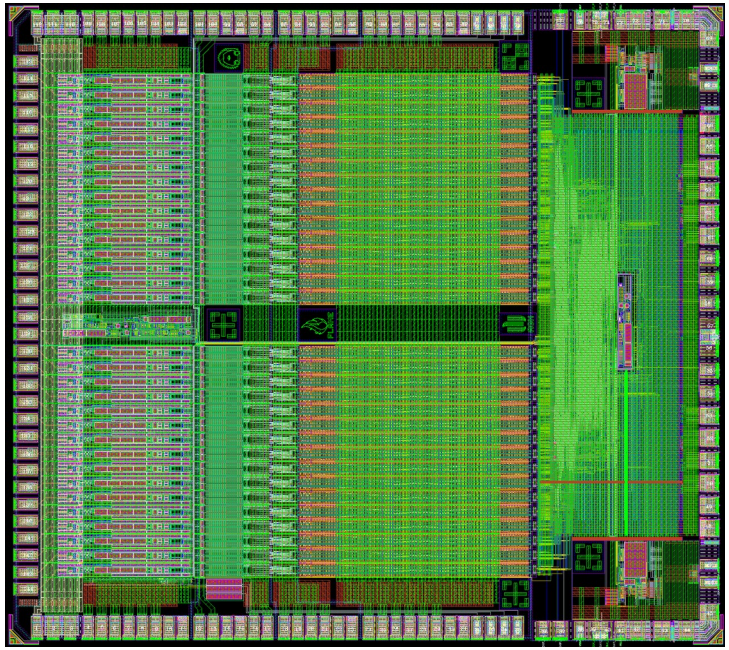
FLAME Readout ASIC
Single channel architecture



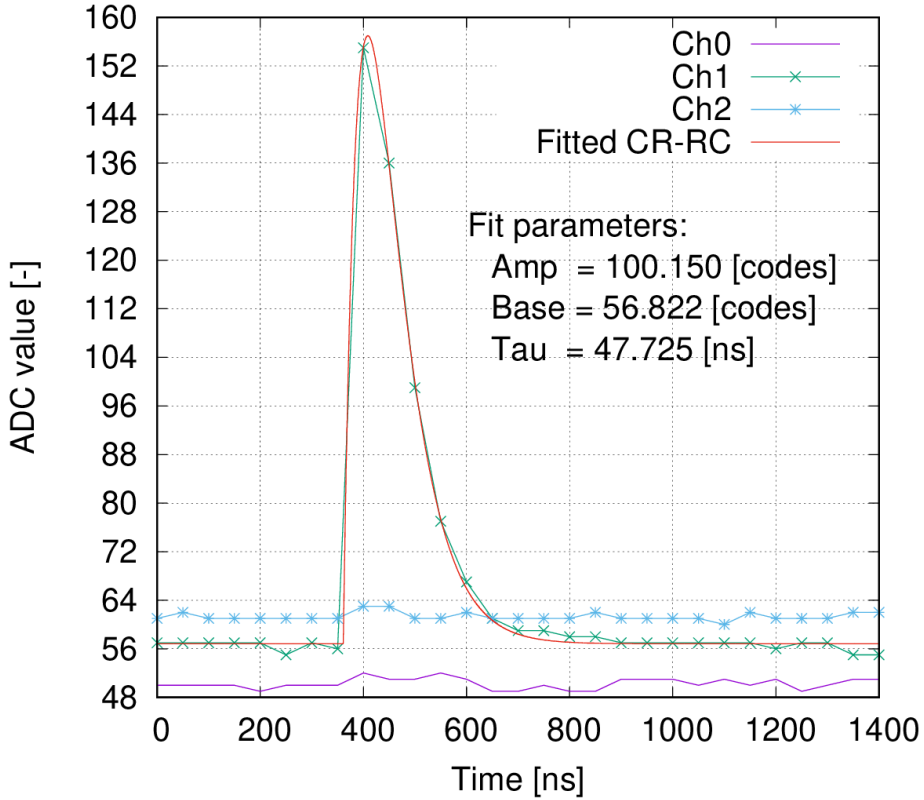
- Analogue front-end comprising:
  - Charge sensitive preamplifier with variable gain:
    - High gain – for MIP sensitivity (up to ~200fC)
    - Low gain – for shower measurement (up to ~6pC)
  - Default detector capacitance ~20-40pF
  - Differential CR-RC shaper with ~50ns peaking time – **for amplitude and time measurement using deconvolution**
  - Krummenacher feedback
  - Internal calibration and pedestal trimDAC
  - Power consumption ~1mW

- 10-bit SAR ADC in each channel
  - Default sampling rate 20MSps (max. up to 50MSps)
  - DNL, INL < 0.5 LSB
  - ENOB > 9.5
  - Ultra low power consumption (<1 mW/channel@40 MSps <0.5mW/channel@20MSps)

FLAME Readout ASIC
Prototype fabrication and First Lab tests



FLAME size 3.7mm x 4.3mm



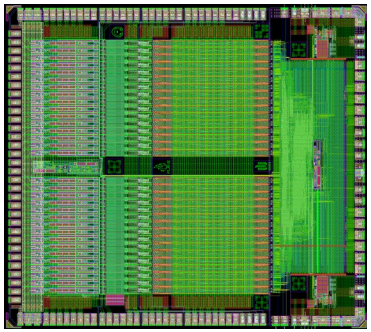
FLAME was fabricated in 2019

All basic functionalities (comprising fast data transmission) were verified

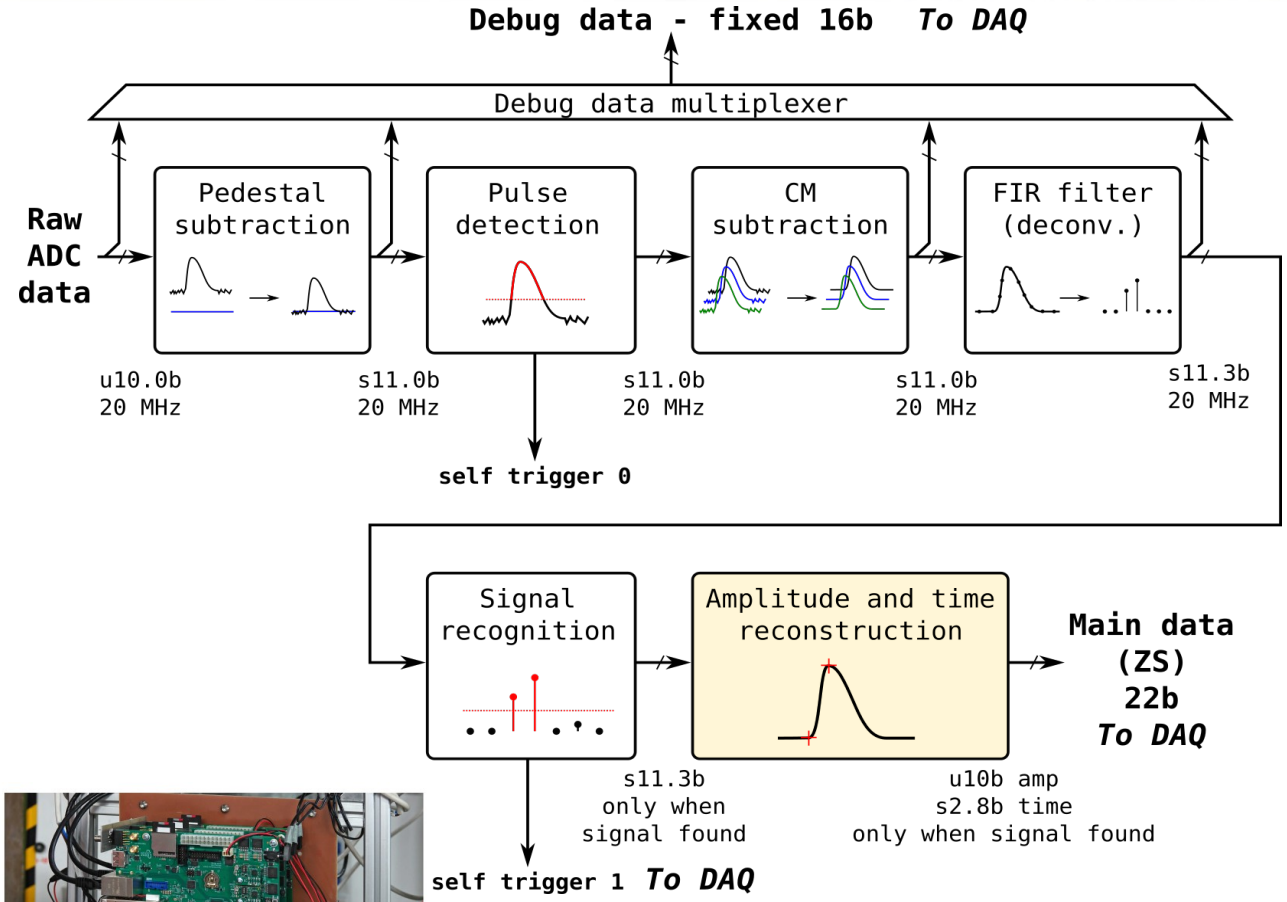
Very good pulse shape was measured, matching with CR-RC shaping

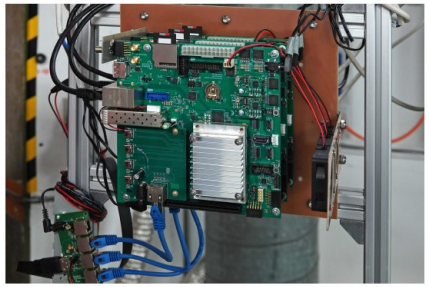
Power pulsing can be used (Digital&ADC OFF, Analog Zero biasing) – to be verified

FPGA-based FLAME Readout
Architecture of FPGA back-end



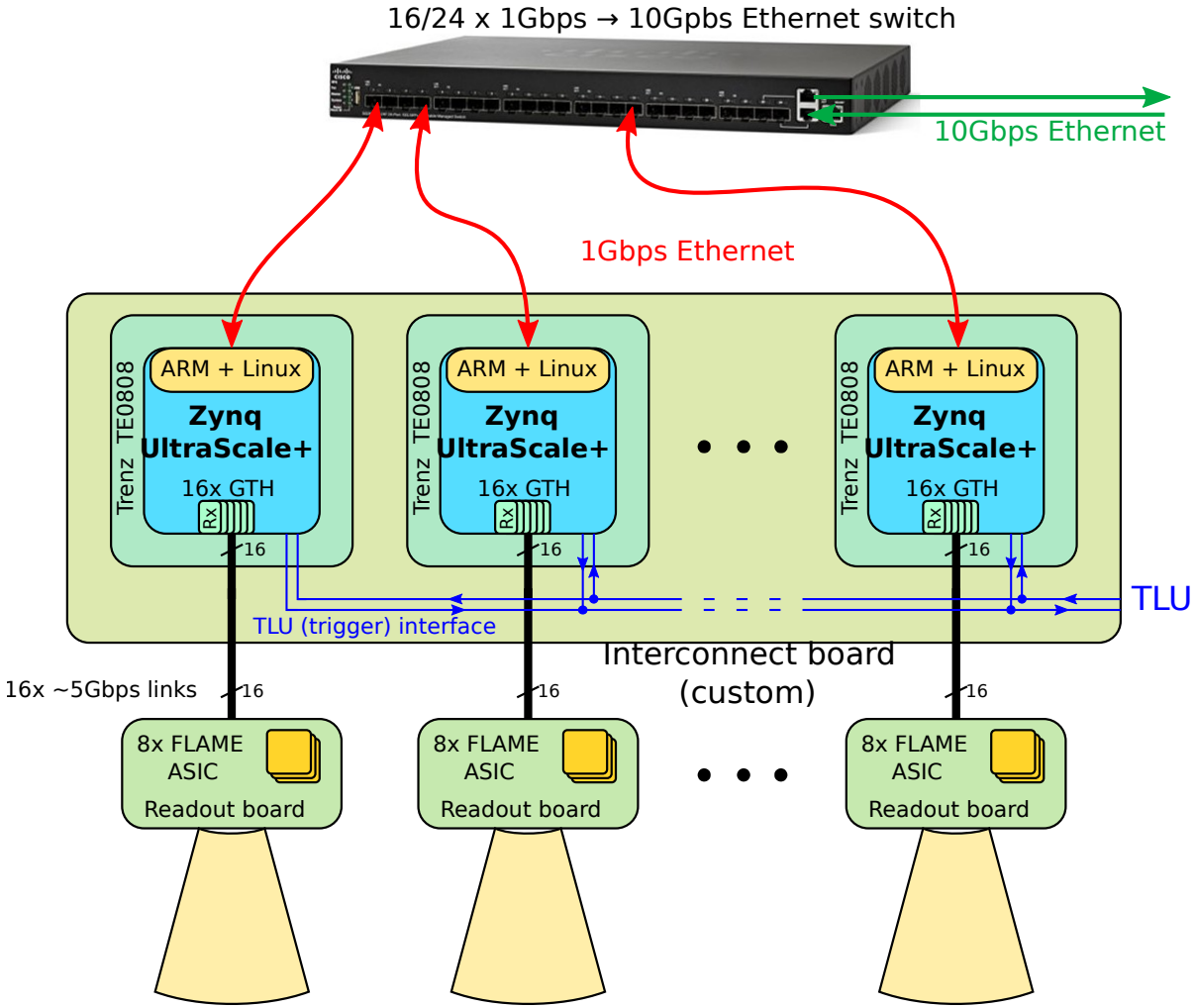
FLAME serializers send data to GTH transceivers of Zynq UltraScale FPGA for online processing





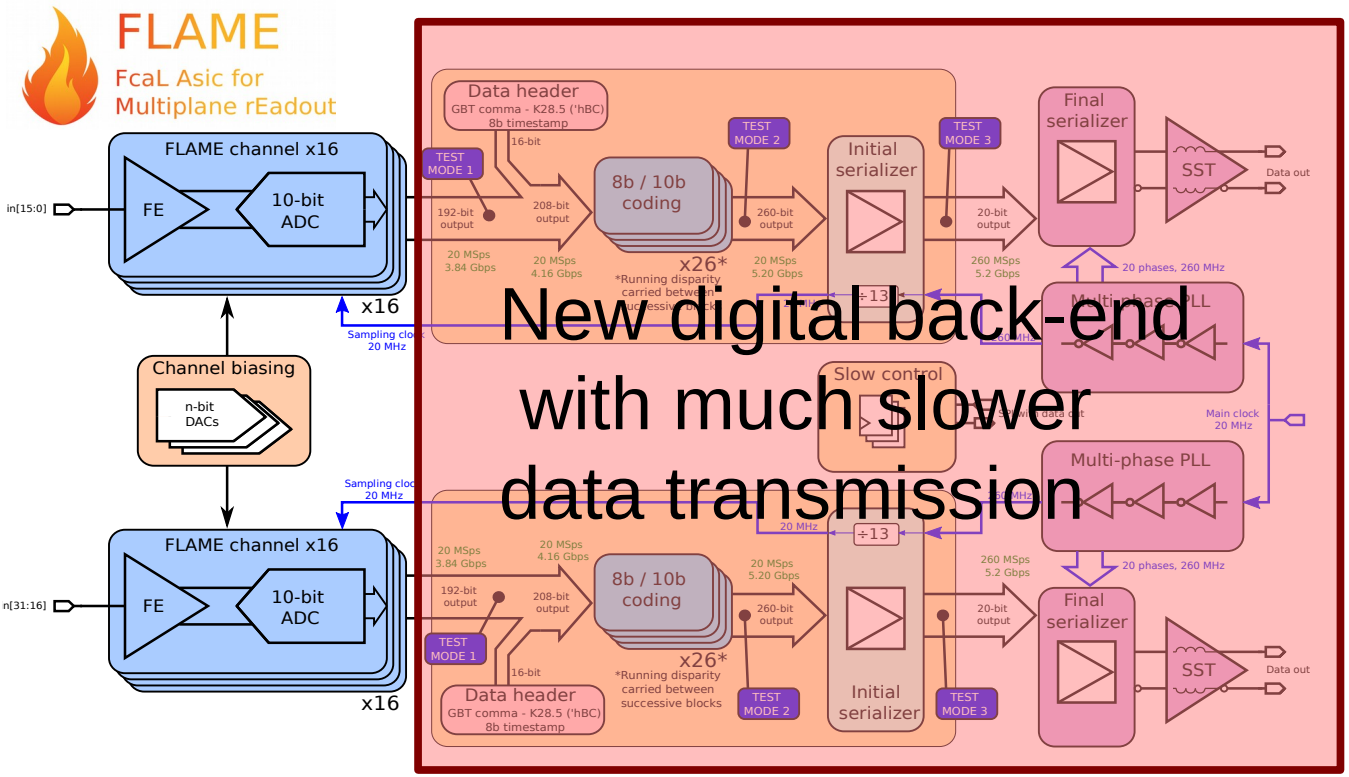
Reconstructed amplitude (10-bit) and time of arrival (~1 ns) information of detected pulses are sent to DAQ system

FPGA-based back-end and DAQ for FLAME



- We have developed a FPGA-based back-end and DAQ receiving many high speed (5.2Gbps) data links, processing data, and doing zero-suppresion
- FE board contains 8 FLAMEs / plane = 256 channels = 16 data links (2 links per FLAME)
- Trenz Electronic modules (TE0808) with Zynq UltraScale+ FPGA, with 16 GTH transceivers are used
- Such readout was used in beam-ests at DESY in 2020 and 2021

FLAXE Readout for LUXE Ecal



For FLAXE the digital serialization and data transmission circuitry will be significantly simplified since very low trigger rate and output data rate is needed in LUXE

Summary and Plans

- Dedicated FLAME readout ASIC with FPGA-based back-end were developed for luminosity calorimeter and its operation was verified in the Lab and on the Beam
- Presently we are preparing FLAXE ASIC, a modified FLAME version for LUXE ECAL experiment
  - digital serialization and data transmission circuitry will be significantly simplified since very low trigger rate and output data rate is needed in LUXE
- We have recently received grant for development of ECAL for LUXE
  - It is critical to have FLAXE chip in the ECAL, since it is a main part of the grant

Thank you for attention