Gluing of sensors

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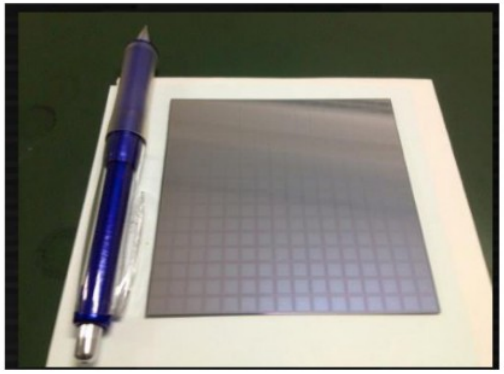
Silicon Sensors

Si Sensor (9x9cm^2 from 6" wafer)



Wafer specs

Tab 1 : Summary of the substrate characteristics

	Min.	Typ.	Max.
N type silicon	-	-	-
Resistivity (kOhms.cm)	4	5	-
Thickness (μm), option T1	310	320	**330**
Thickness (μm), option T2	490	500	**510**
Width (mm), option S1	89.7	89.8	89.9
Width (mm), option S2	44.7	44.8	44.9

Definition of specifications for different wafer types:
Resisitvity: > 5 kΩxcm

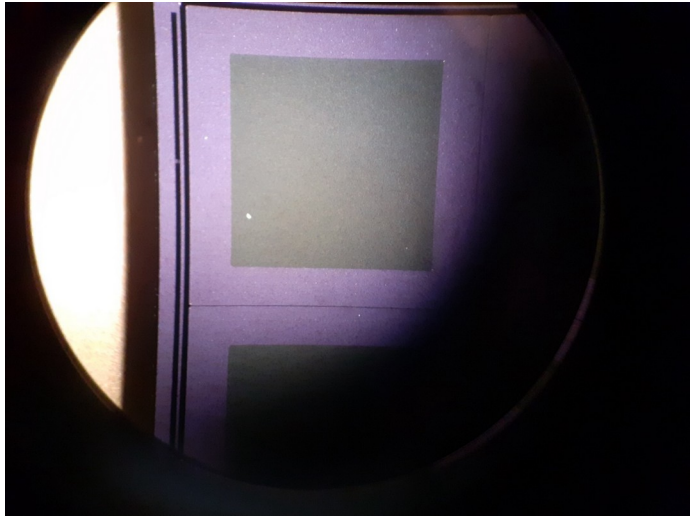
N-type silicon
Crystal Orientation: <100> or <111>

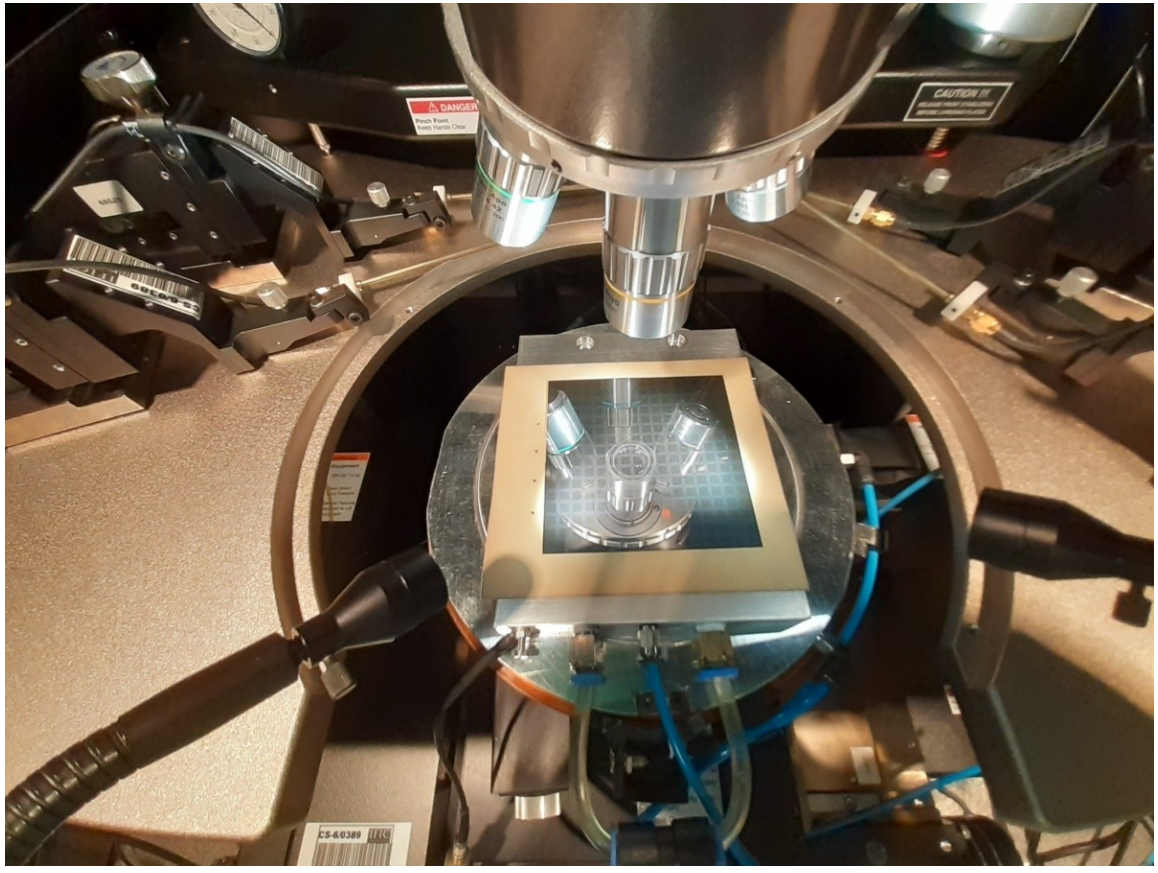
- In addition we require small leakage current:s under full depletion a few nA/pixel
  but for cost reasons we tolerate a certain fraction of pixels with higher leakage currents

- Vendors: OnSemi (CZ) and Russian company for physics prototype (~2003)
  Hamamatsu for technological prototype (since ~2010)
  Contacts with other vendors (e.g. LFoundry) hibernating mainly for funding reasons

Silicon Sensors

- Hammamatsu
- 500umx90mmx90mm
- 256 PIN diodes (5.5mx5.5mm)
- No guard rings

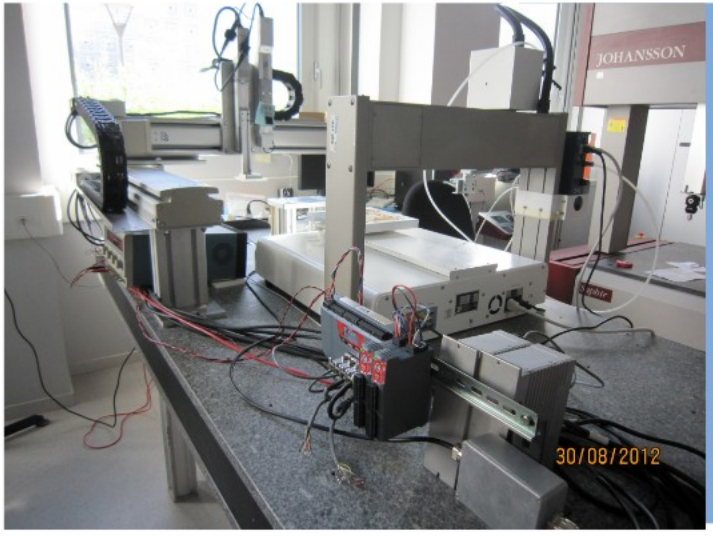


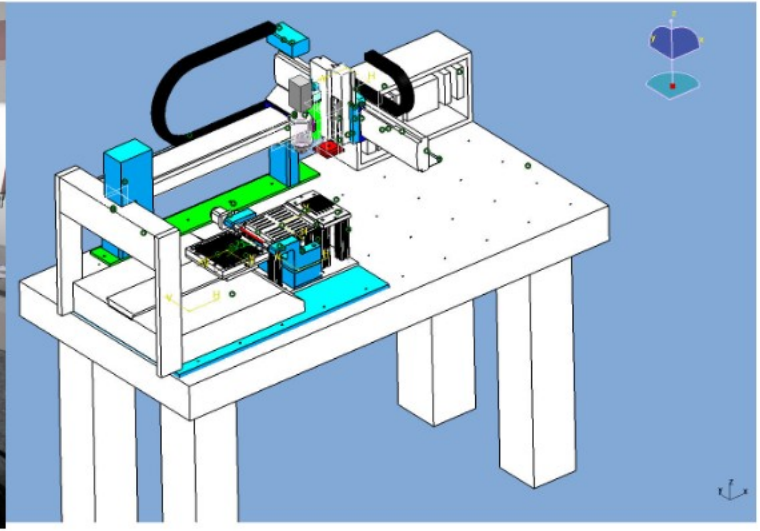


Gluing (LPNHE & Kyushu U.)

- A new system was purchased for:
  - Positioning
  - Wafer and PCB handling
- Gluing process performed with the current machine

2 robots +1 pcb aspiration palate
- robot1 for positioning and gluing deposition
- robot2 for aspiration nof the wafr and deposition on top of the PCB





Gluing (LPNHE & Kyushu U.)

- Glue: EJ2189LV (since 2018?)
  - https://ftpolymer.fr/colles-epo-tek/colles-conductrices-electriques-epo-tek/colle-epoxy-bicomposante-ej2189/
- Specs: 80°C/3 Hours - 23°C/72 Hour

Procédure de collage

Mélange 90%/10% durcisseur
- mesure à la balance de précision (qq g)
- **1-2 mins à la main**
  - centrifugeuse au LLR
- ⚠ poussières
- rem: PAS DE DÉGAZAGE

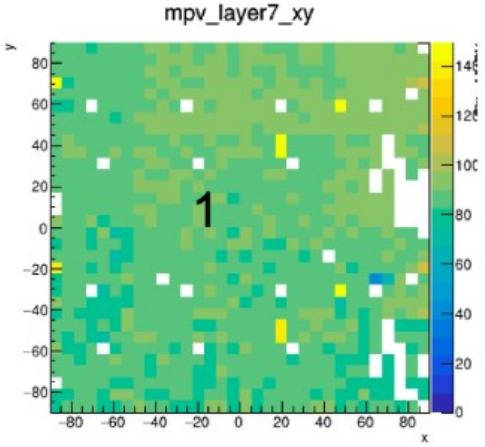
Dépôt
- **même qté**
  - sf 1re rangée
  - **par pression×temps dispenseur**
    - Ajustage à chaque collage (fluidité, température)
    - temps de pose ~ 30 mins
    - colle ~ validité qq h

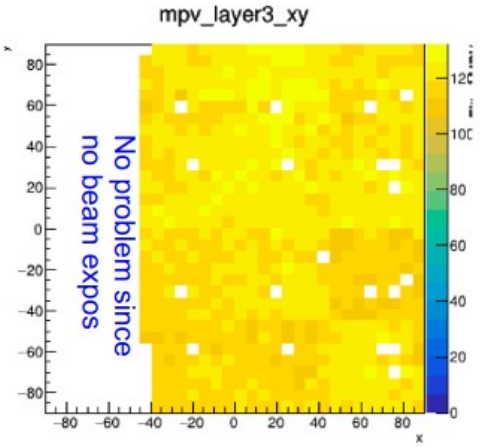
points centrés
- **décalage 1er points, rang exterieurs**
  - 0,2 mm

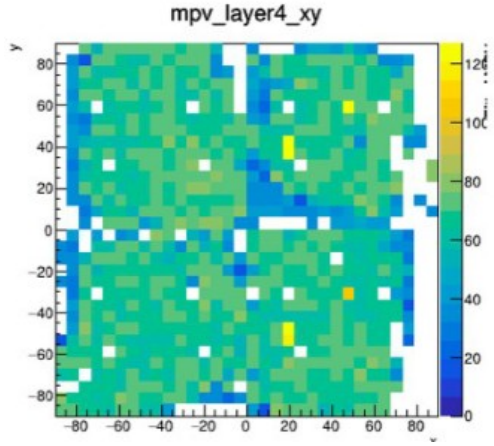
Polymerisation
- **1 nuit à 40°C**

wafers aspirés et posés dessus à distance fixe
- **point de colle Ø 1–2 mm × 0,3mm**
  - moins homogène

Observed issues







- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
    - Understood and will be corrected

... and not so good layers

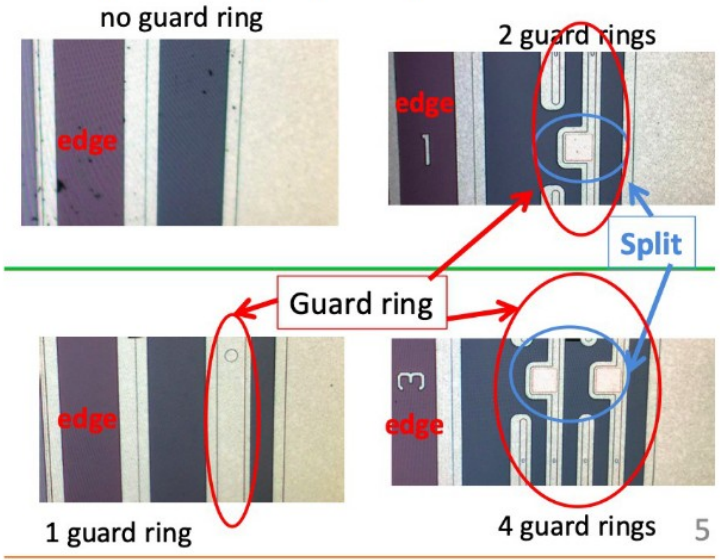
- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => major debugging tool
- In any case less good layers will be replaced in coming months

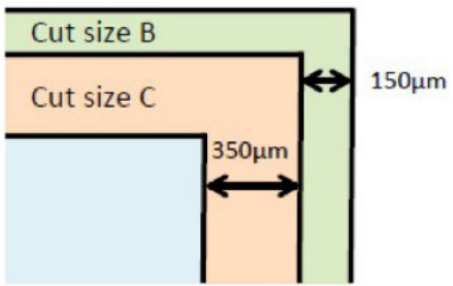
Observed issues: strategy

- Hot topic... for after the beam test.
  - We started a “educated” brainstorming between most actors on how to address this issue
- Mechanic issue ?
  - bending of the PCBs
  - vibrations
- Chemical issue ? (degradation of the glue)
  - Due to ambiental circumstances? (humidity, change of temp....)
- Improvable method? (curing time? Etc?)
- Access to resources like climate chambers, vibration tables etc ?
  - Under discussion.
  - CERN? IN2P3? IFIC?
- IFIC budget request for a gluing robot + material + postdoc in order to contribute on
  - the systematic gluing aging studies, module assembly
  - Simulation studies & data analysis
- Kyushu U. also performed gluing on sensors
  - Dedicated comparison between performance of both ?

SiW Ecal – Wafer R&D II

We (i.e. Mainly Kyushu) have tested several wafer types in previous years





- Cut size determine the actual sensitive area of a wafer
- Different designs mainly on test samples of “baby wafers”
- The “Hamamatsu” standard is still 0 or 1 full guard ring
  - 0 is “fake 0” guard ring, in fact there is still a small guard ring

Observations in recent years (see also backup for more details)

- Split or no guard ring lead to suppression of square events
- In prototype we still use full wafers with 0 or 1 guard ring
- General trend of reduction of bias voltage
- Can operate 500mum wafers at 60-80 V in full depletion

- Towards 8” wafers?
  - General trend (e.g. CMS) is to use 8” wafers
  - Larger surface/wafer =>smaller cost
  - Standard thickness 725mum