Further pixel chip testing

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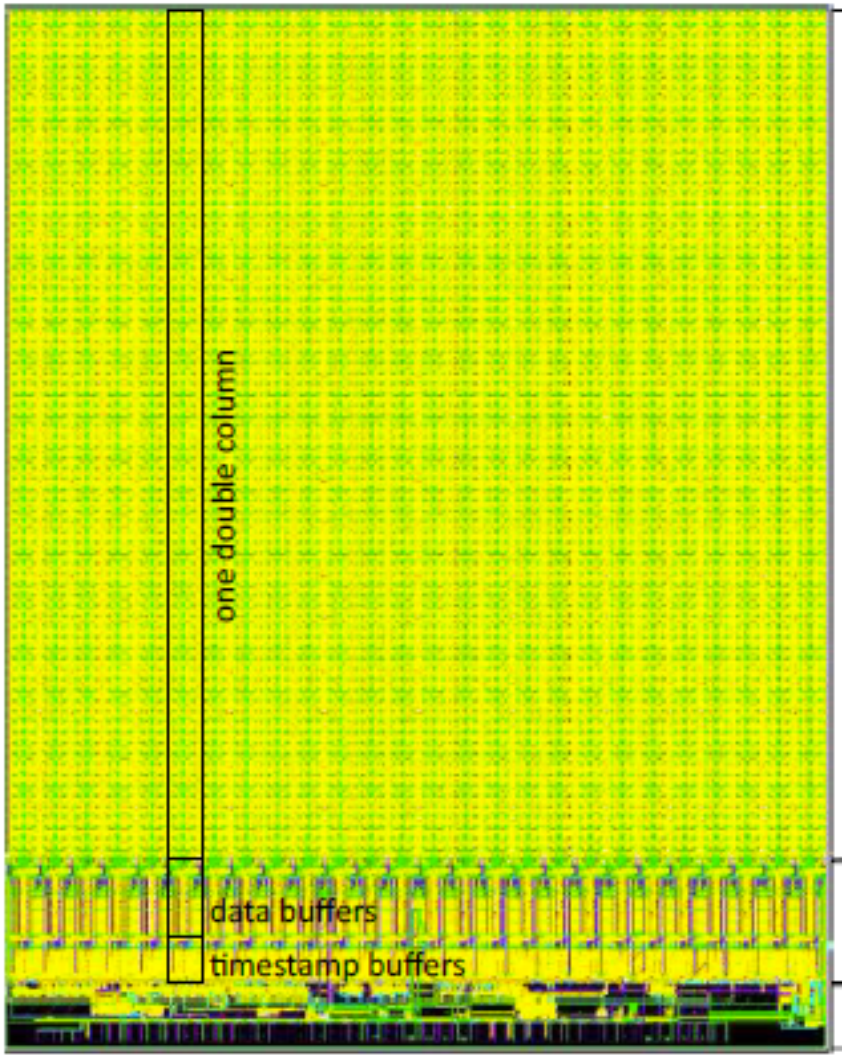
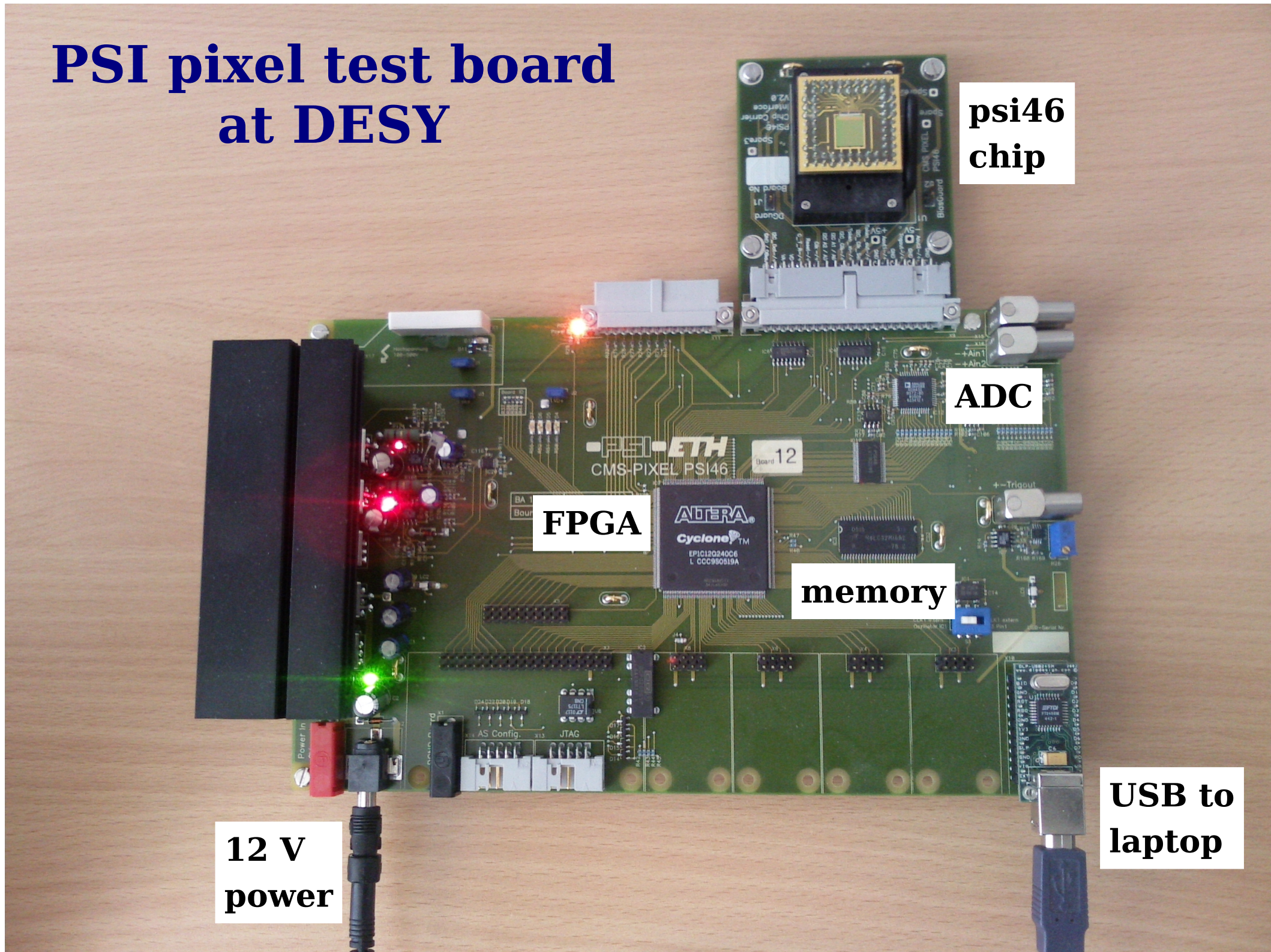
CMS Tracker Upgrade 8.3.2011



- software progress
- power
- timing study
- working point
- thresholds

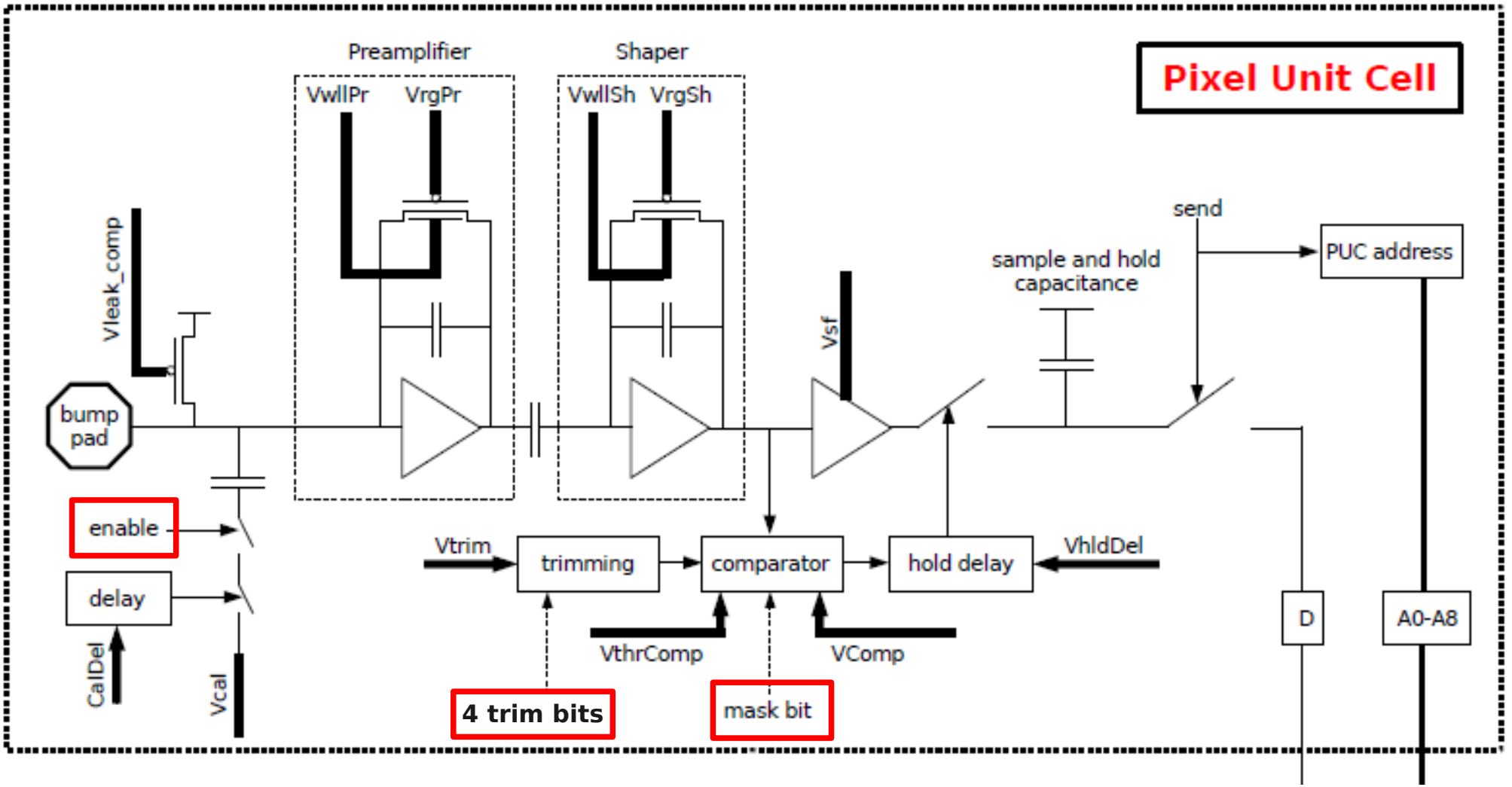
PSI pixel test board at DESY



Software technical progress

- Instead of single pixel, single measurements (slow USB setup) now:
  - activate 26 or 52 pixels in parallel columns and transfer together,
  - perform scan of DAC settings from the FPGA, transfer 256 values.
- Shifted readout timing by 2 BC:
  - CalDel 25 → 125, WBC 21 → 20, tct 24 → 25.
- Decode pixel address:
  - C1, C0, A2, A1, A0 → column, row.
- Steer psi46expert by command script instead of interactively:
  - faster, reproducible, self-documenting.
- Fast efficiency determination on the FPGA does not work:
  - Configuration problem (single ROC test, no TBM)?
  - Have to use slower methods...

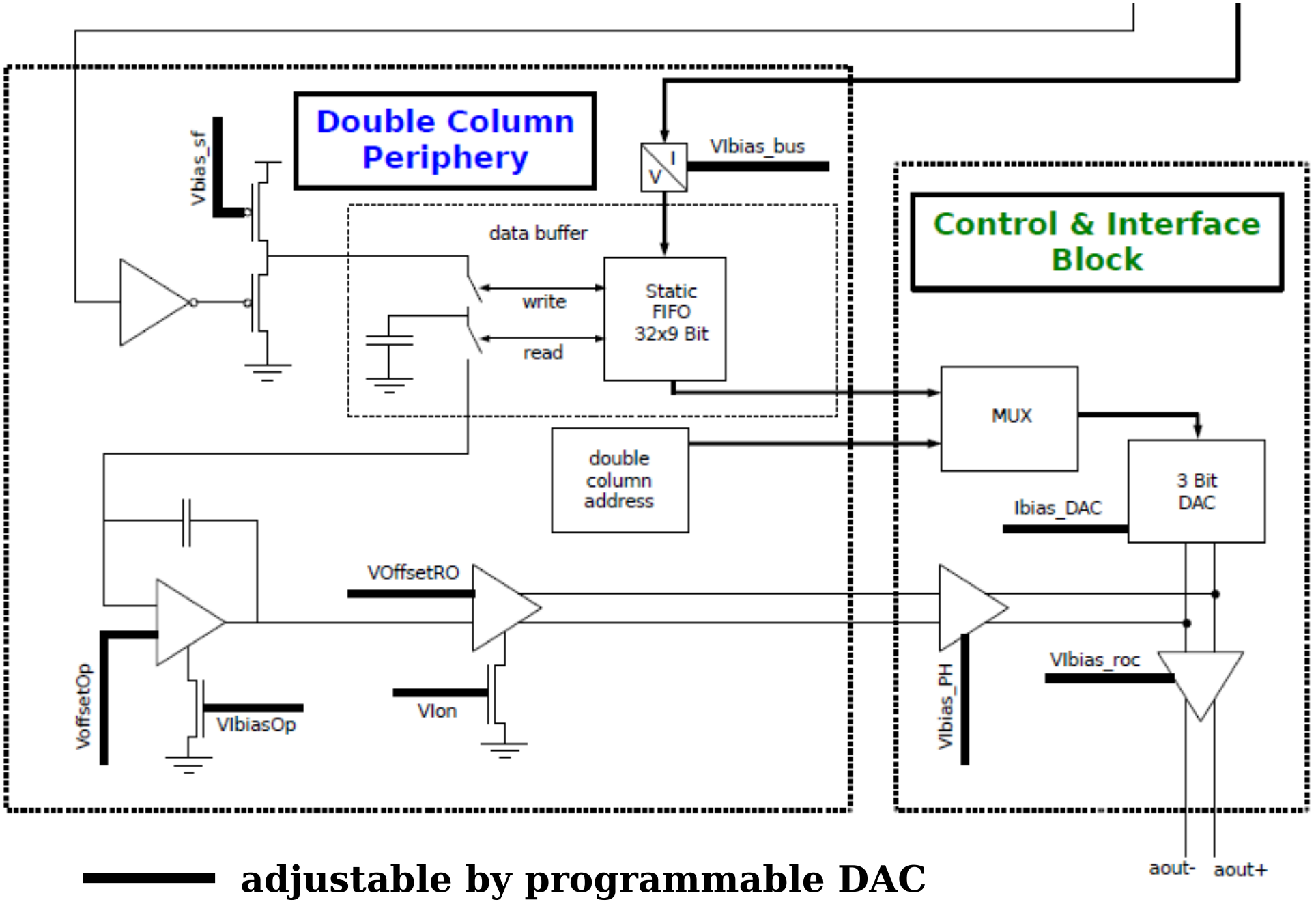
psi46 pixel readout chip



adjustable by programmable DAC, per ROC

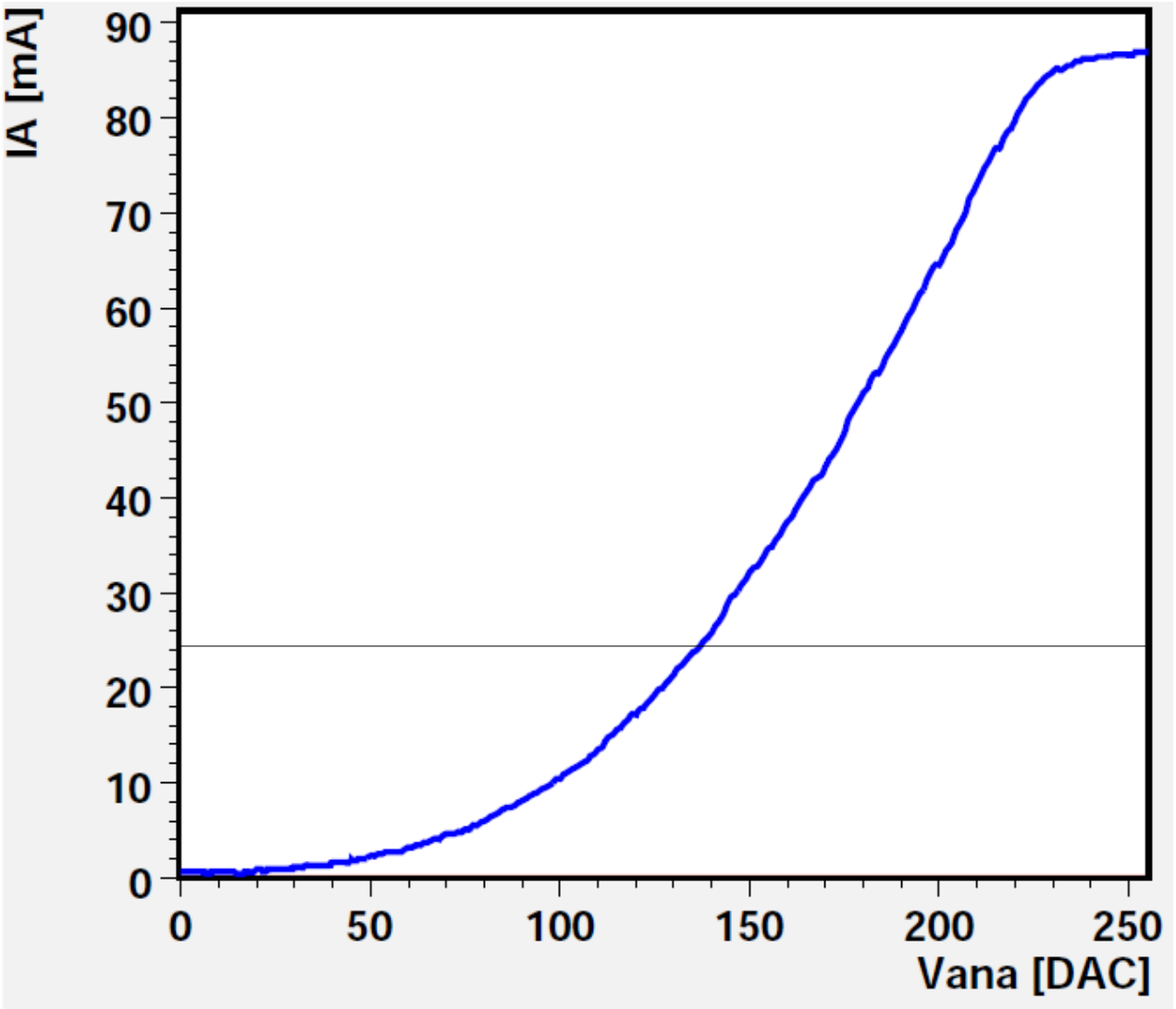
programmable register, per pixel

psi46 pixel readout chip



adjustable by programmable DAC

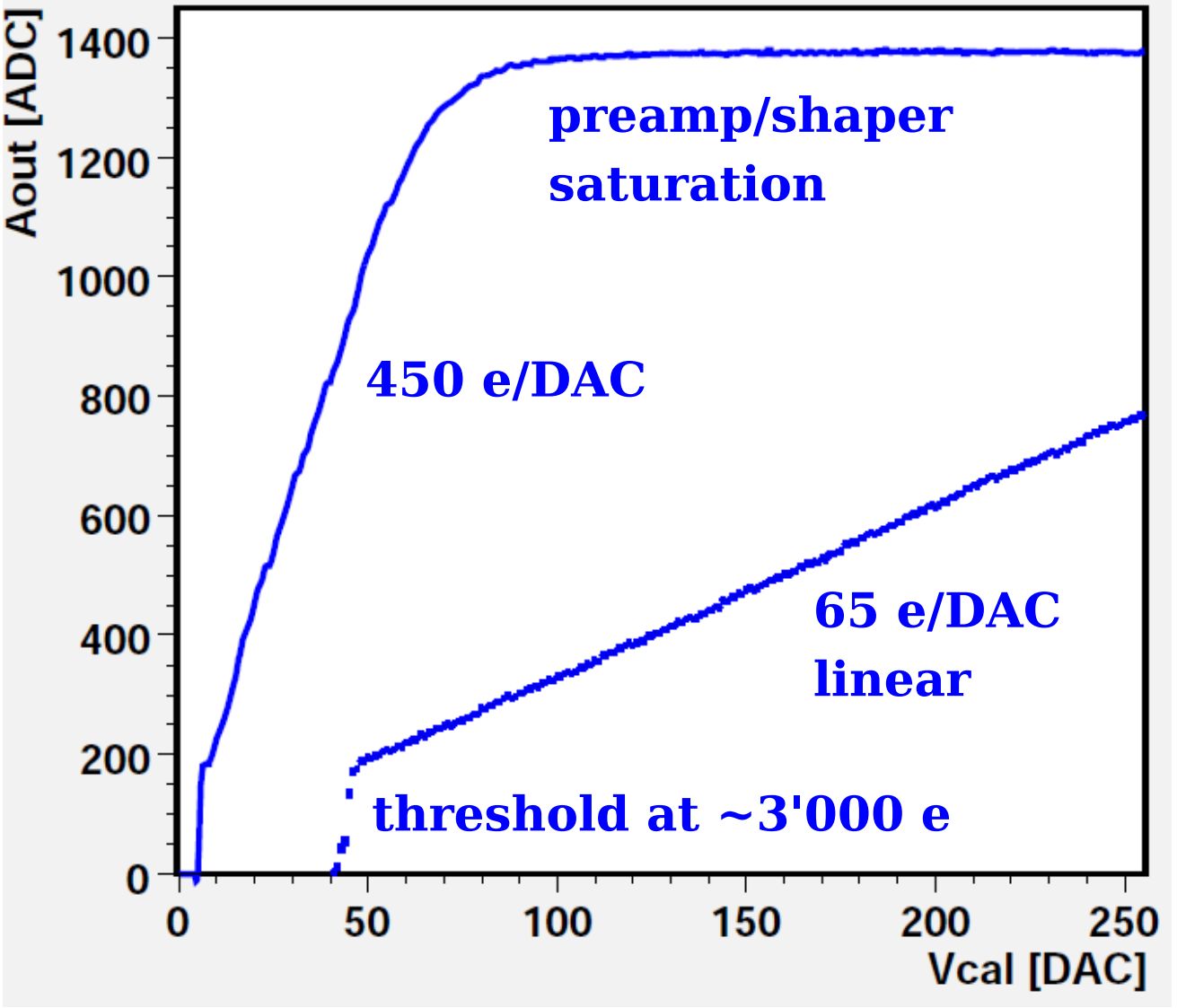
power



currents measured on test board.

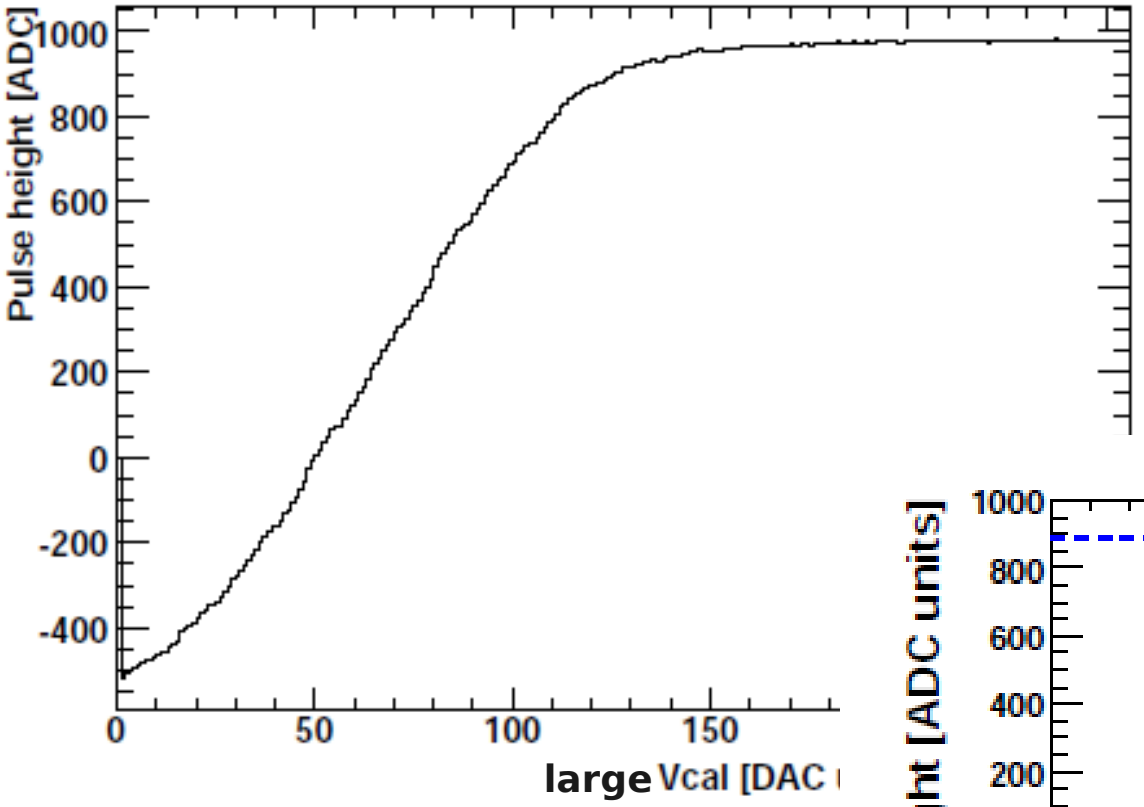
- External supply:
  - VA = 1.7 V,
  - VD = 2.5 V.
- Analog and digital voltage can be further regulated on chip.
- PSI:
  - IA = 25 mA,
  - ID = 35 mA.
  - total 130 mW / chip
  - 31 µW / pixel,
  - 2.1 W/module,
  - 1.5 kW for Barrel.

gain and linear range



- One pixel.
- 2 Vcal ranges (PSI X-ray calibration):
  - CtrlReg 0 or 4,
  - 65±5 e/DAC,
  - 450 e/DAC.
- Linearity for small pulses important for spatial resolution using charge sharing.
- Saturation around 36'000 e (~2 MIP).

linear range and saturation at PSI



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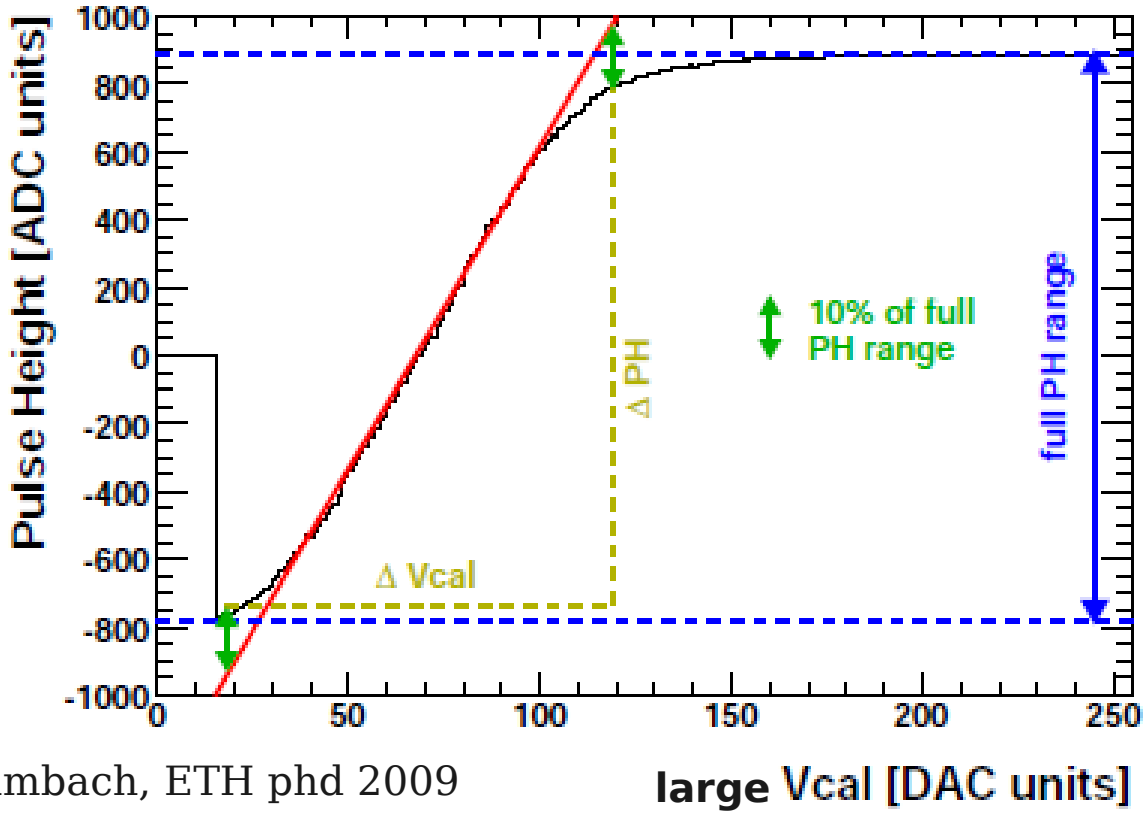
- Taken at PSI:
  - looks similar.
  - somewhat larger linear range
  - different working point?



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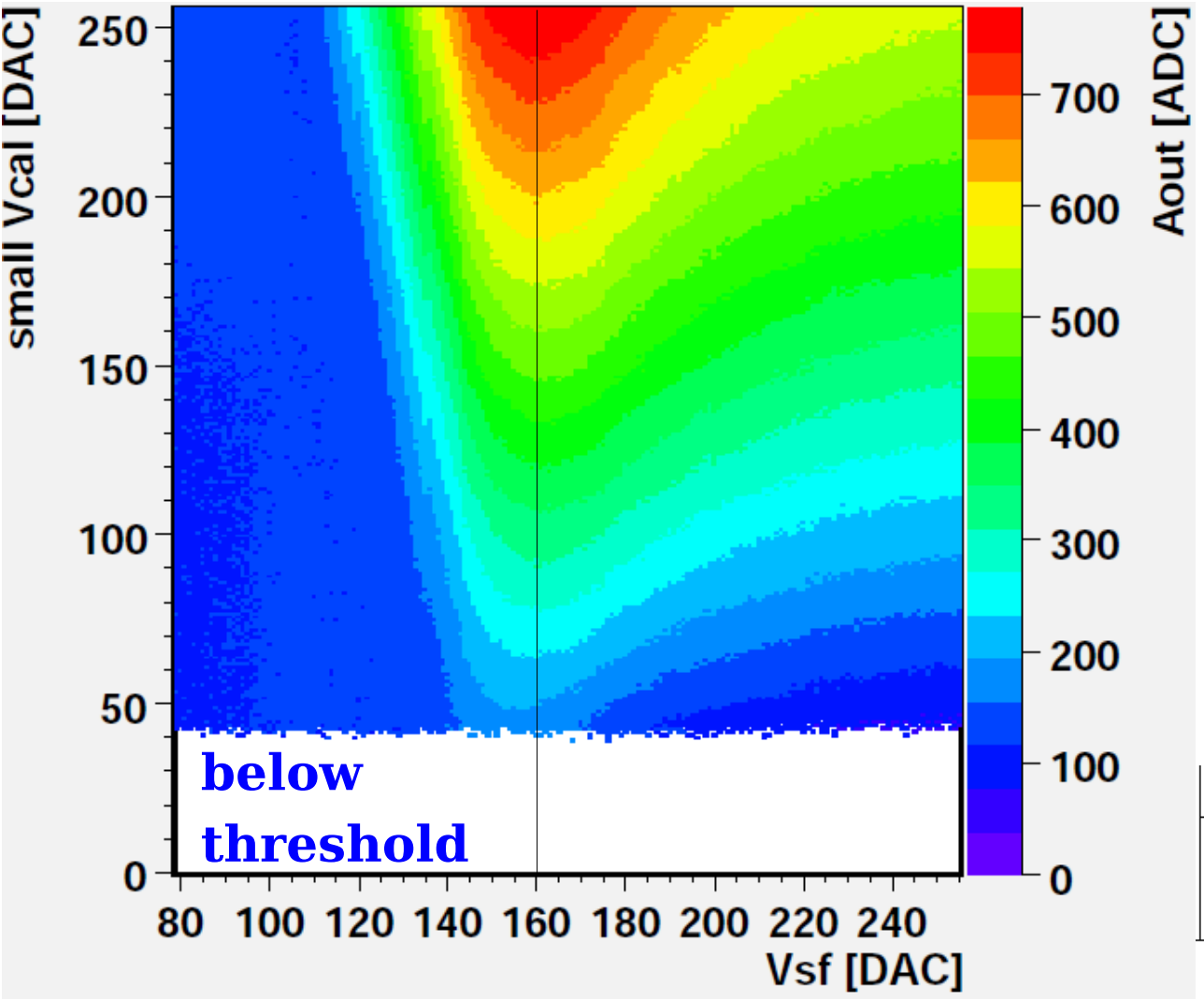
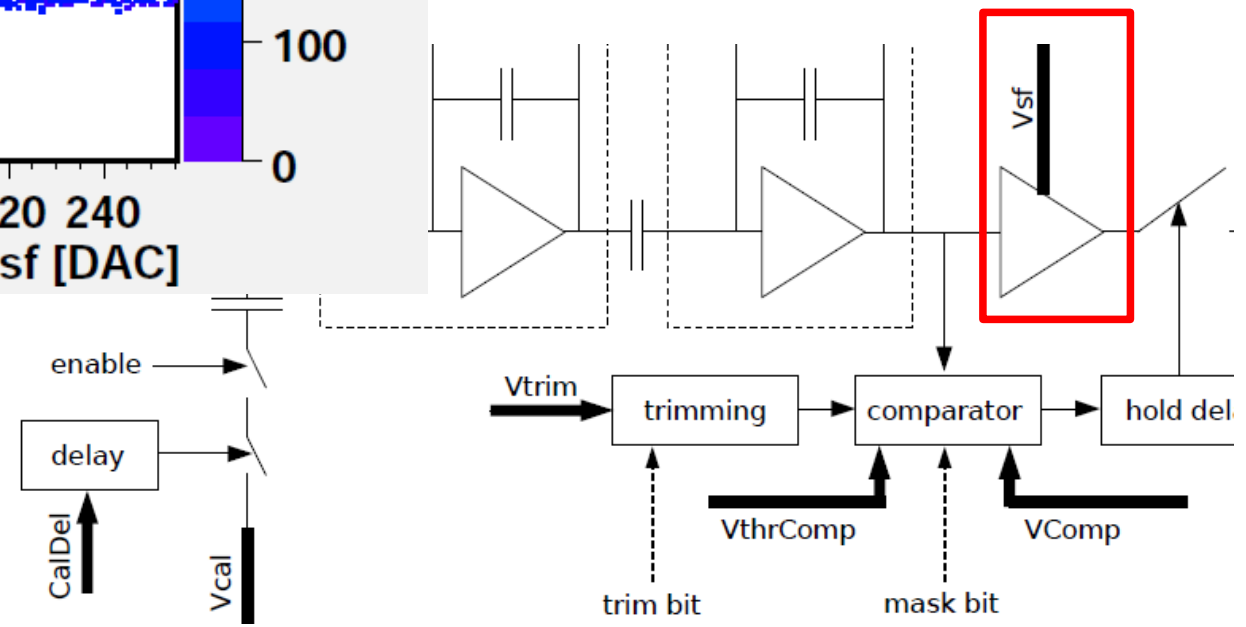
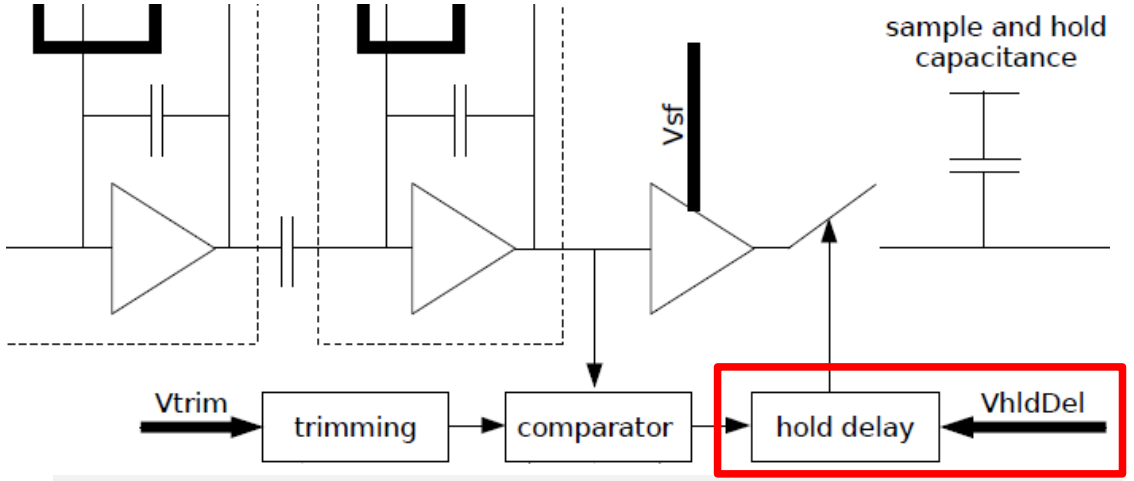
Linear range vs Vsf

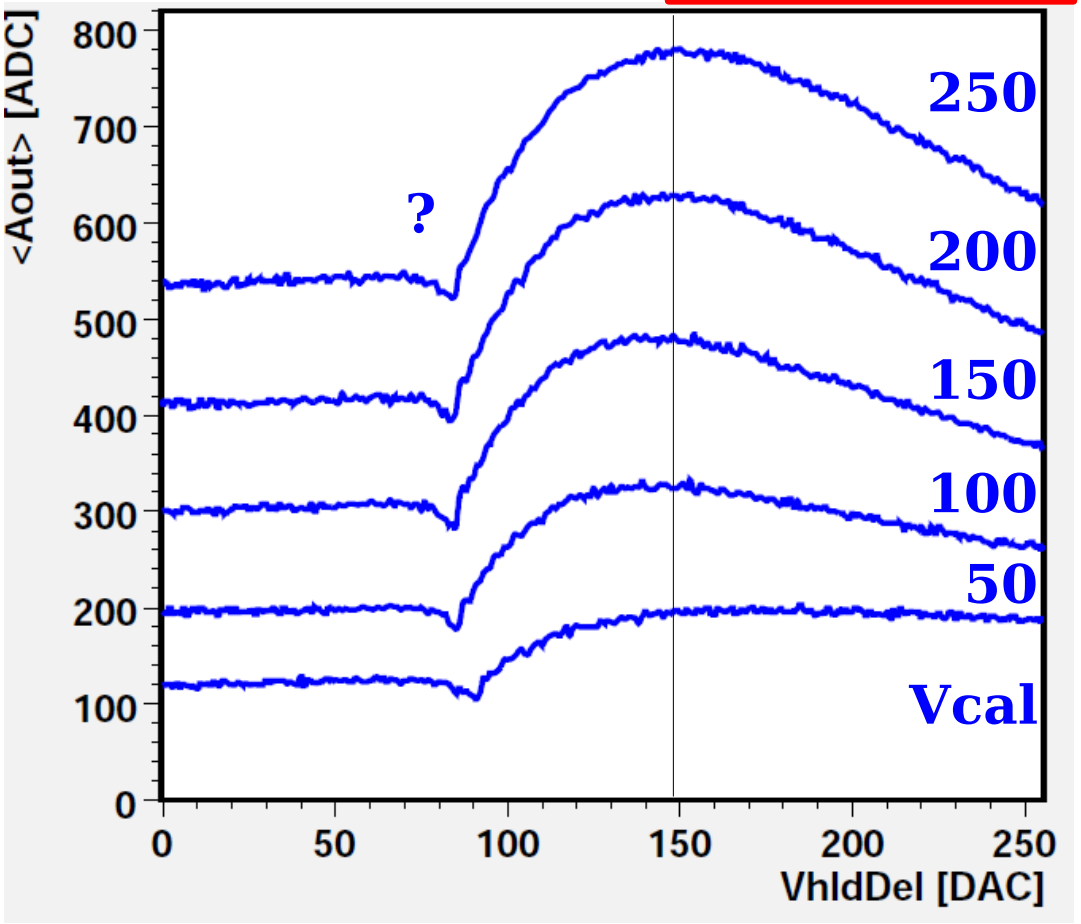


- One pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Best linearity in valley.



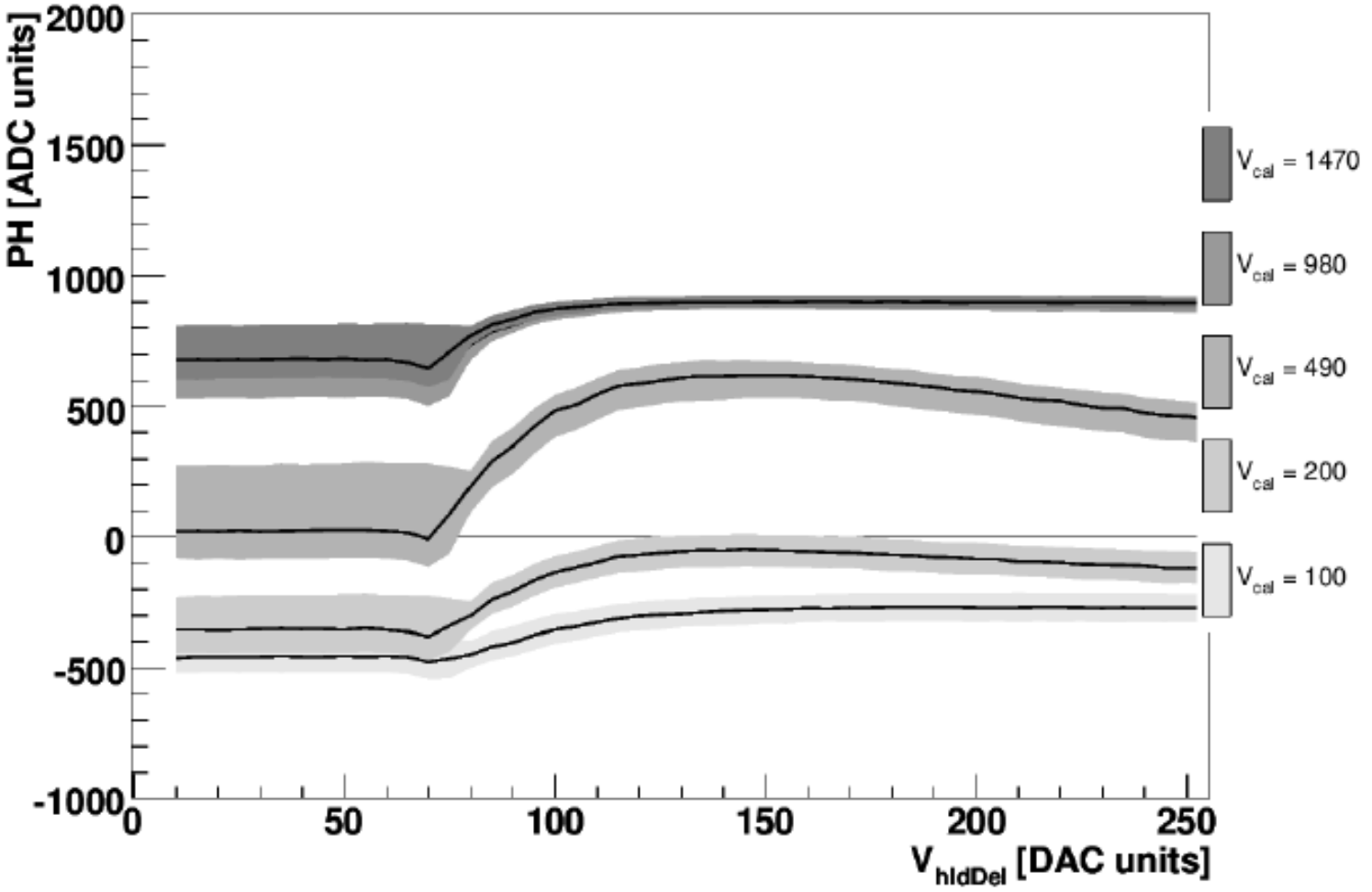
Sample and hold timing





- One pixel.
- Position of maximum depends on pulse height:
  - time walk.
- DAC 150 is compromise

Sample and hold timing at PSI



- Similar observations
- Somewhat different working point.

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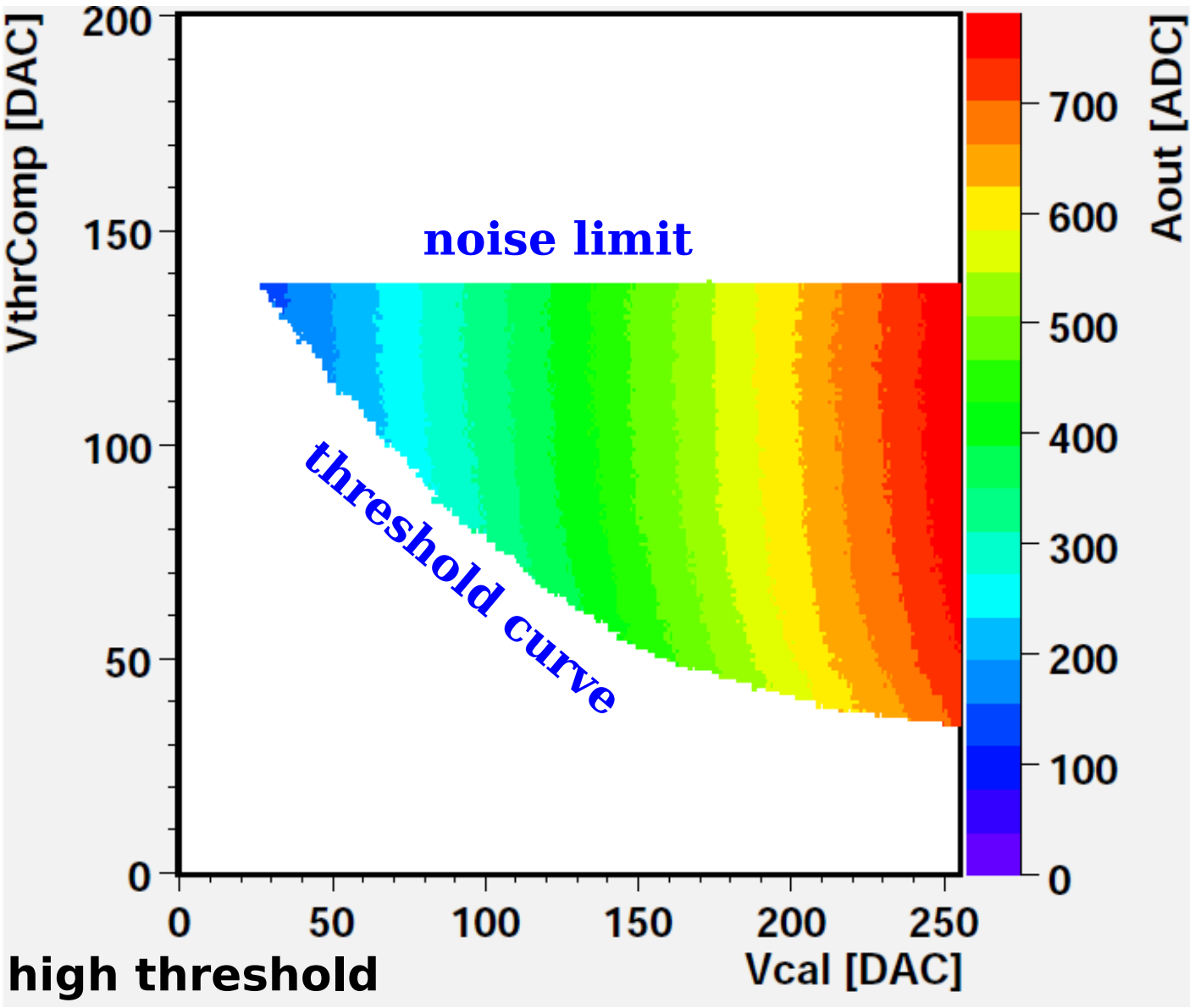
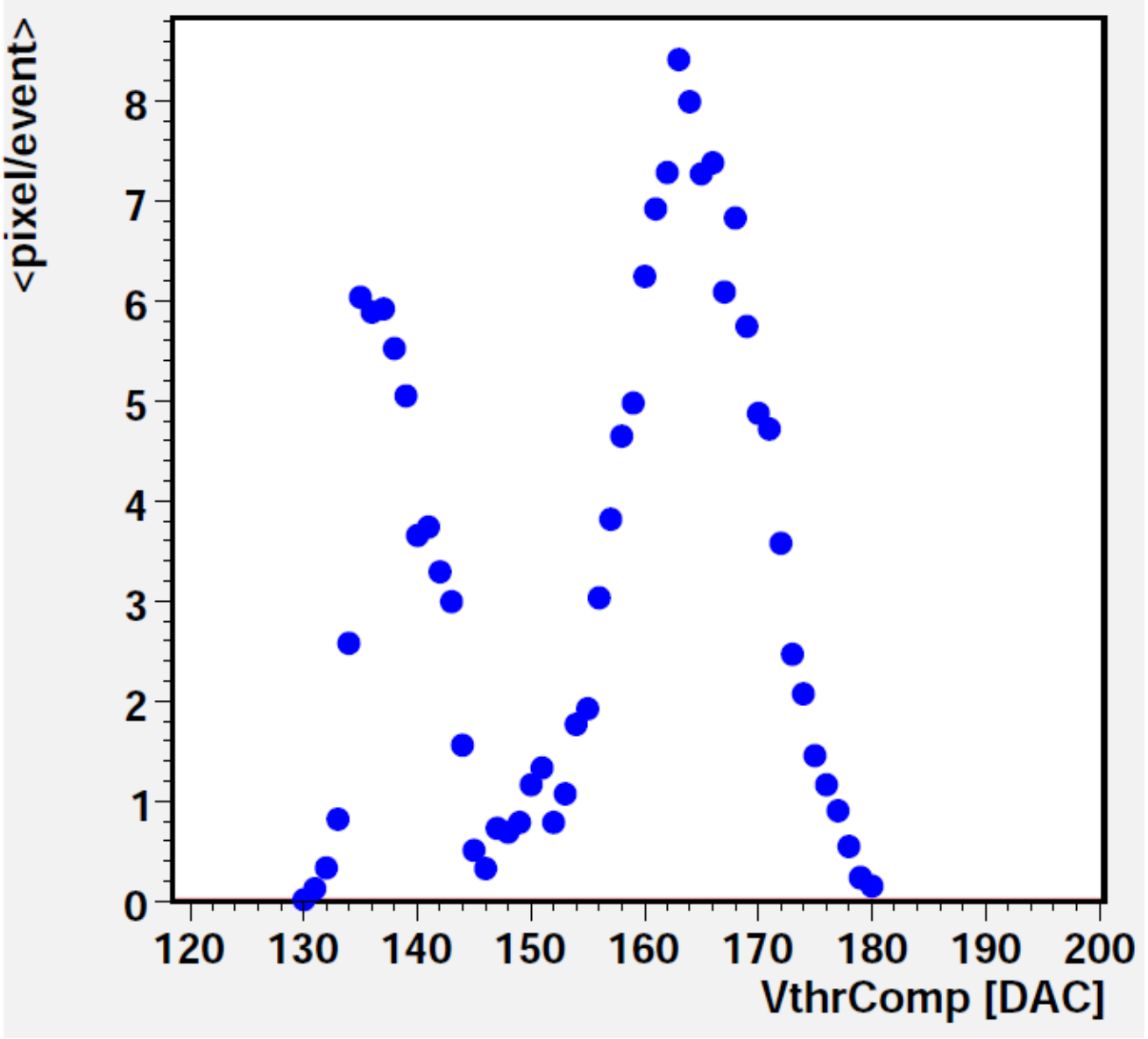
Comparator threshold



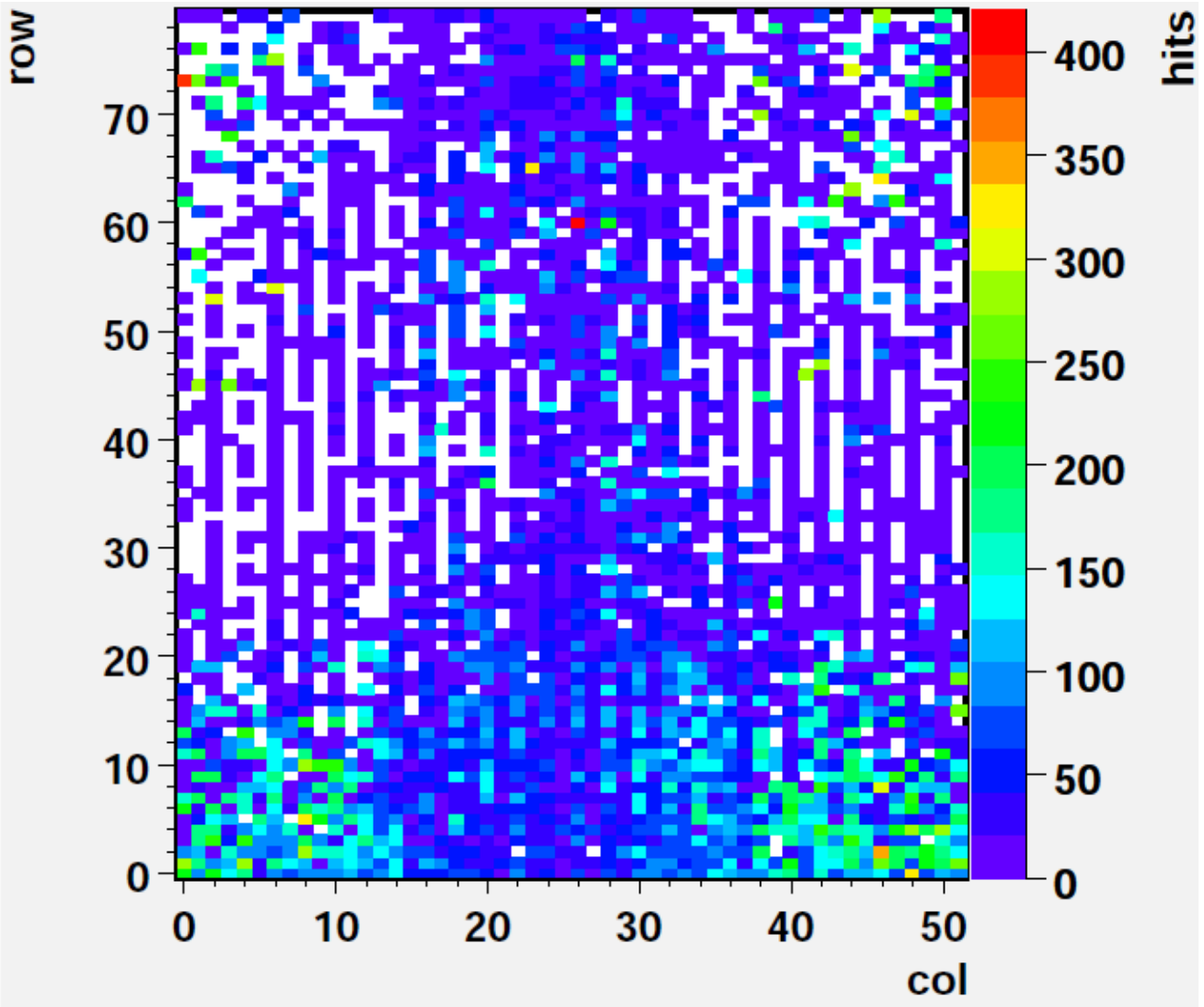
- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- White region:
  - no signal.
- Colored bands are not vertical:
  - time walk.

Noise limit



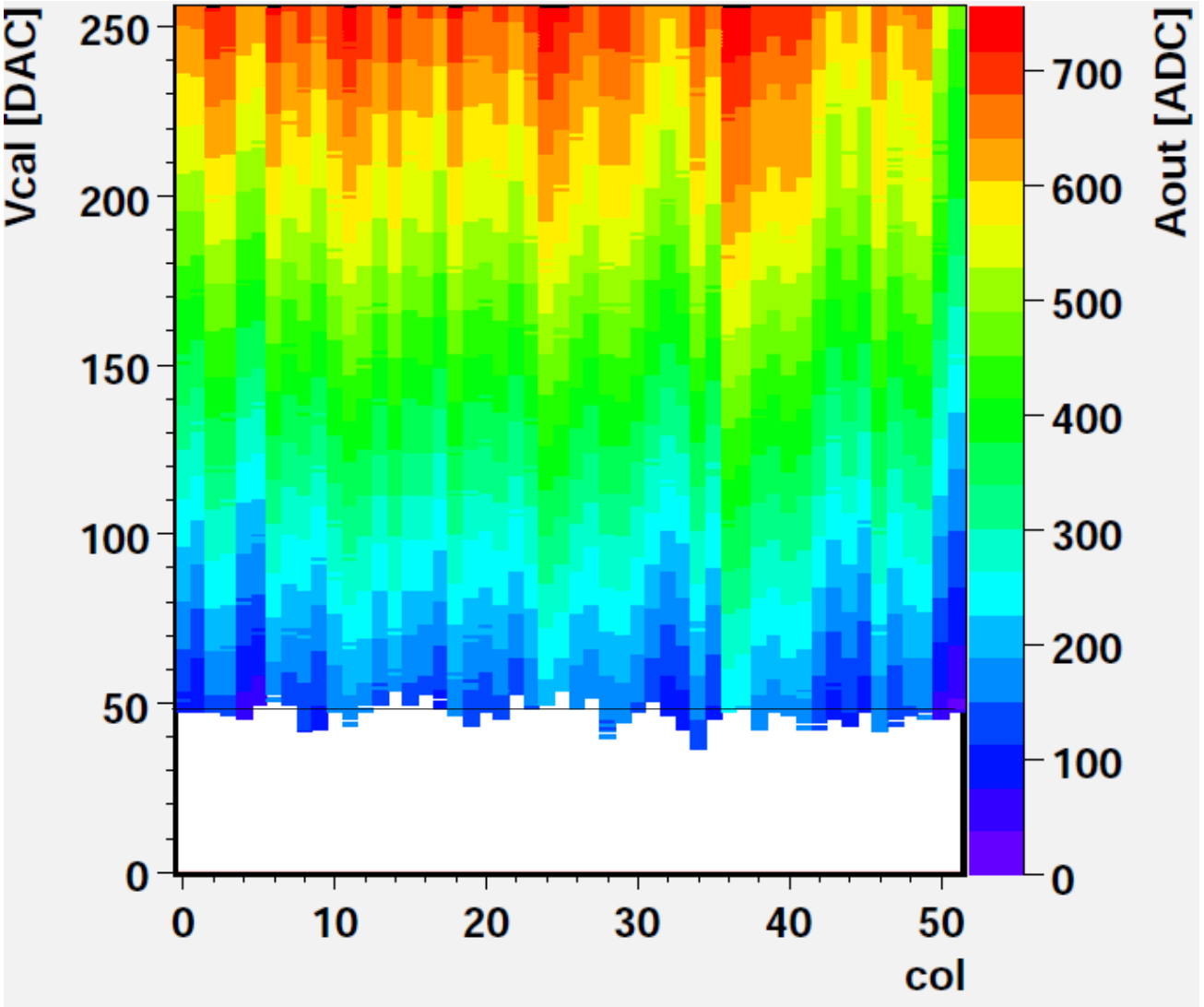
- Activate all 4160 pixels!
- Take random trigger (50 Hz).
- Count pixels.
- Scan threshold.
- Chip is quiet for thresholds below 130.
- 2 noisy regions around 138 and 166.
- Comparator does not work for thresholds above 180.

Noise map



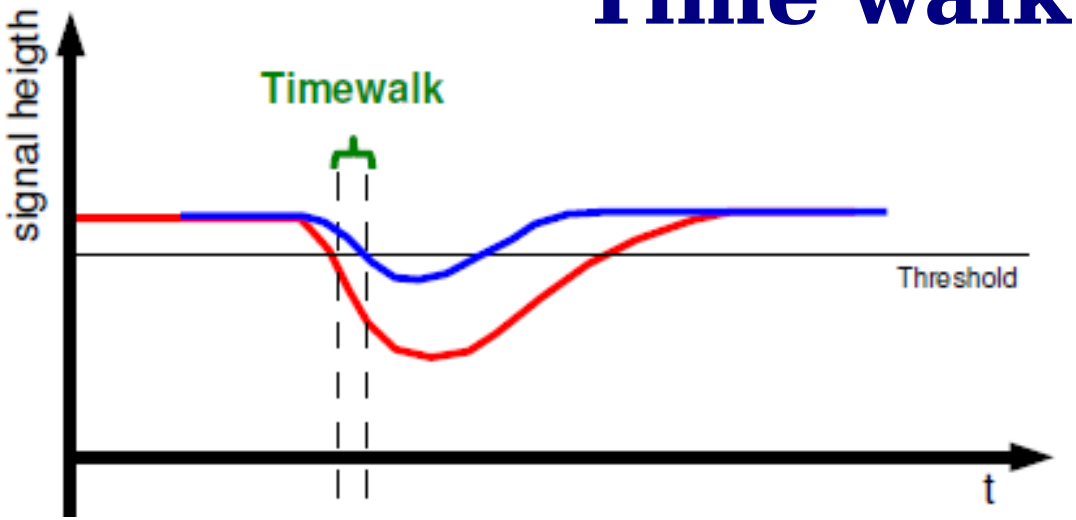
- Activate all 4160 pixels!
- Take random trigger (50 Hz).
- Scan threshold.
- Decode pixel address.
- White regions are quiet?
- Even-odd column pattern?
- Noisy regions vary with threshold.

Threshold variation

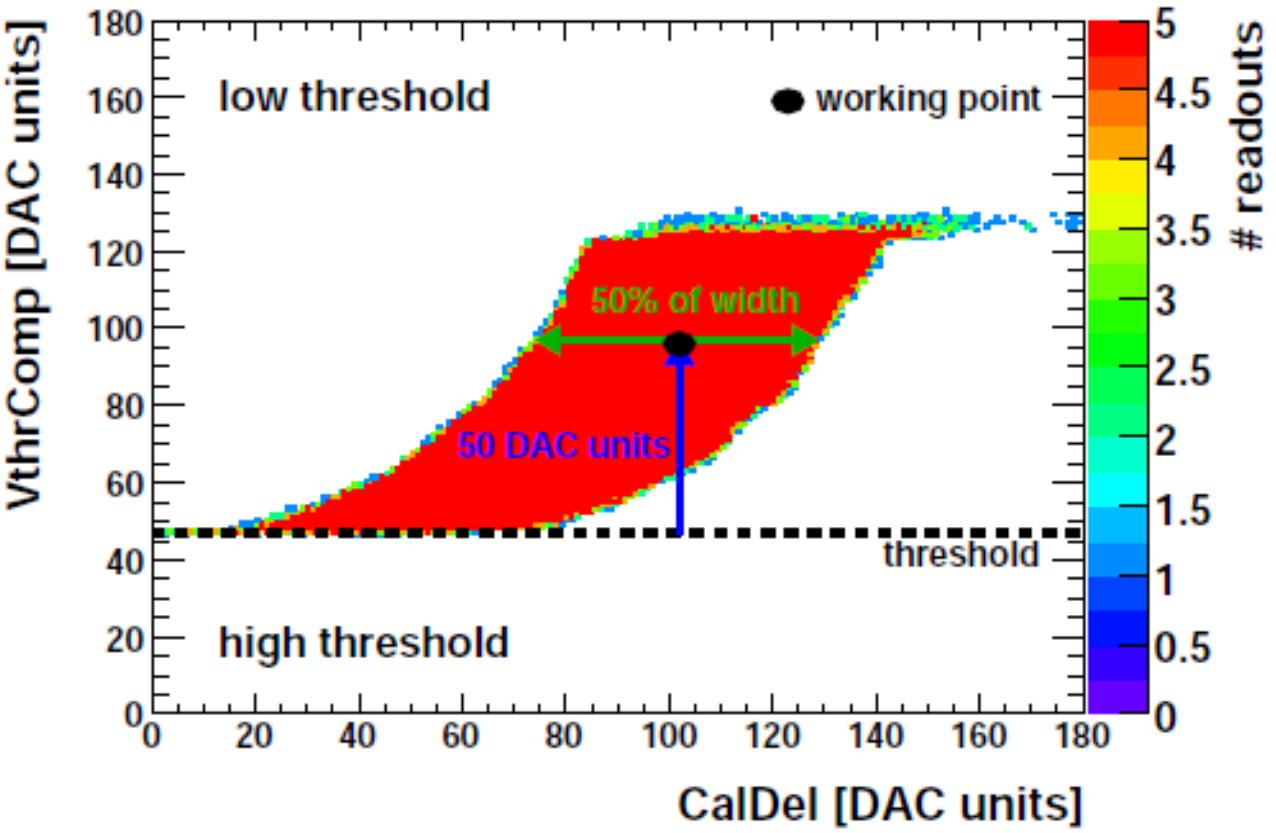


- Vcal scan for pixel 4 in each column 0..51.
- White region: no signal.
- Threshold varies by about ±5 DAC:
  - spread can be reduced by trimming.
- Columns 50, 51 have low gain.
  - systematic feature?

Time walk at PSI



- A
  - t
- L



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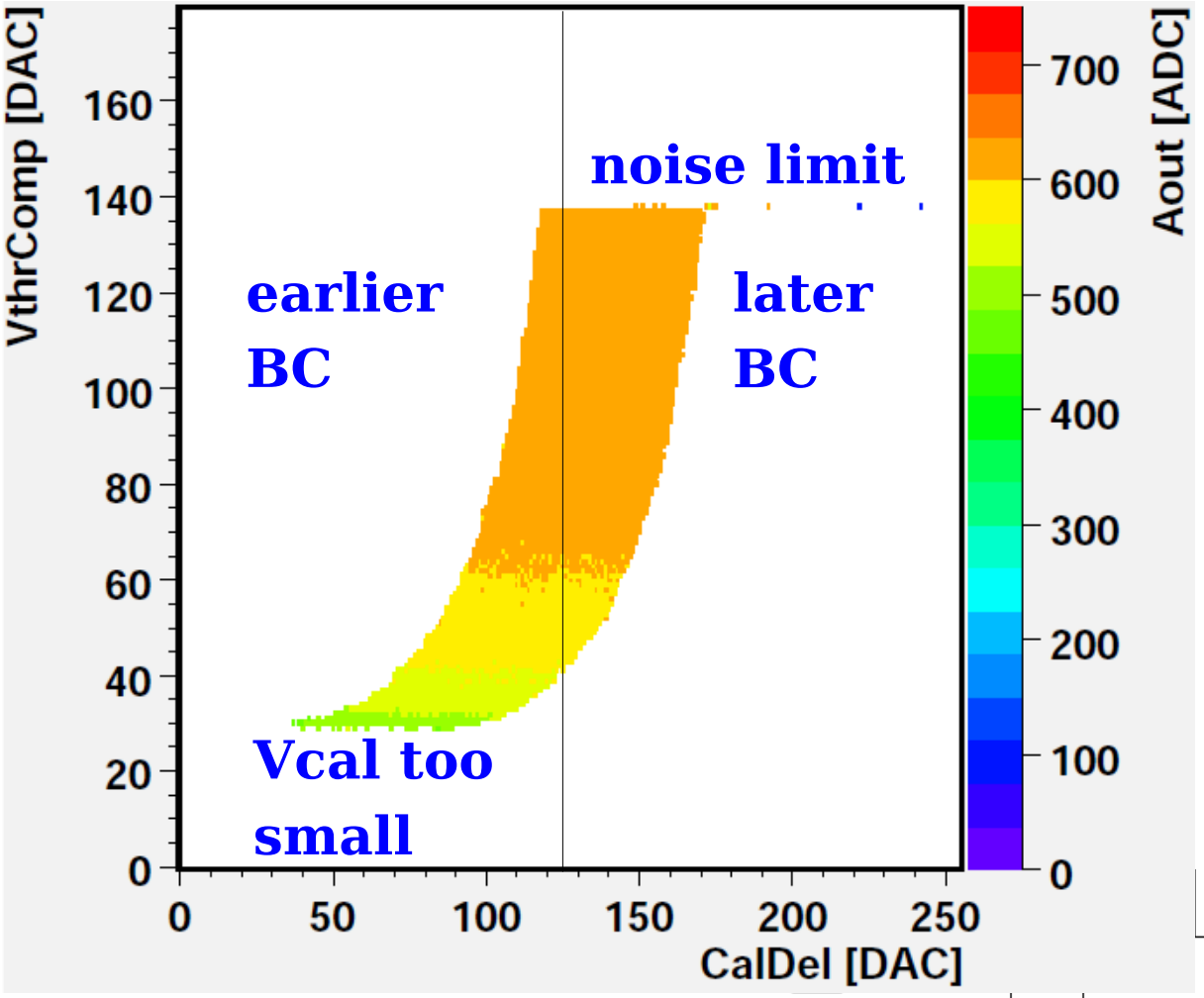
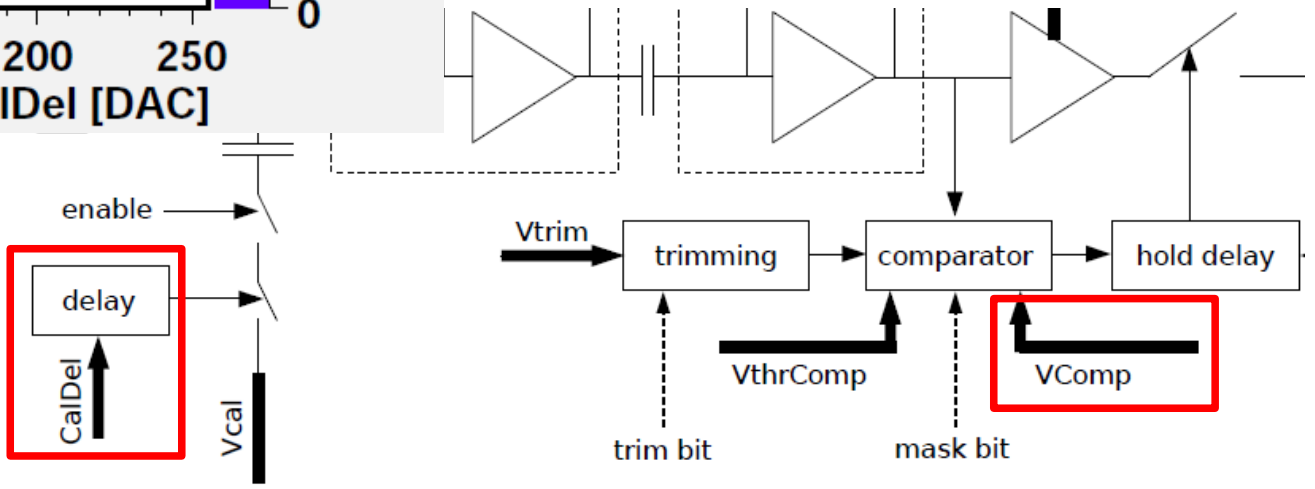
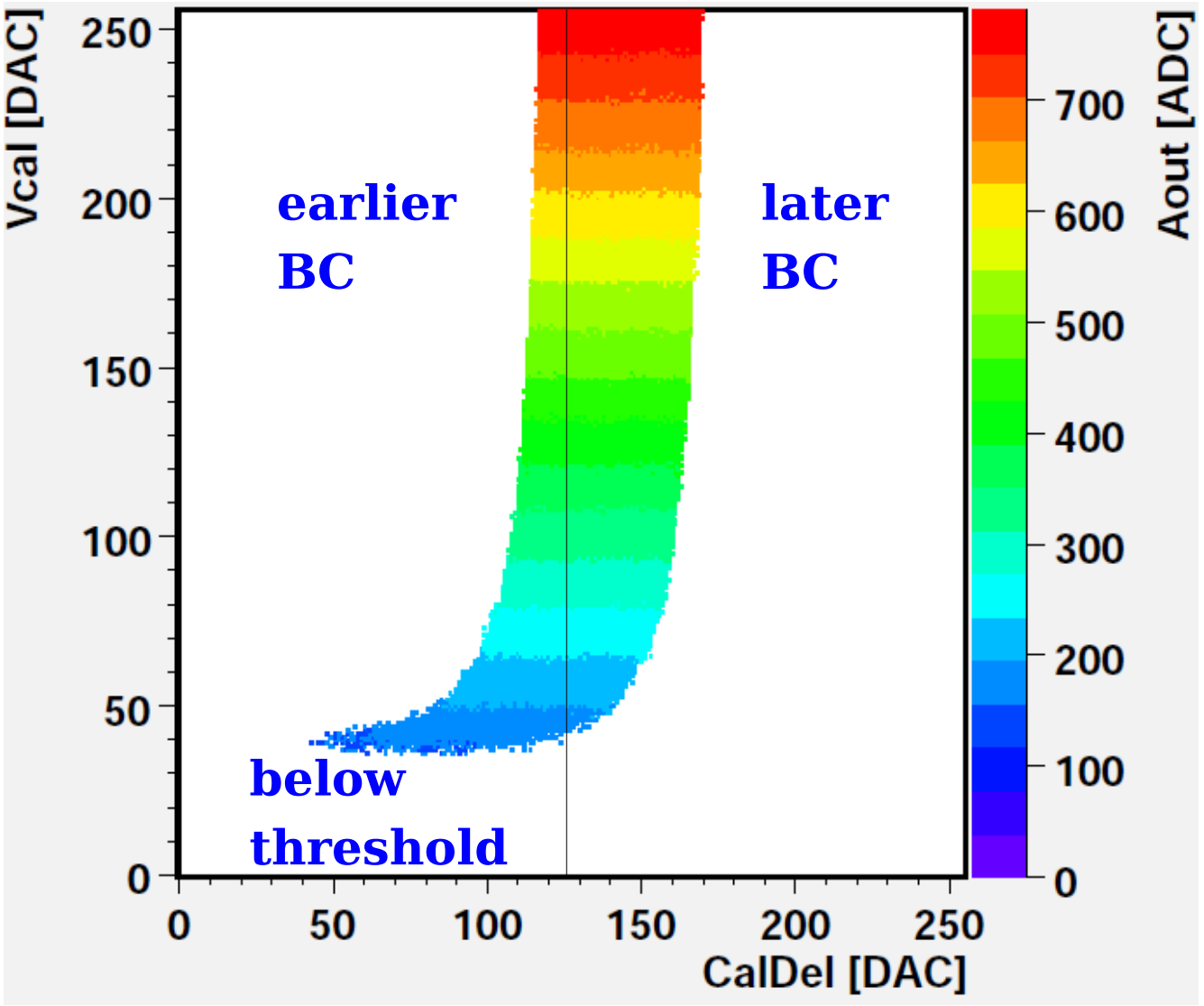
Time walk

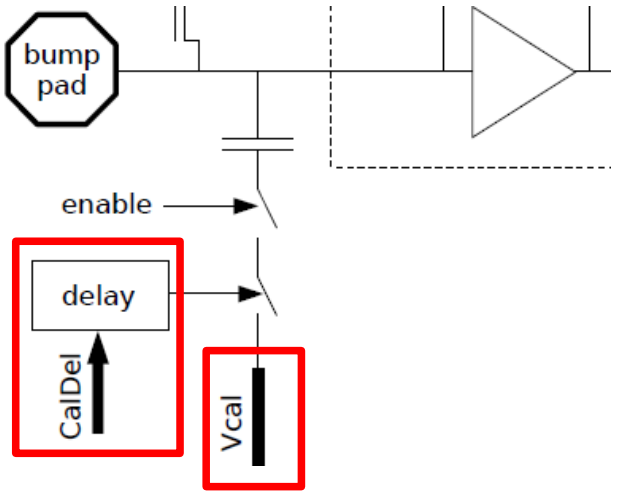


- One pixel.
- Vcal 200 small DAC.
- Moving the threshold shifts the timing:
  - time walk.



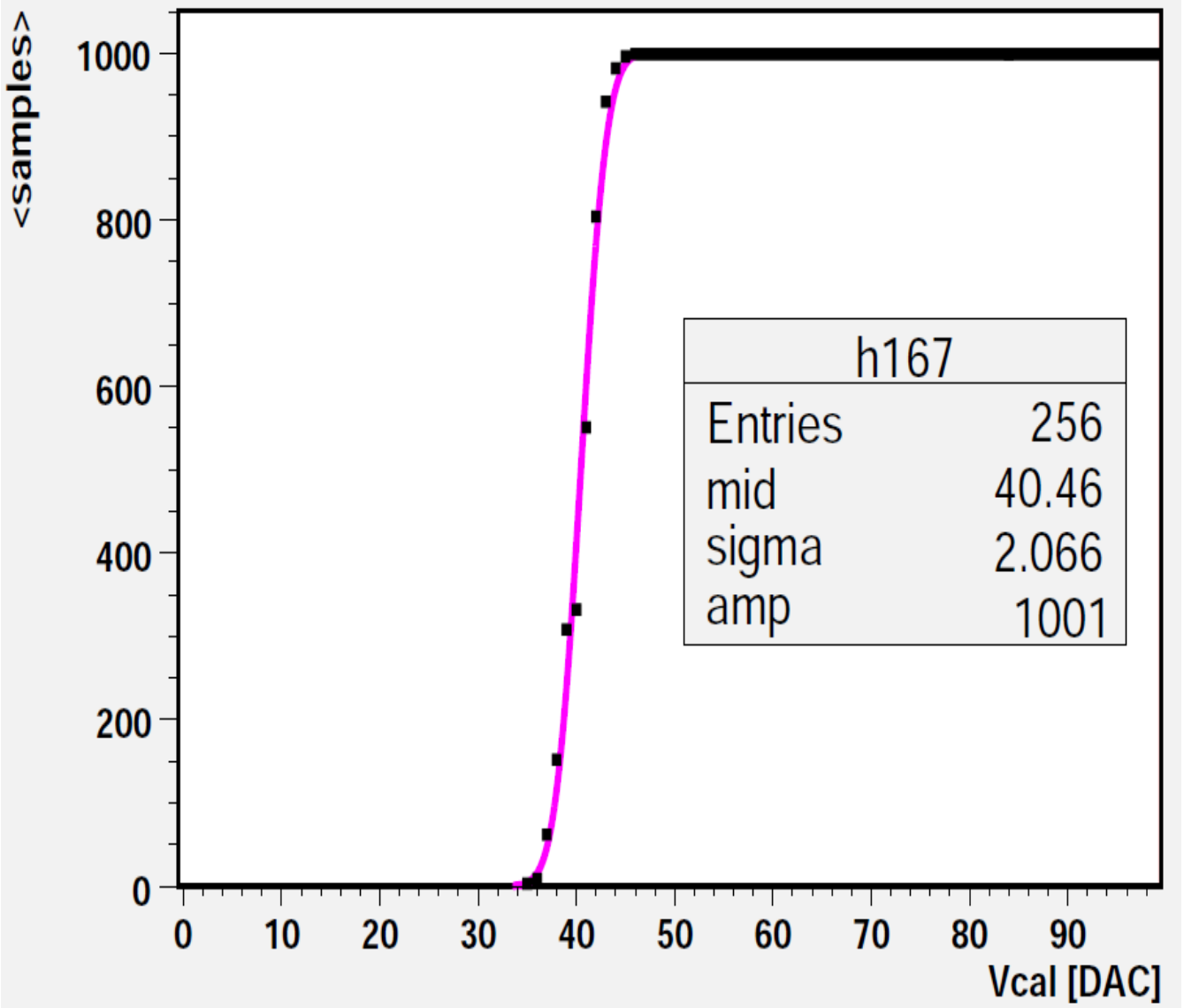
Calibrate timing





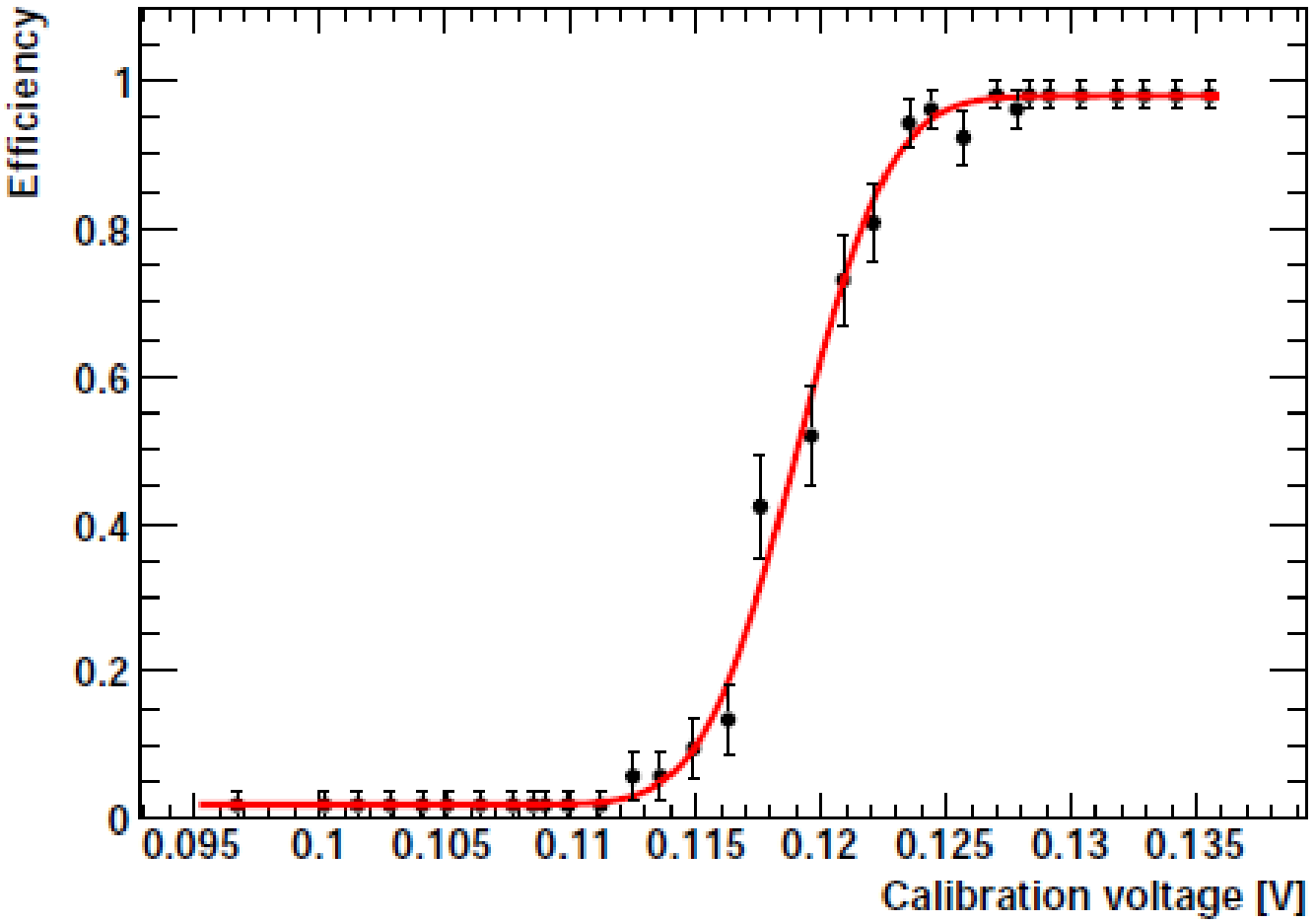
- One pixel.
- Threshold set close to noise limit.
- Window is 1 BC wide.
- We choose 125.
- Small pulses:
  - time walk.

Threshold curve



- One pixel.
- Fixed threshold
- Scan Vcal
  - 999 times
- count valid readouts
- threshold curve:
  - error function
  - width = noise
  - noise = 2.1 DAC
  - = 130 electrons.
  - (bare chip without sensor).

Threshold curve at PSI



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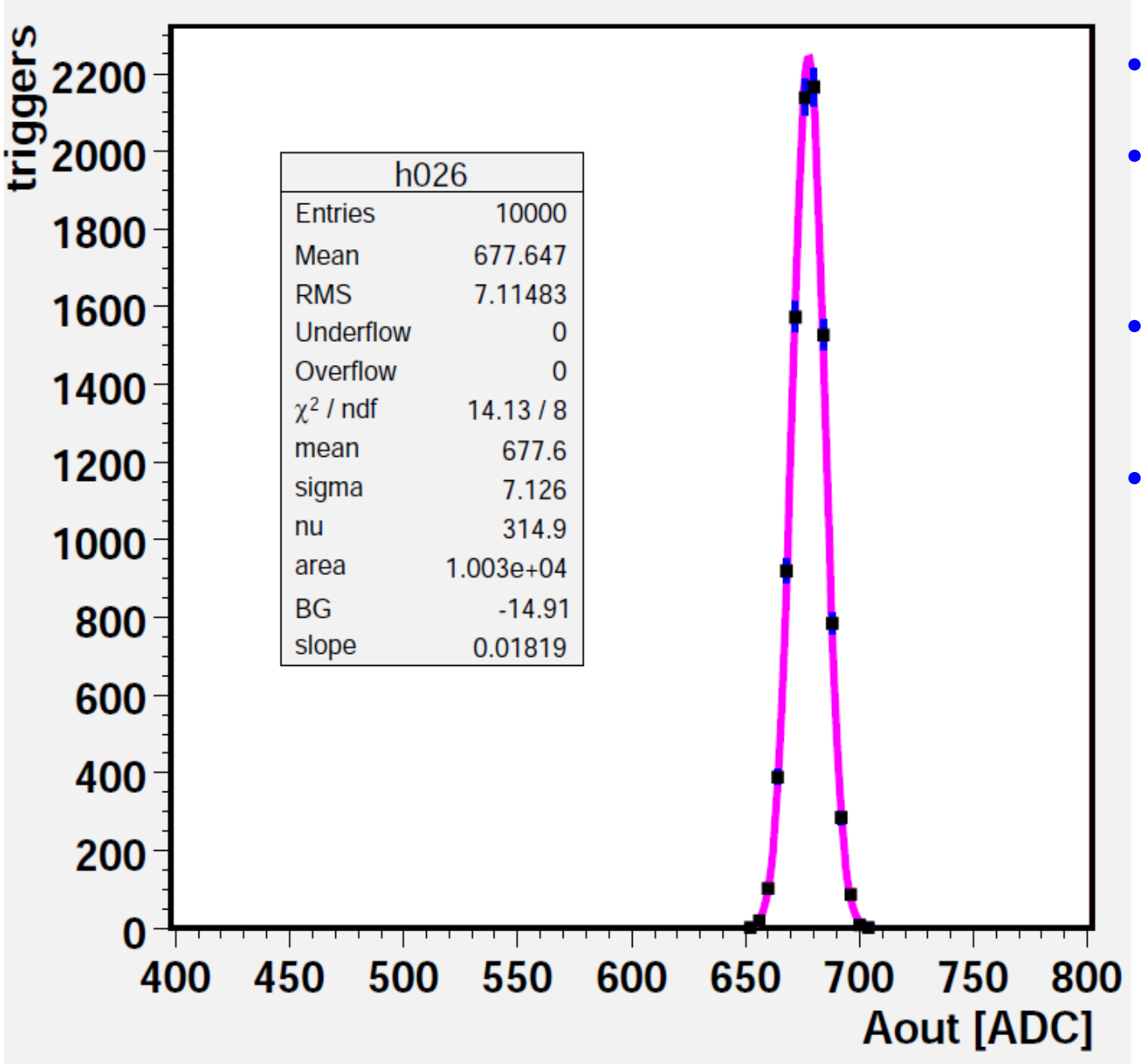
one pixel with test pulse

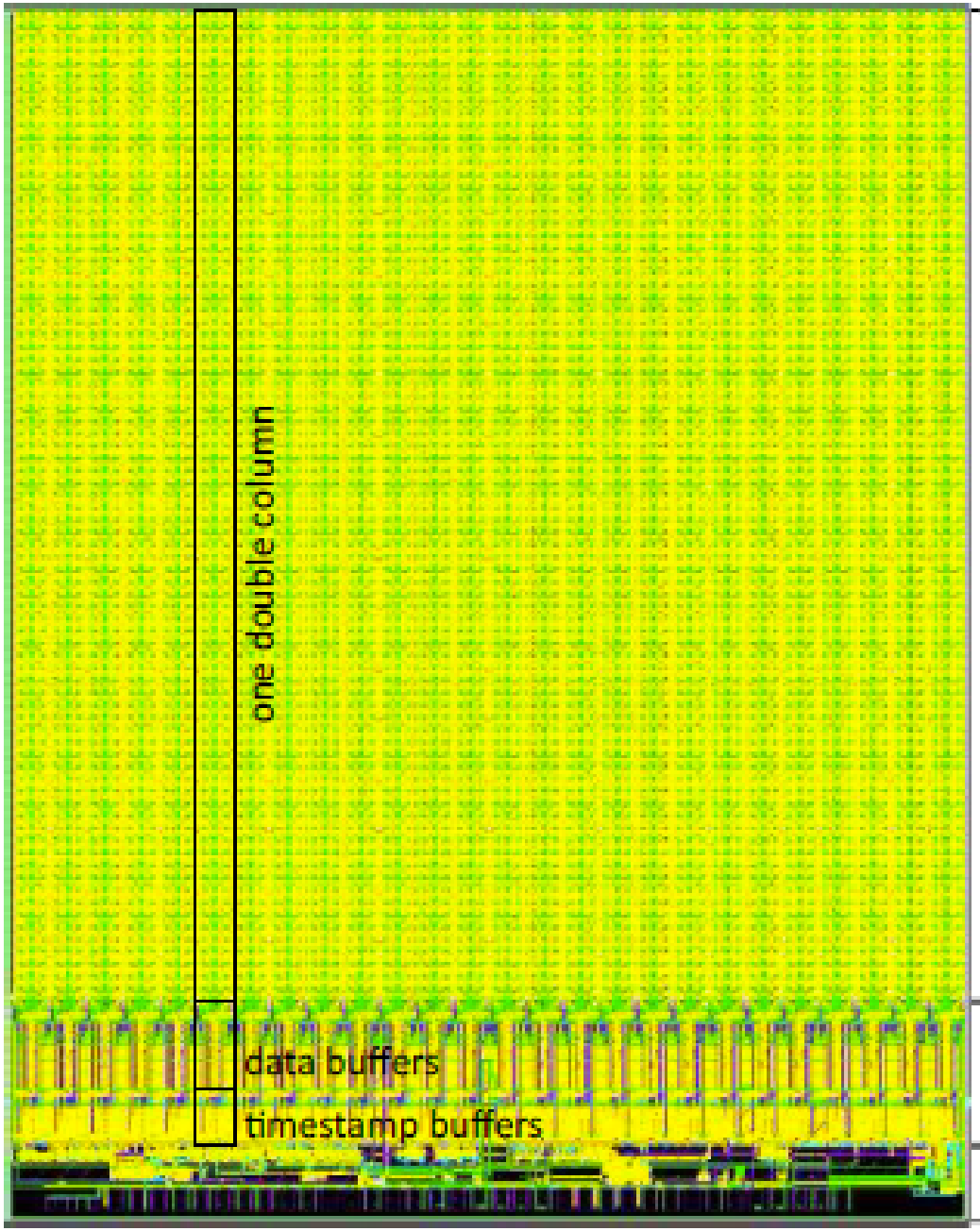


- one pixel.
- 10k triggers:
  - at 100 Hz = 100 s.
- Calibrate 200 small DAC = 13'000 e (PSI).
- Width = 7 ADC counts:
  - thermal noise,
  - perfect Gaussian,
  - 135 e (no sensor).
  - agrees with threshold scan!

Summary

- Progress in understanding the psi46 readout chip (without sensor):
  - operation range explored: timing, thresholds, voltages.
  - several results are similar to PSI measurements.
  - several correlations among the 26 DACs observed
  - working point established, may need fine tuning.
- Large variations from chip to chip (not shown today)
  - need automated 'bootstrap' procedures for finding a working point.
- Further:
  - More data analysis (reduction): linearity, threshold, noise.
  - Activate threshold trimming algorithm (solve FPGA problem).
  - Test chip with sensor.
  - Develop (activate) bump bonding tests.

psi46



pixel array:
52 columns × 80 rows
(4160 pixels)

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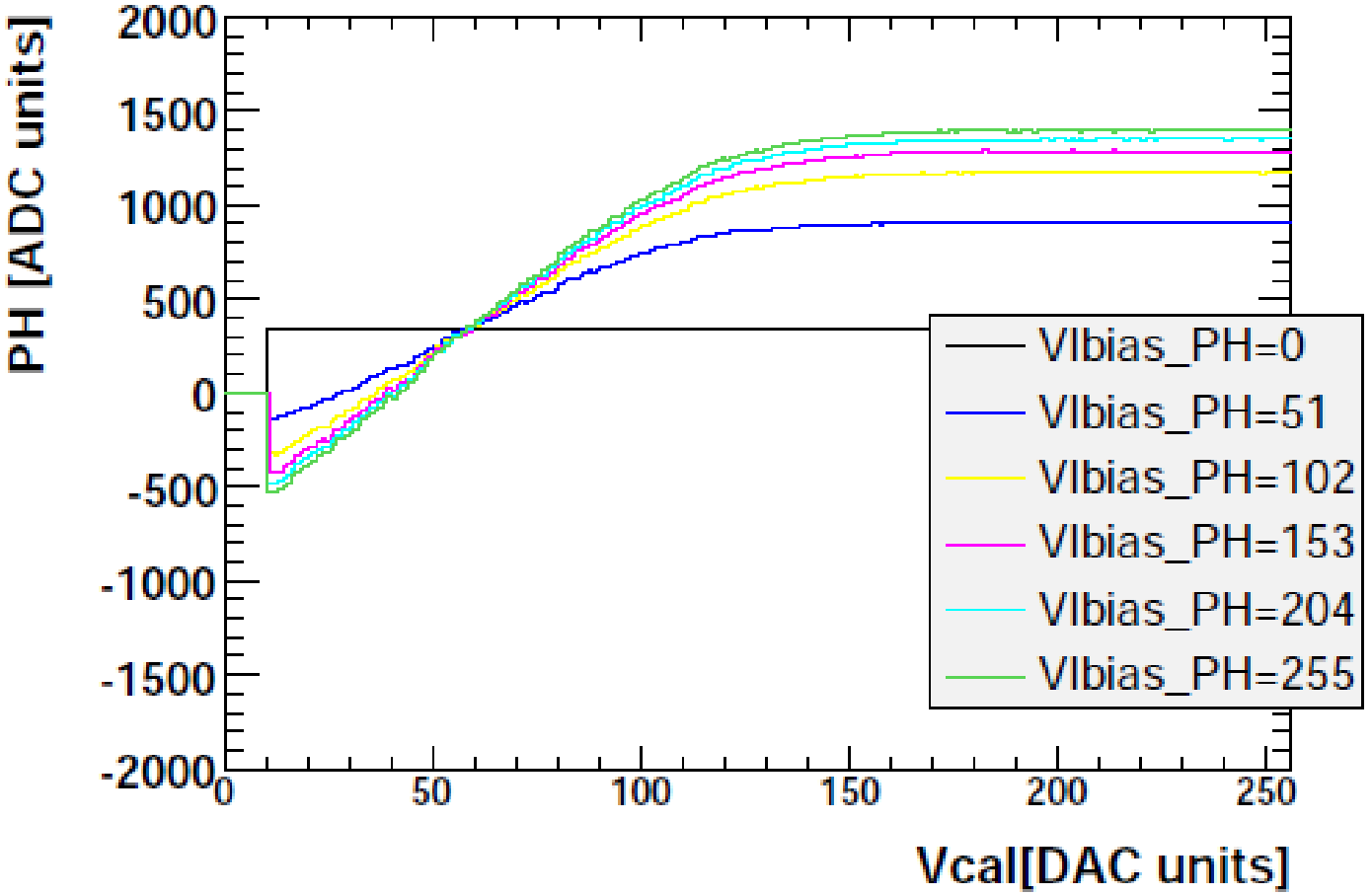
double column periphery

chip periphery

PH output driver



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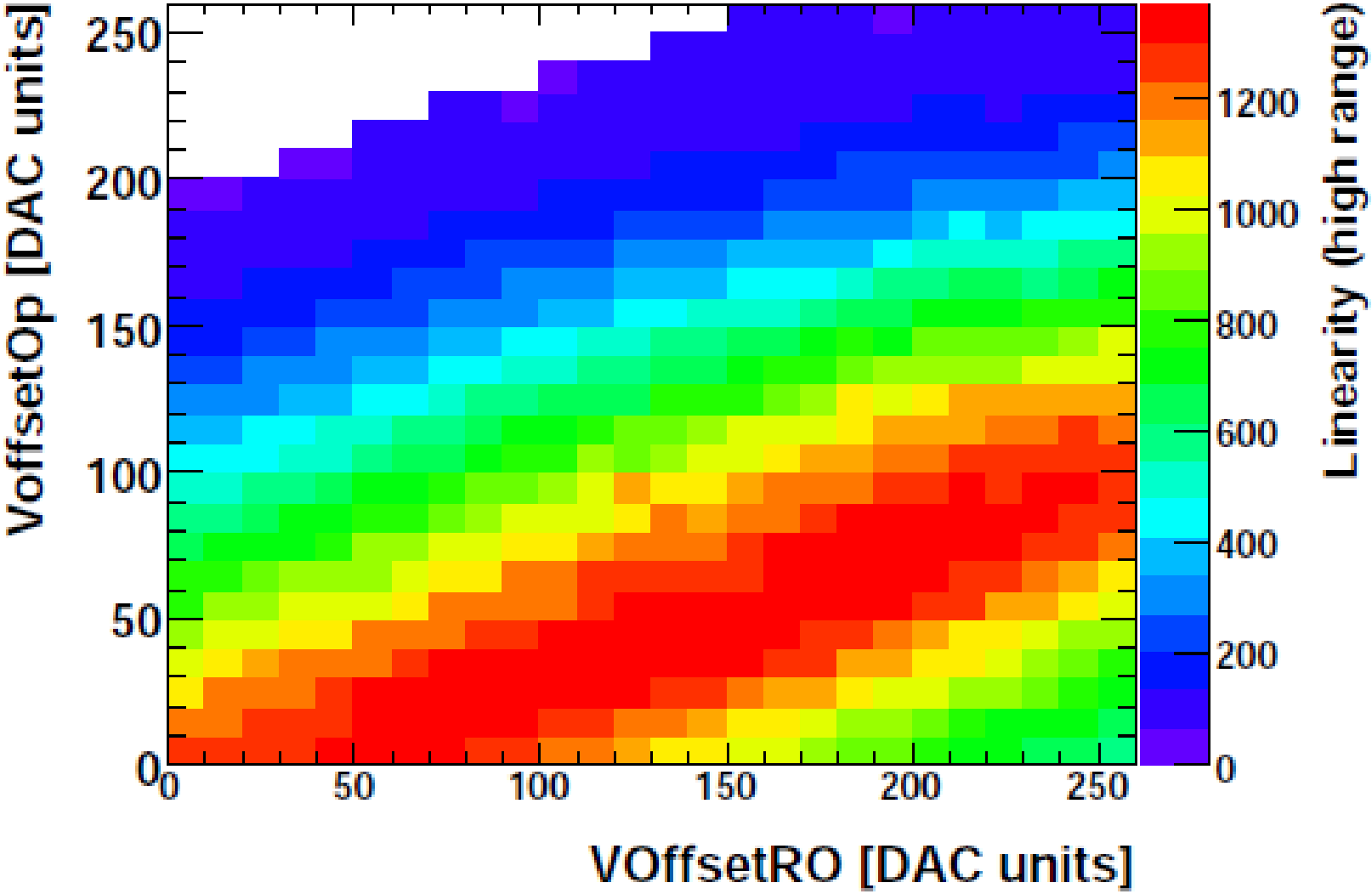
Linear range vs offsets



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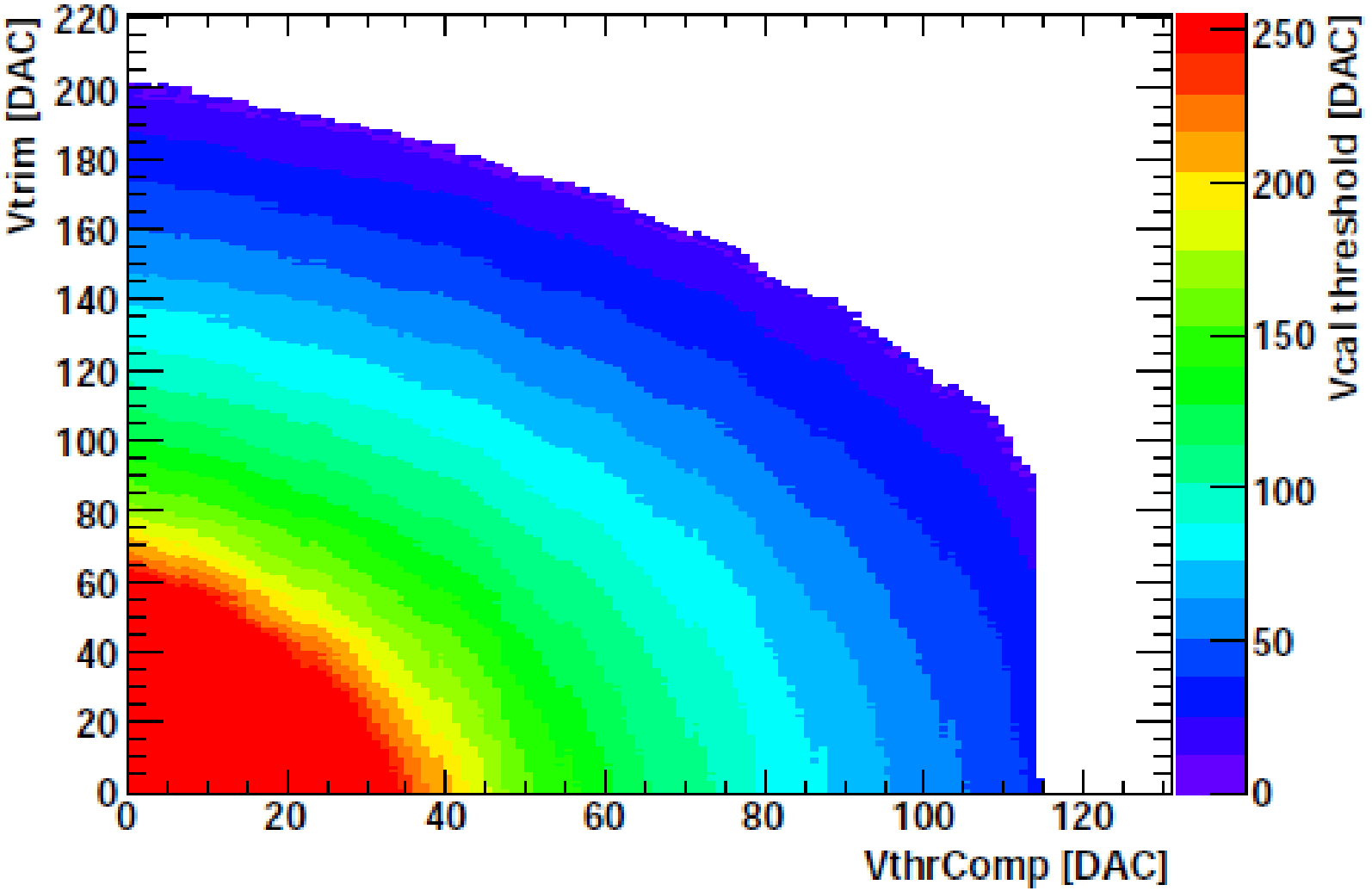
Threshold vs trim voltages



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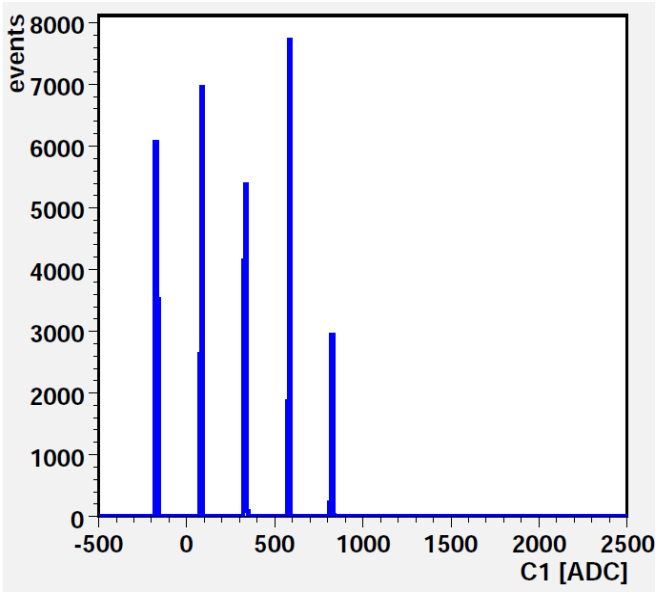
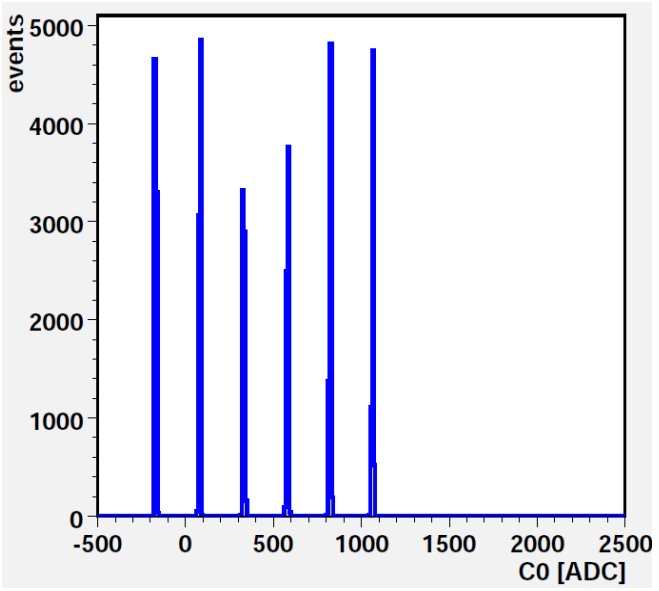
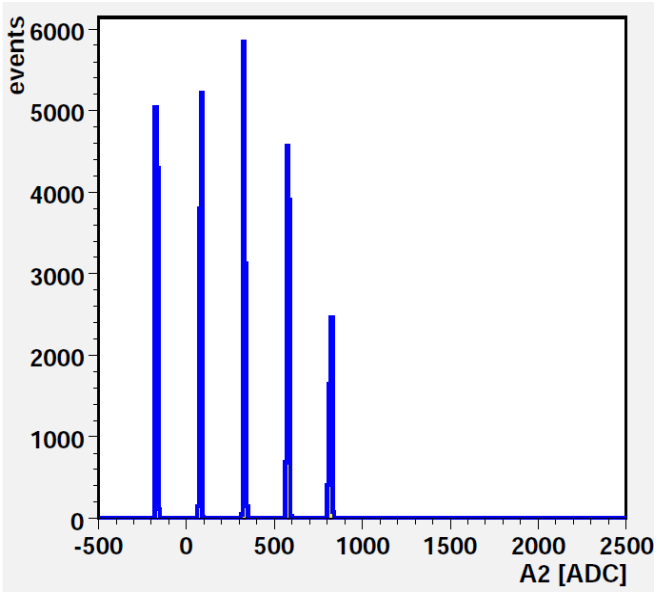
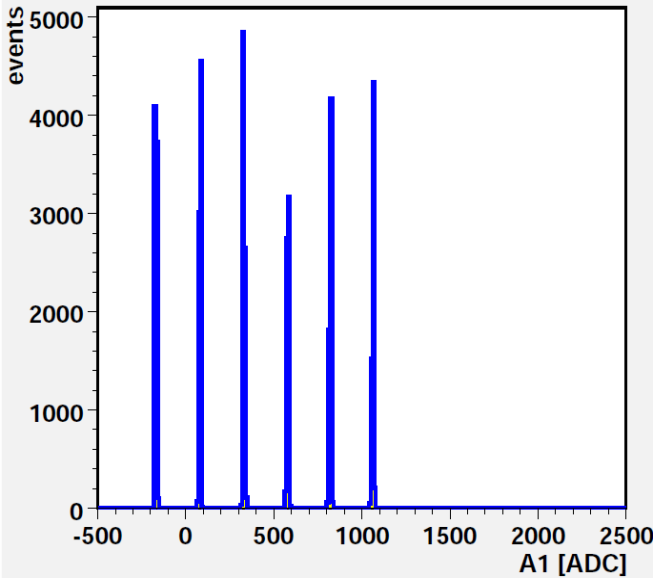
Pixel address

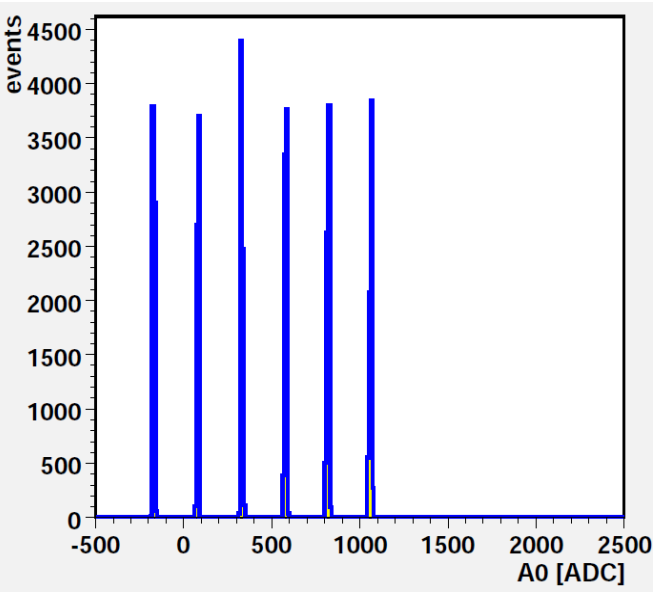




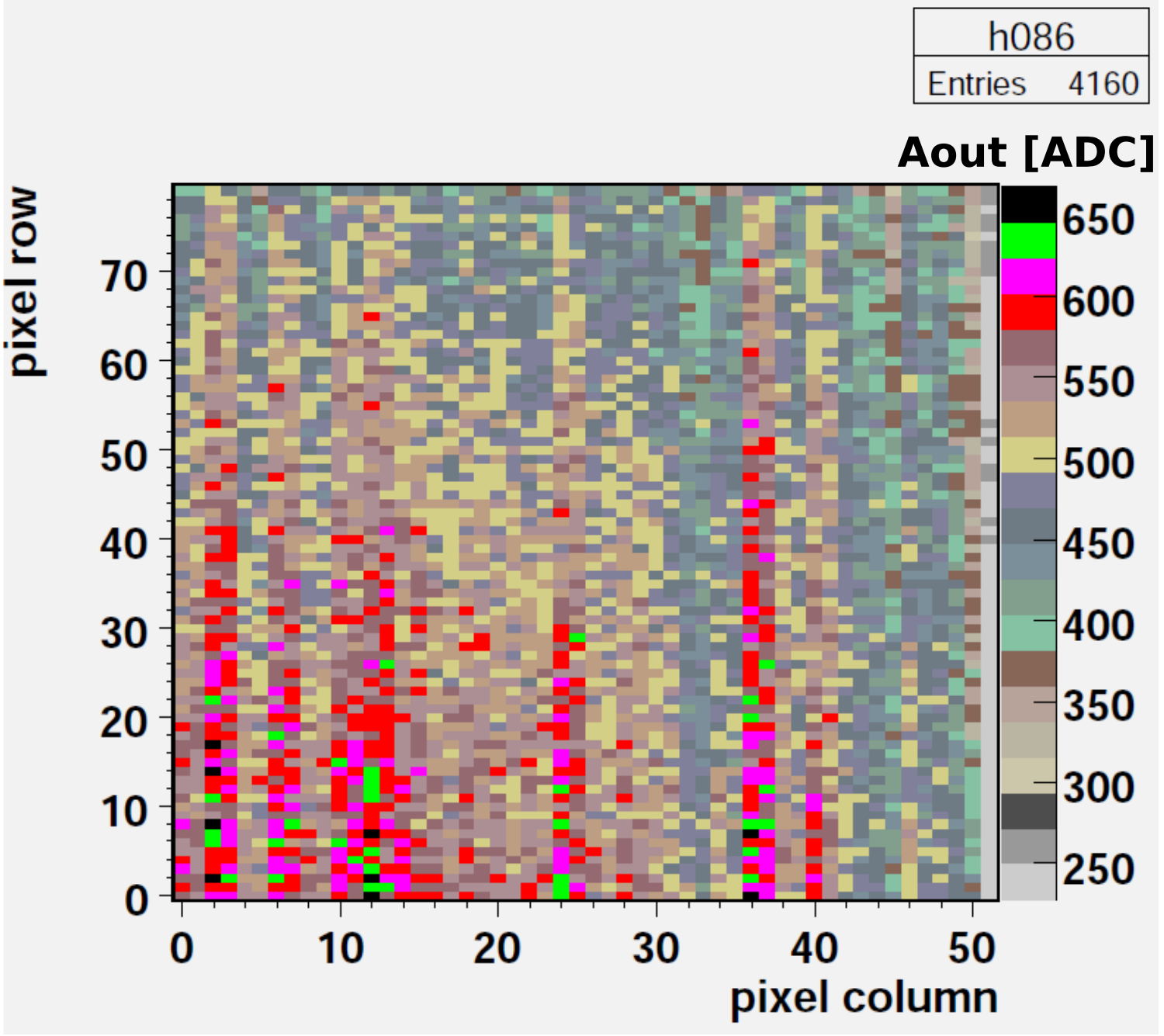
Pixel address in 5 data:
C1,C0 d-columns 0..25
A2, A1, A0 rows 0..159
each with 6 analog levels (2.5 bit).
All well separated.







Pixel map



- 52 × 80 = 4160 pixel per chip.
- Vcal = 200 DAC
- VthrComp = 80
- Strong pulse height variation:
  - gain?
  - timing?