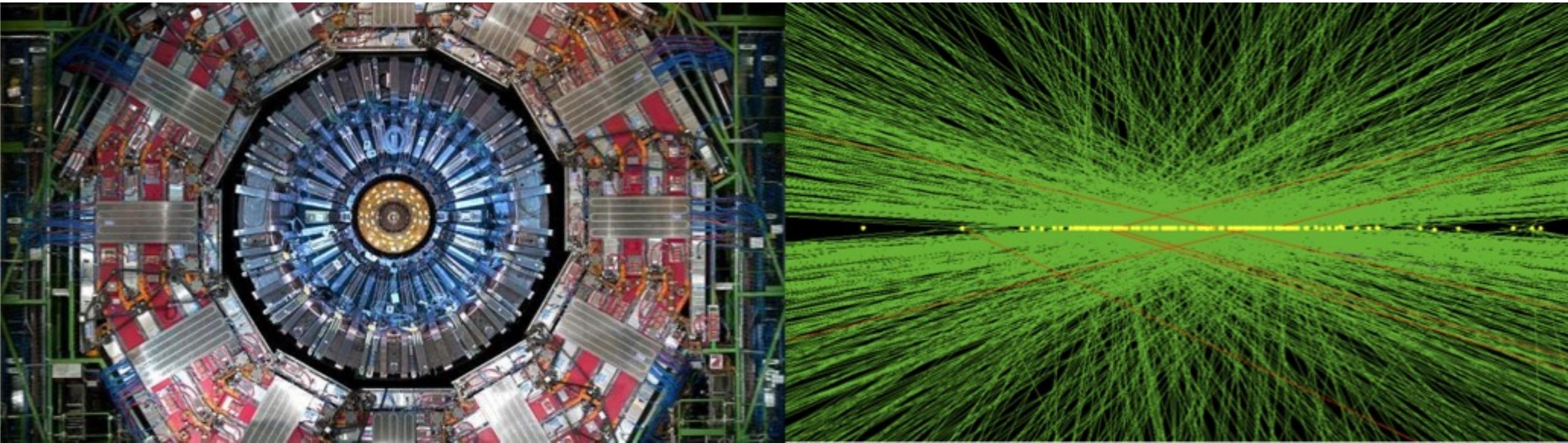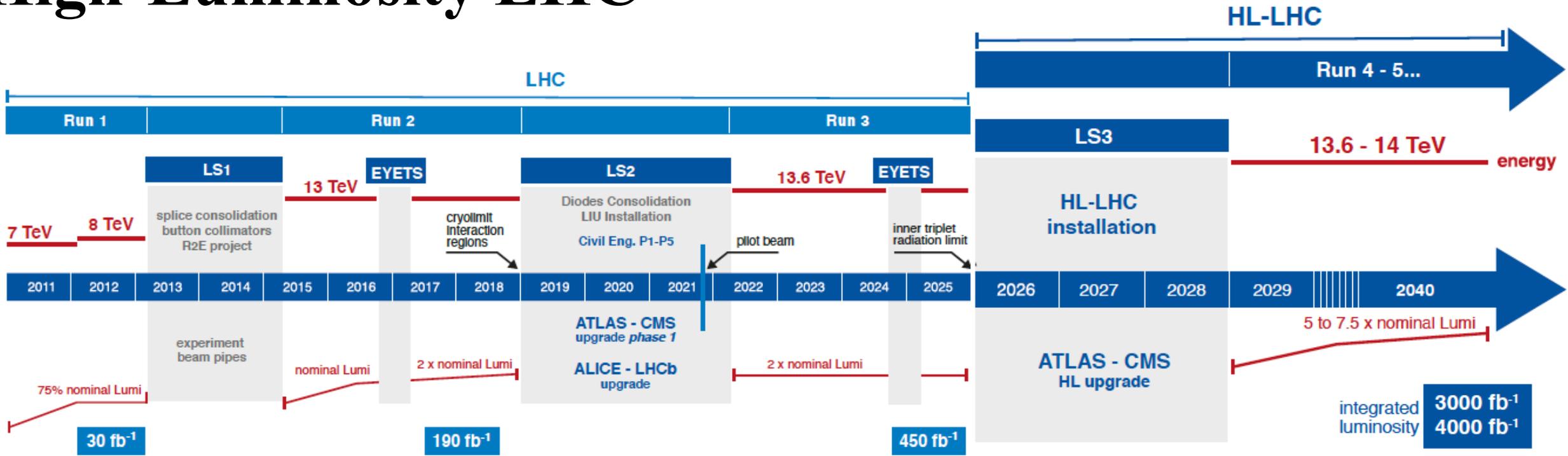# Precision Timing at HL-LHC with the CMS MTD Endcap Timing Layer

Zhenyu Ye @ University of Illinois at Chicago
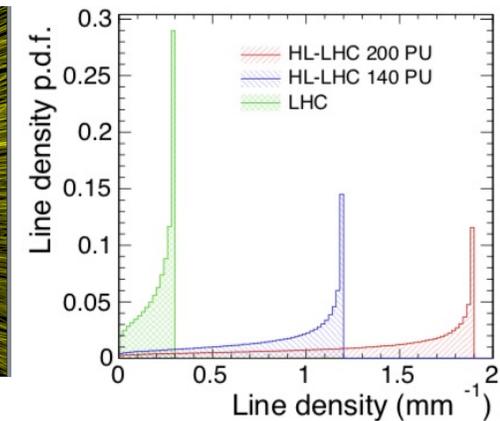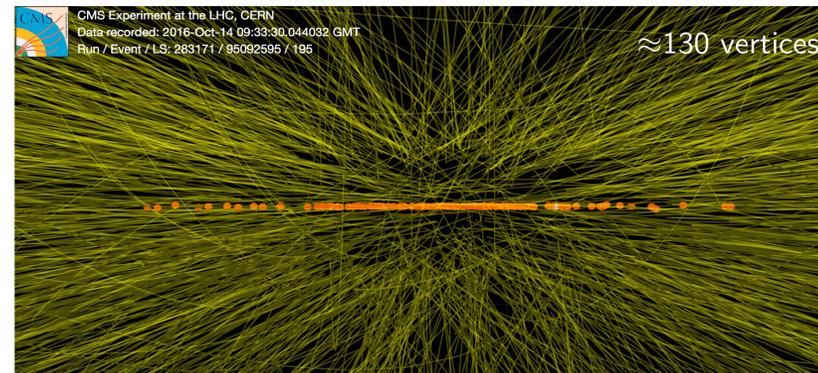
on behalf of CMS collaboration

High-Luminosity LHC

The HL-LHC will have x3-4 instantaneous and x10 integrated luminosity, requiring **detector upgrades** to
- deal with enhanced pileup interaction and radiation damage levels at the HL-LHC
- improve the experiment for better discovery potential and/or measurement precision

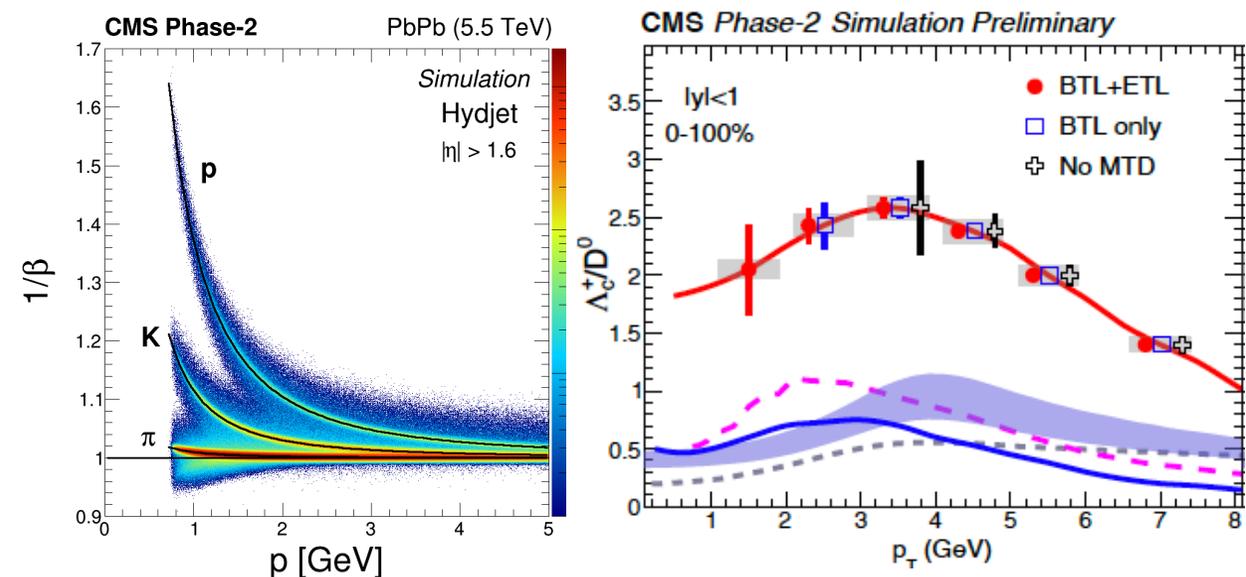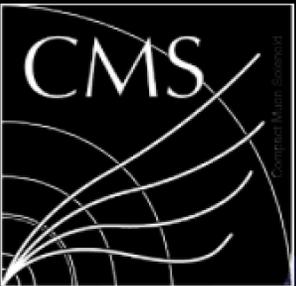# Role of Precise Timing at HL-LHC

Vertices significantly overlap in space but more separable in space + time
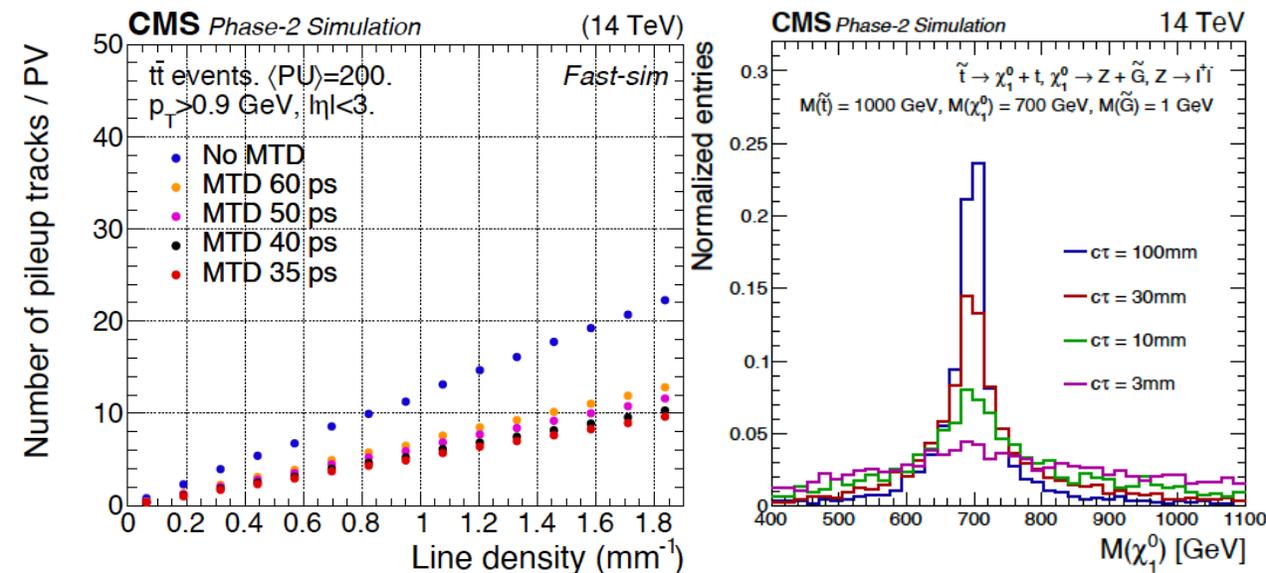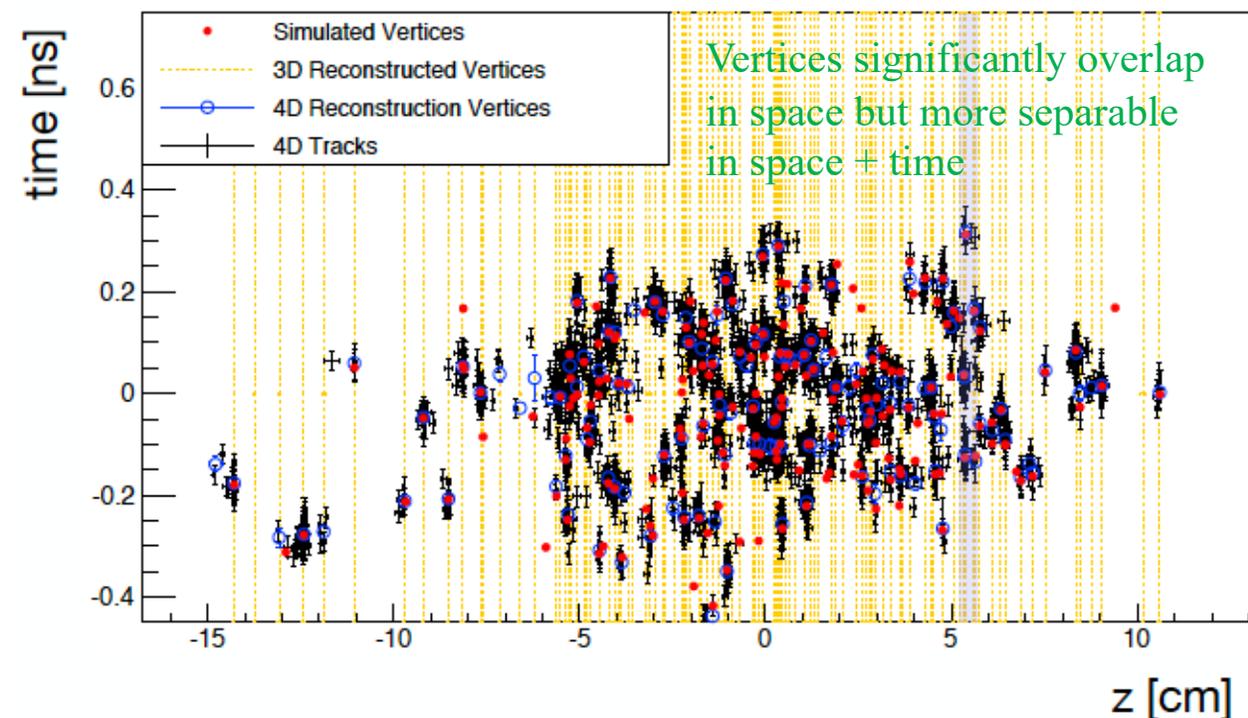
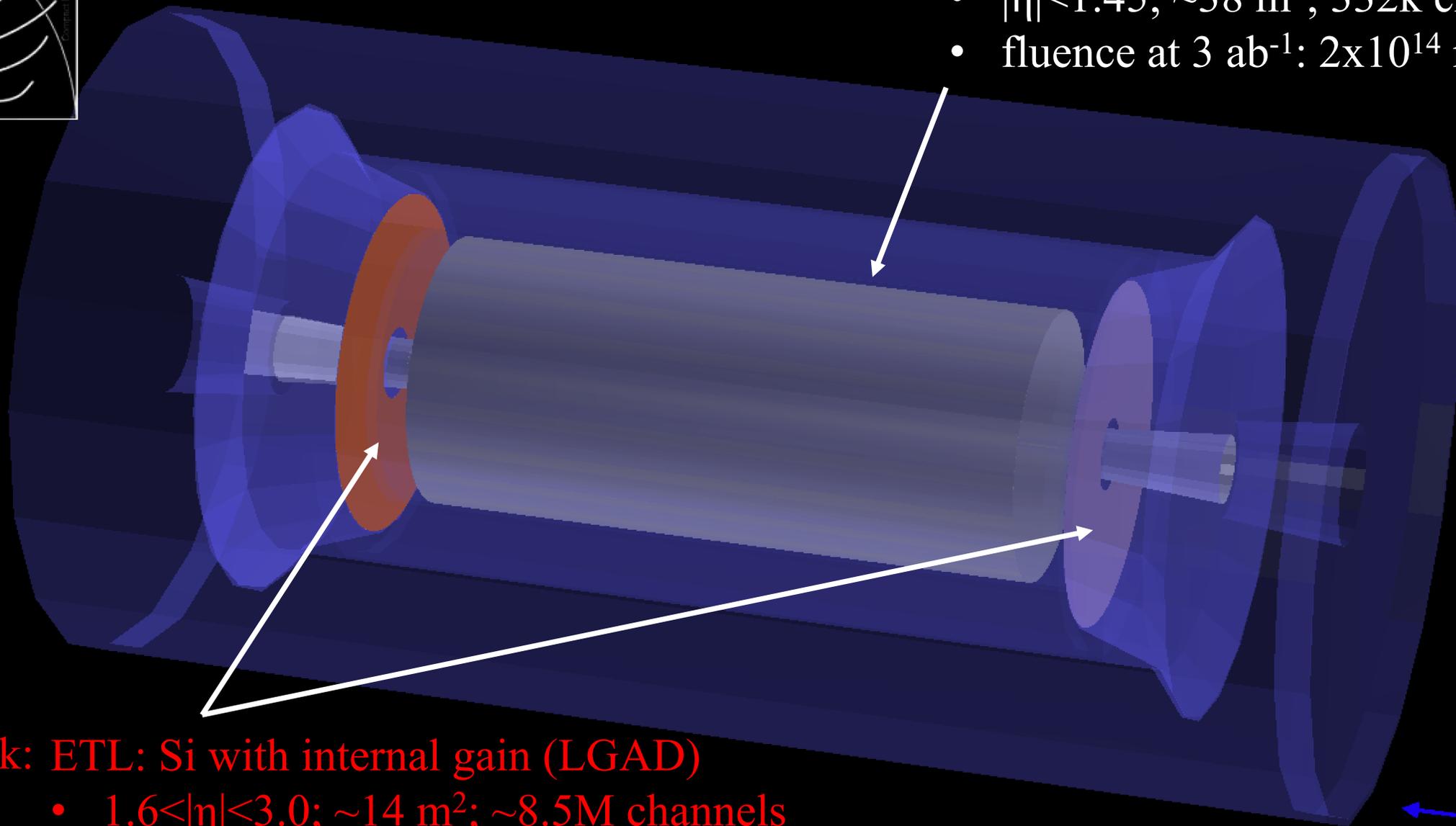Per-particle precise timing allows 4D track and vertex reconstruction, which
- reduce pile-up contributions and improve object reconstructions
- provide new physics opportunities for LLP search, heavy ion, etc

BTL: LYSO bars + SiPM
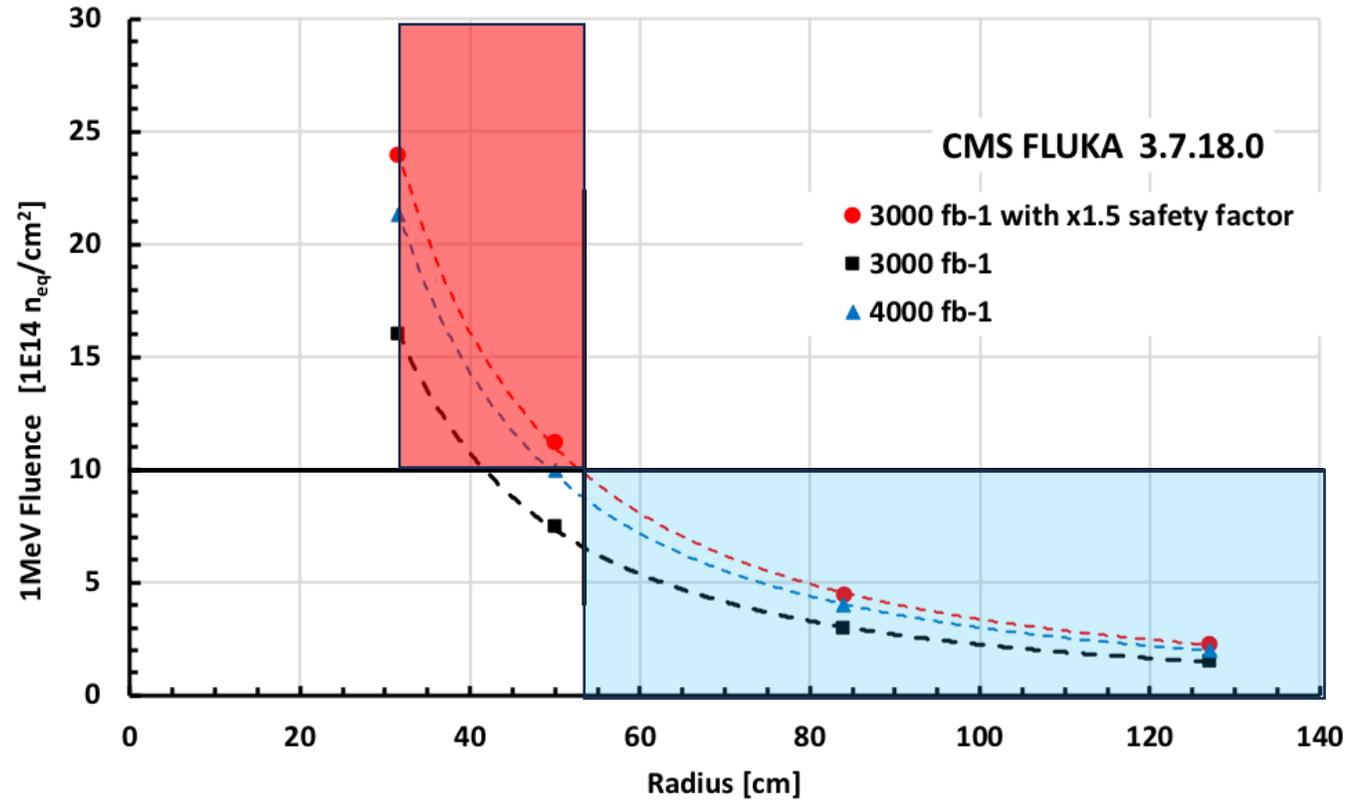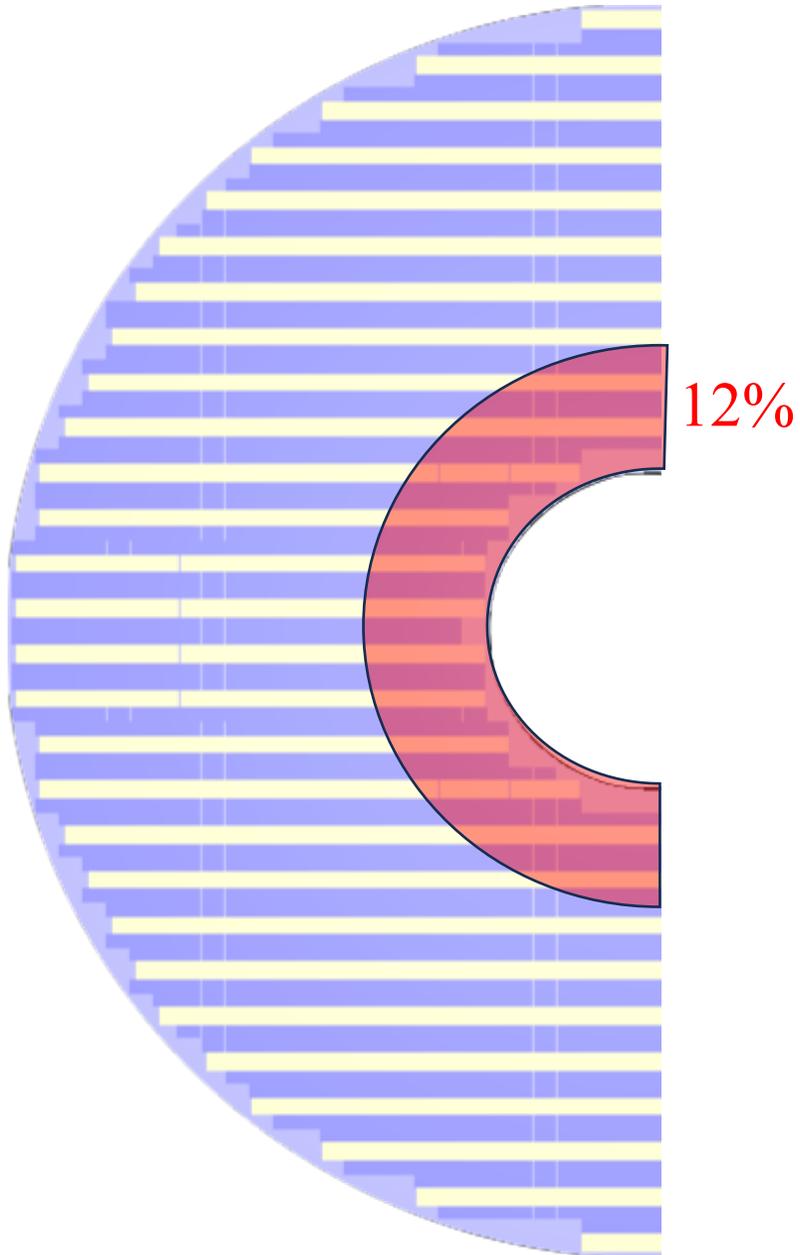- $|\eta|<1.45$; ~38 m^2; 332k channels
- fluence at 3 ab^{-1}: 2×10^{14} n_{eq}/cm^2

This talk: ETL: Si with internal gain (LGAD)
- $1.6<|\eta|<3.0$; ~14 m^2; ~8.5M channels
- fluence at 3 ab^{-1}: ~2×10^{15} n_{eq}/cm^2

ETL Requirements

- **Time resolution**: <35 ps per track at the beginning of HL-LHC
- **Fill-factor** (ratio of active and total detector surface): >95%
- **Low occupancy**: <0.1% at low η, 1% at highest η
- **Radiation tolerance**: up to 1.7×10^{15} n_{eq}/cm^2
  - Only 12% of surface will reach higher fluences than 1×10^{15} n_{eq}/cm^2, where degradation begins

ETL Design
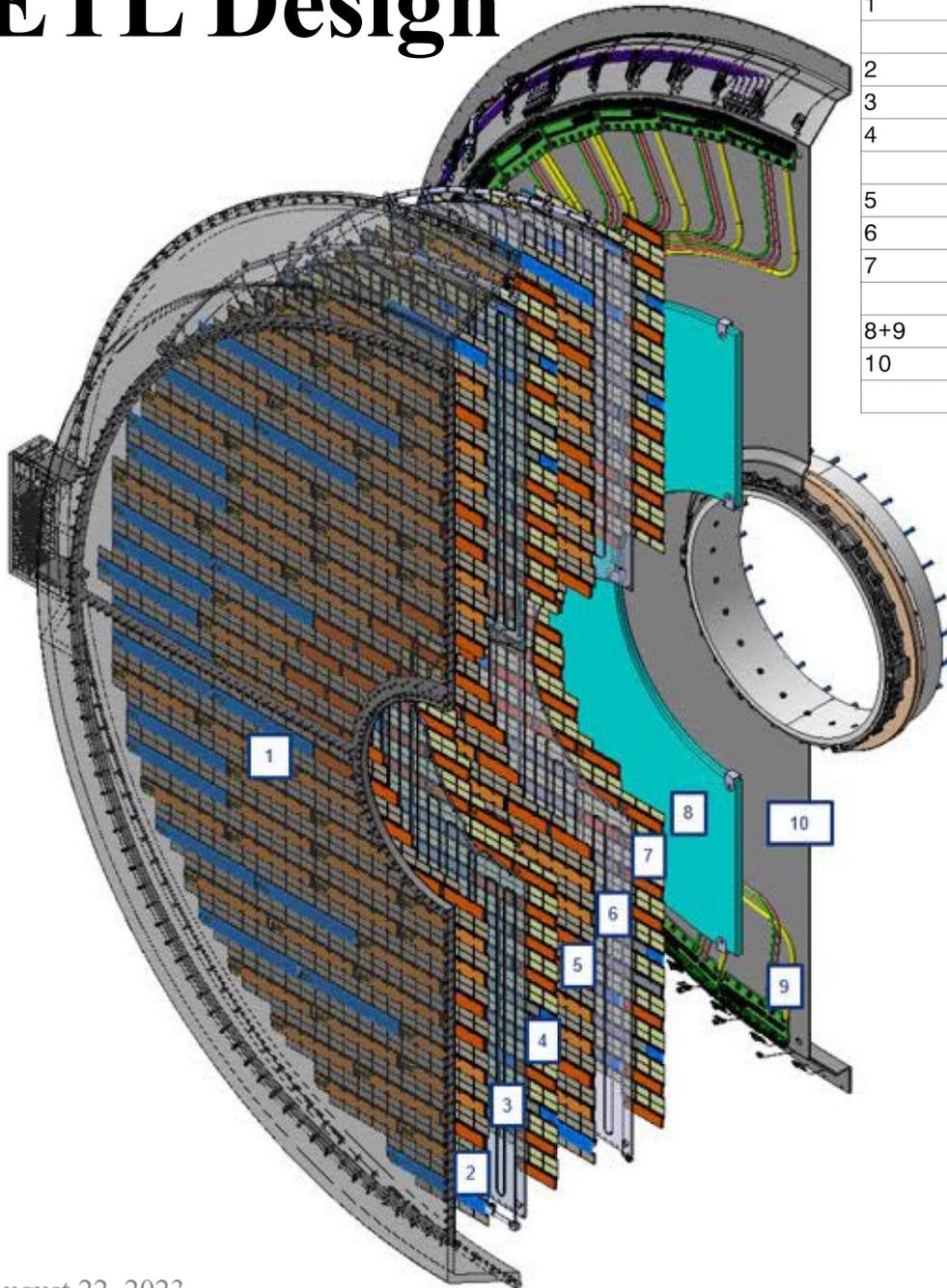
| Element	
1	Thermal screen
	Gap between thermal screen and Face 1
2	Face 1 - active layer
3	Front disc
4	Face 2 - active layer
	Gap between Face 2 and Face 3
5	Face 3 - active layer
6	Back disc
7	Face 4 - active layer
	Gap between Face 4 and ETL front moderator
8+9	Patch panels O + cables [9] + ETL front moderator
10	ETL back support plate
	Gap between ETL back support plate and CE thermal screen
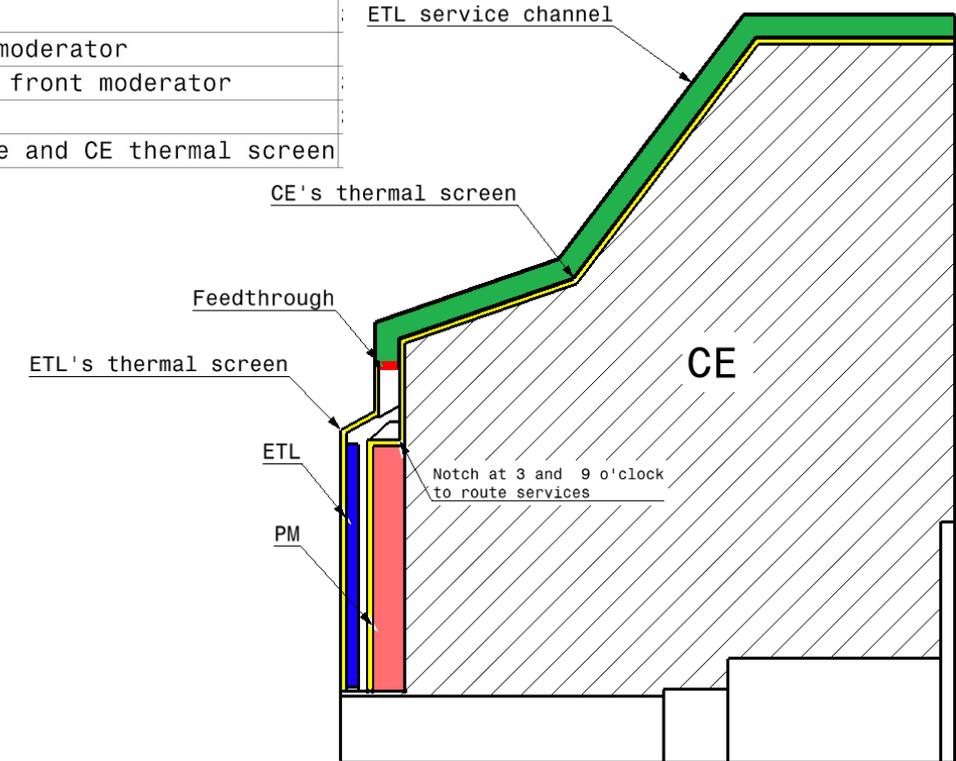
- Two ETL disks on each side allowing up to 2 measurements per track: <50 ps per hit → <35 ps per track
- Independent volume isolated and operated separately from HGCAL: stageable, serviceable, maintainable

ETL Design
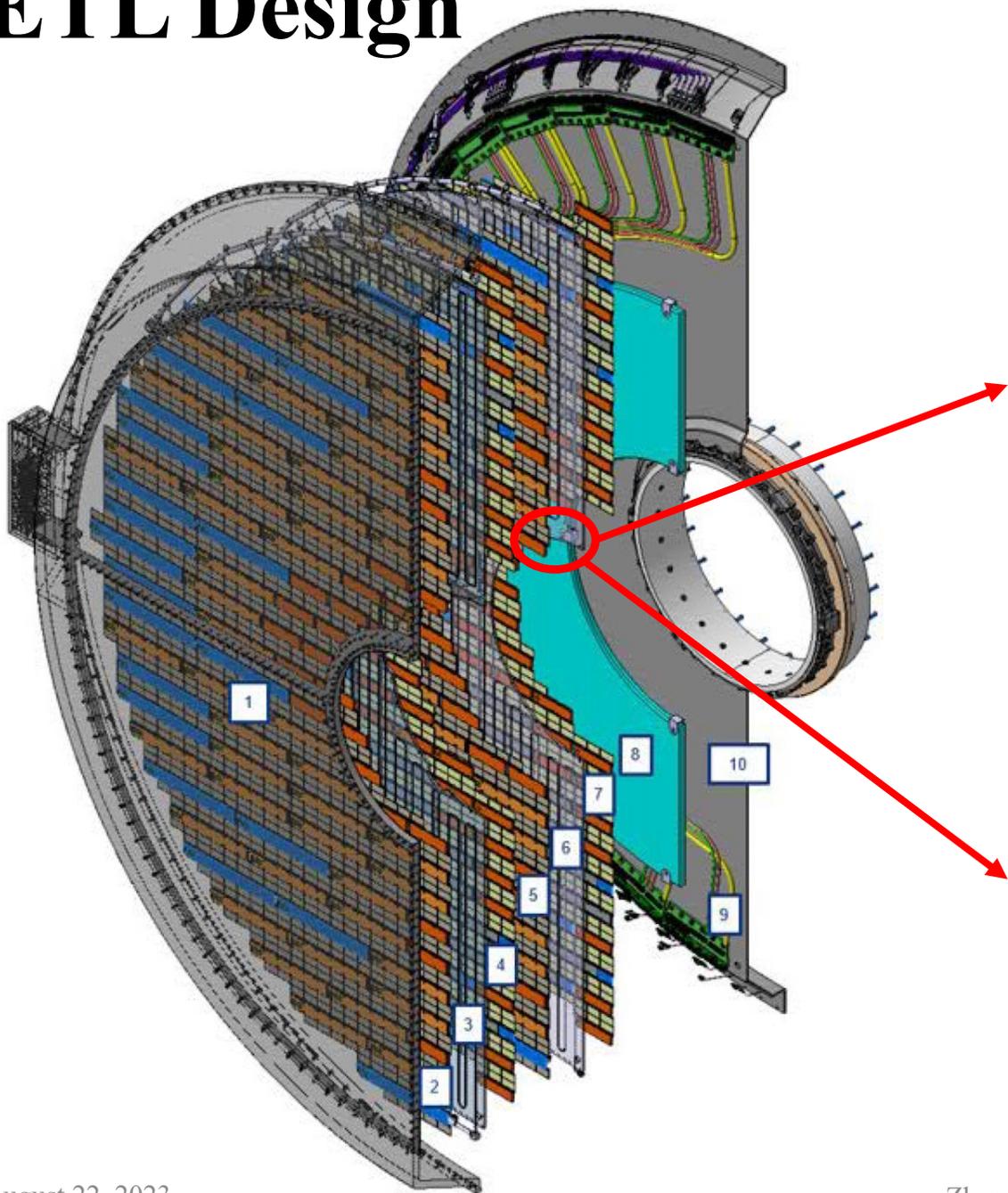
1: Base plate (AlN)
2: LGAD
3: ETROC
4: PCB
5: Wire bonds
6: Board-to-board connector

Module PCB

ETROC

LGAD

Baseplate
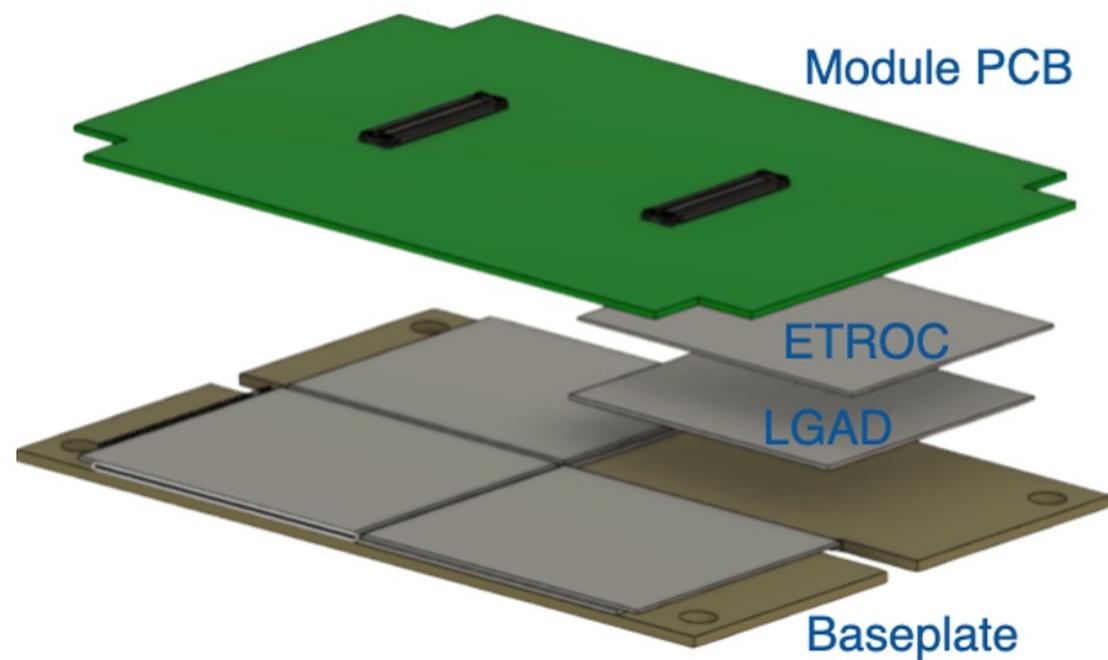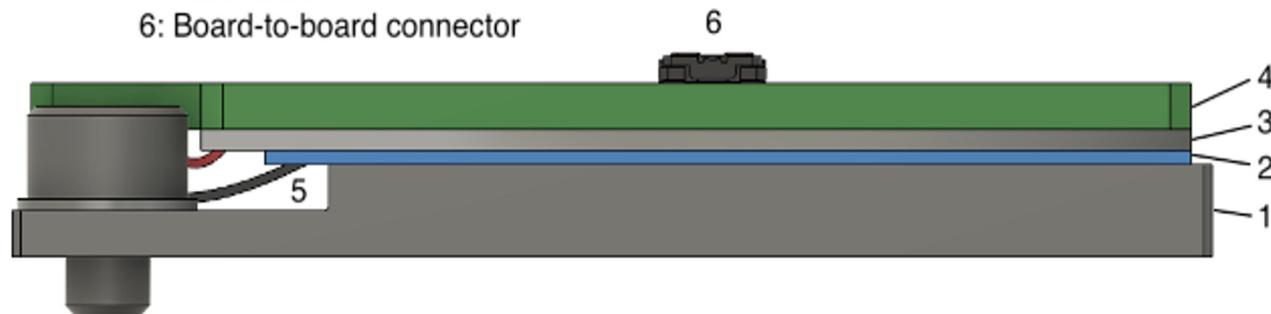
ETL Sensor

- ETL will be instrumented with Low Gain Avalanche Diode (LGAD) sensors optimized for timing measurements

- LGADs has an internal gain layer, which is a highly-doped thin layer near the p-n junction, where a high local electric field producing charge multiplication with a moderate gain factor of 10-30 to maximize signal/noise ratio

- ETL sensor requirements:
  - Sensor size: 50 μm-thick, 16×16 pads array with 1.3×1.3 mm^2 pads, whose size is determined by occupancy and read-out electronics
  - Low leakage current to limit power consumption and noise
  - Large and uniform signals: >8 fC pre-radiation, >5 fC after highest irradiation point
  - Minimized "no-gain" area: inter-pad distance < 50 μm
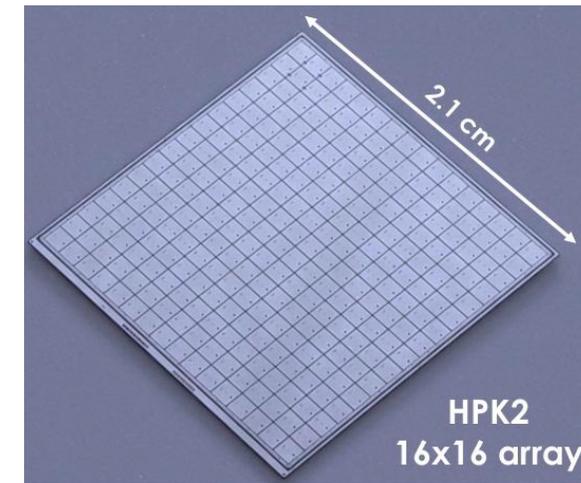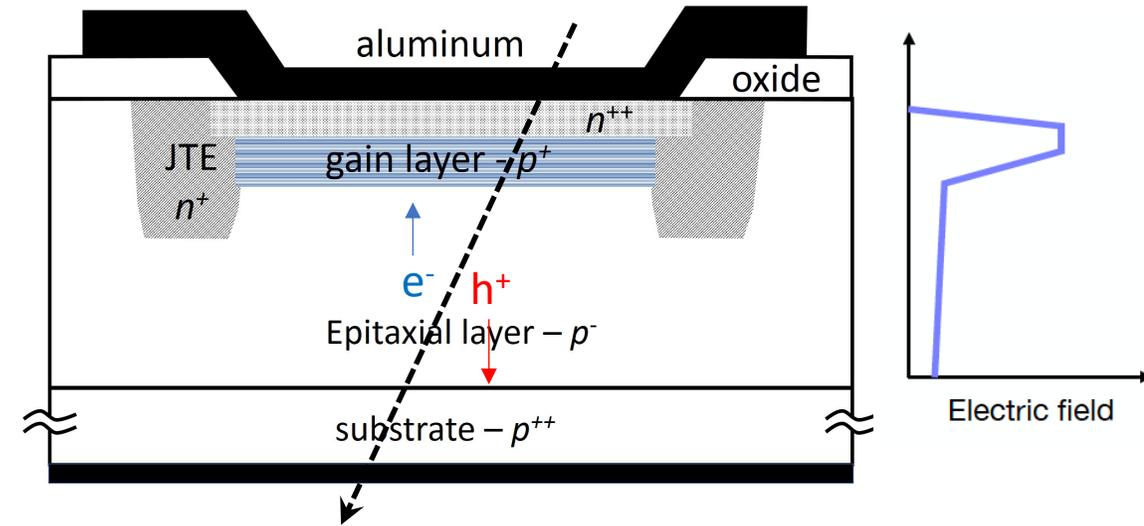
ETL Sensor Prototyping
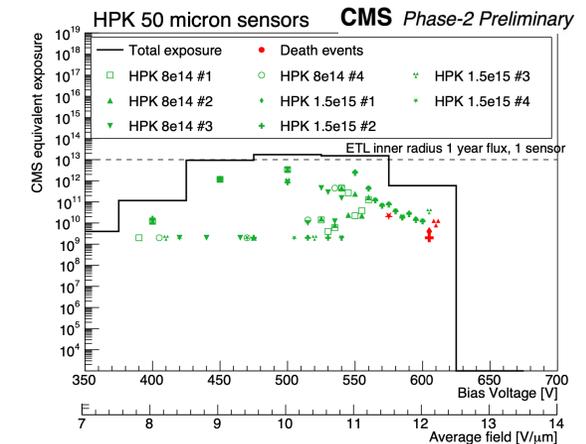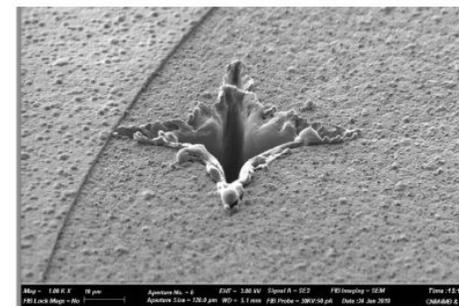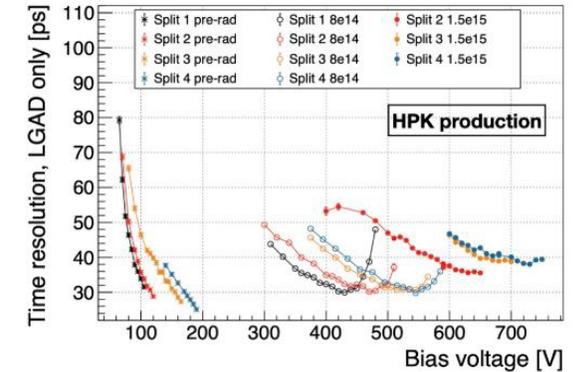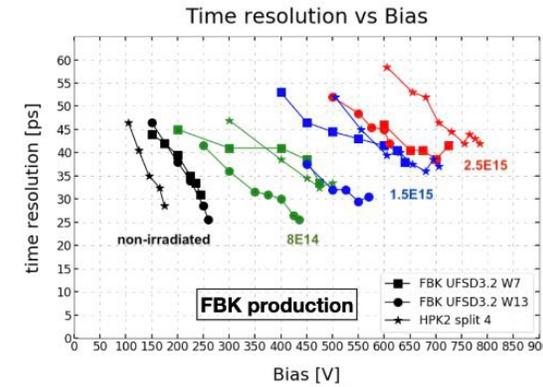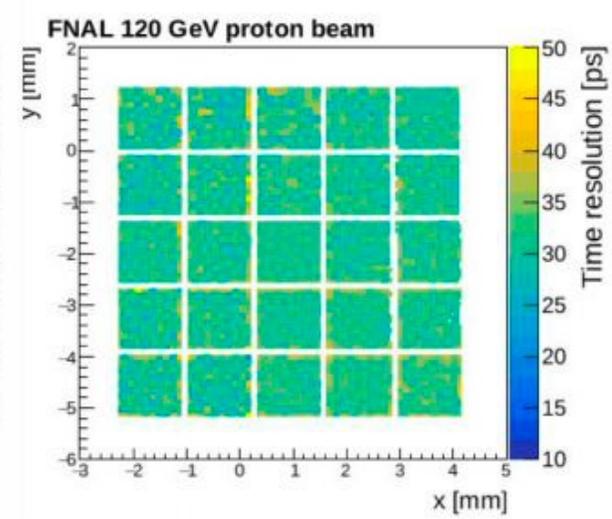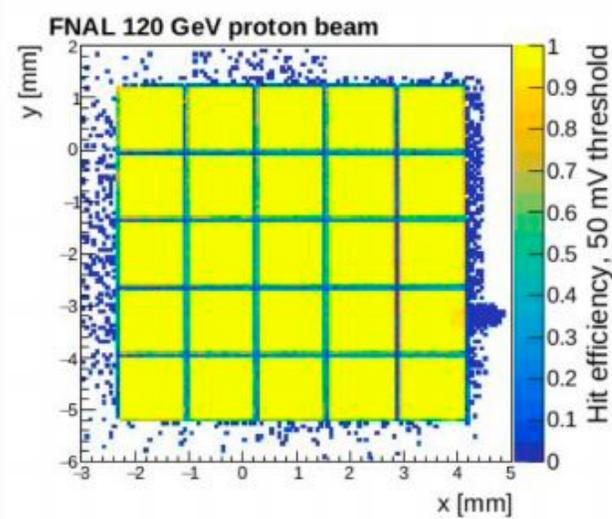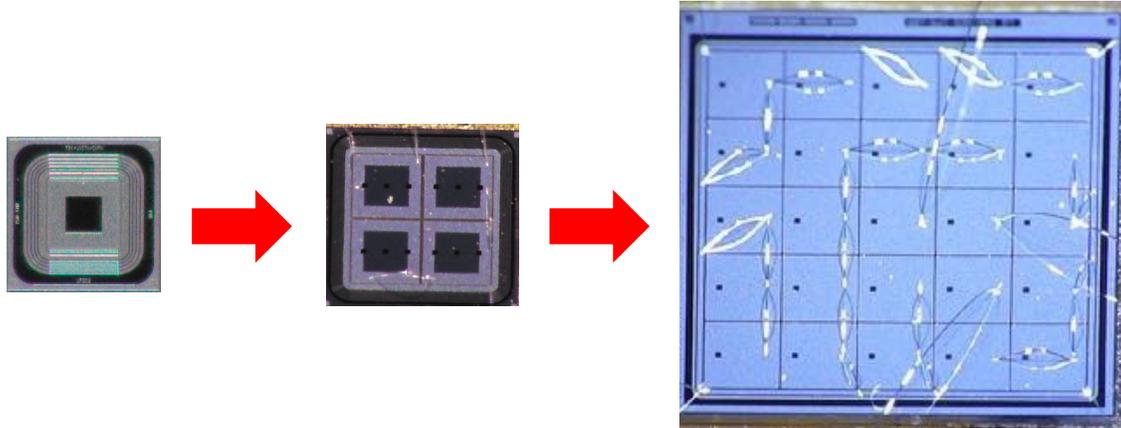
- Worked with multiple vendors to develop prototype sensors and optimize their designs for ETL
- Thin silicon sensors have been found to be susceptible to sudden death when operated with BV corresponding to ≥ 11.5V/μm caused by **"single event burnout"** from rare, large ionizing events where excess charge leads to highly localized conductive path
- Prototype LGAD sensors were characterized before and after irradiation to determine their operation constraint and radiation hardness, and checked whether they can meet the performance requirements with BV$\leq$11.5V/μm

Towards Final Sensor Design
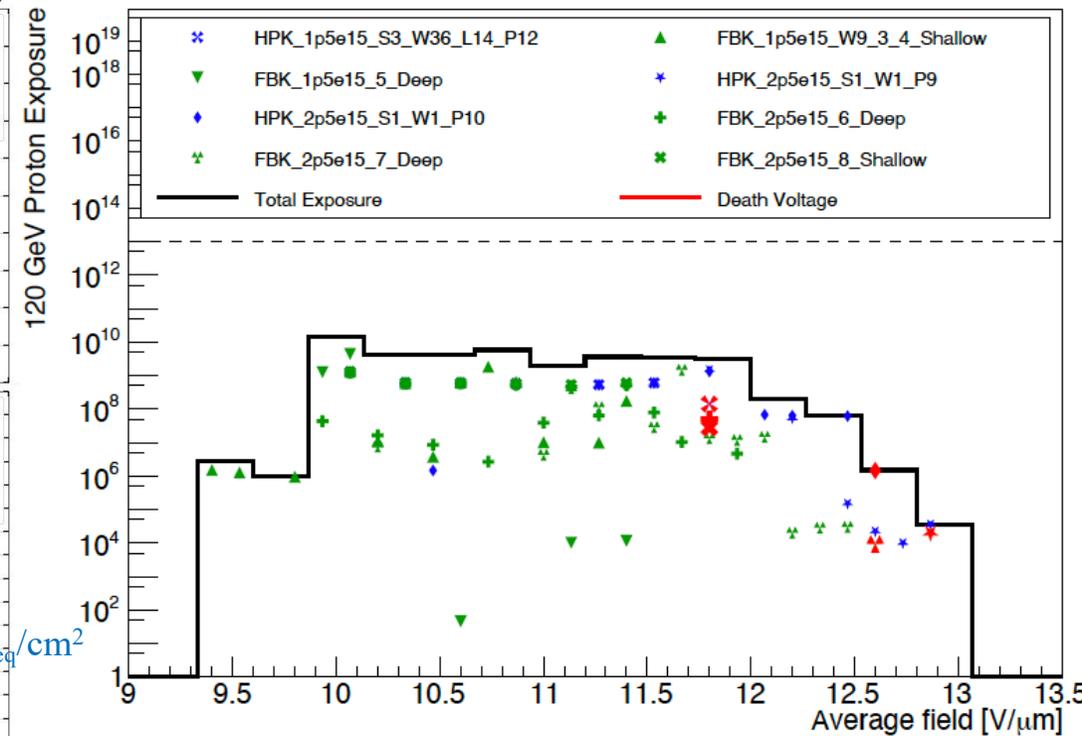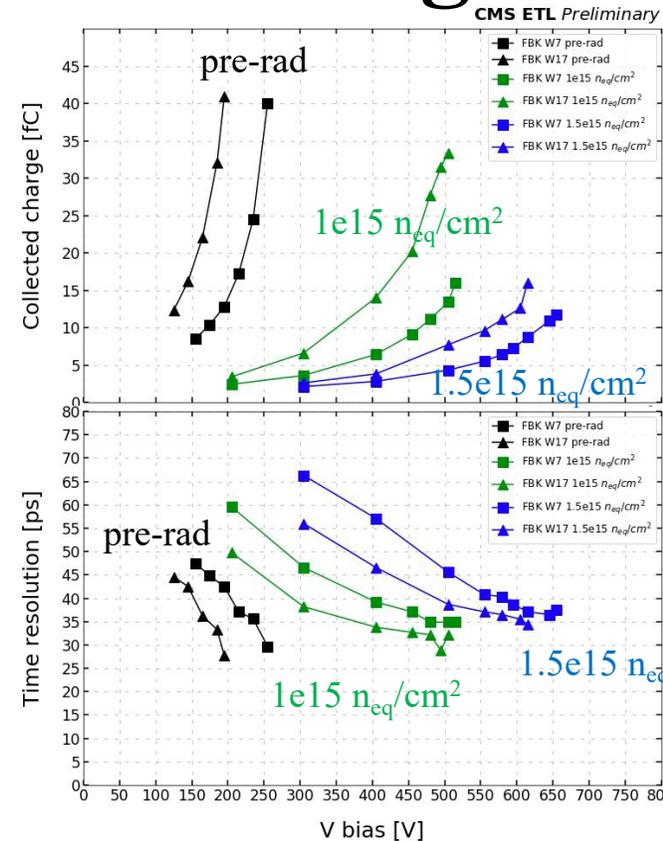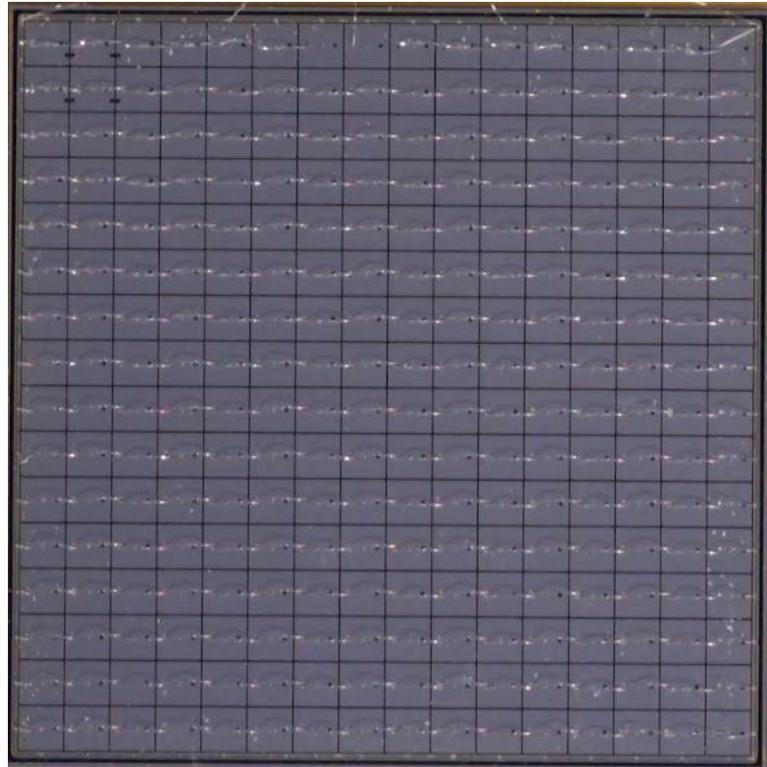
- **Path to freeze the sensor geometry and specifications**
  - Complete stress tests of full size LGAD 16x16 pads – ongoing
  - Perform detailed test of sensors with ETROC2 (see next slide)
- **Vendor qualification (market survey) based on full size sensors almost complete**
  - 3 vendors qualify for the low fluence area, two of them also qualify for high fluence area
  - 1 additional vendor may qualify for the low fluence area

Performance consistent with 5x5 sensors

ETL Readout Chip (ETROC)

65 nm

16 x 16 channels
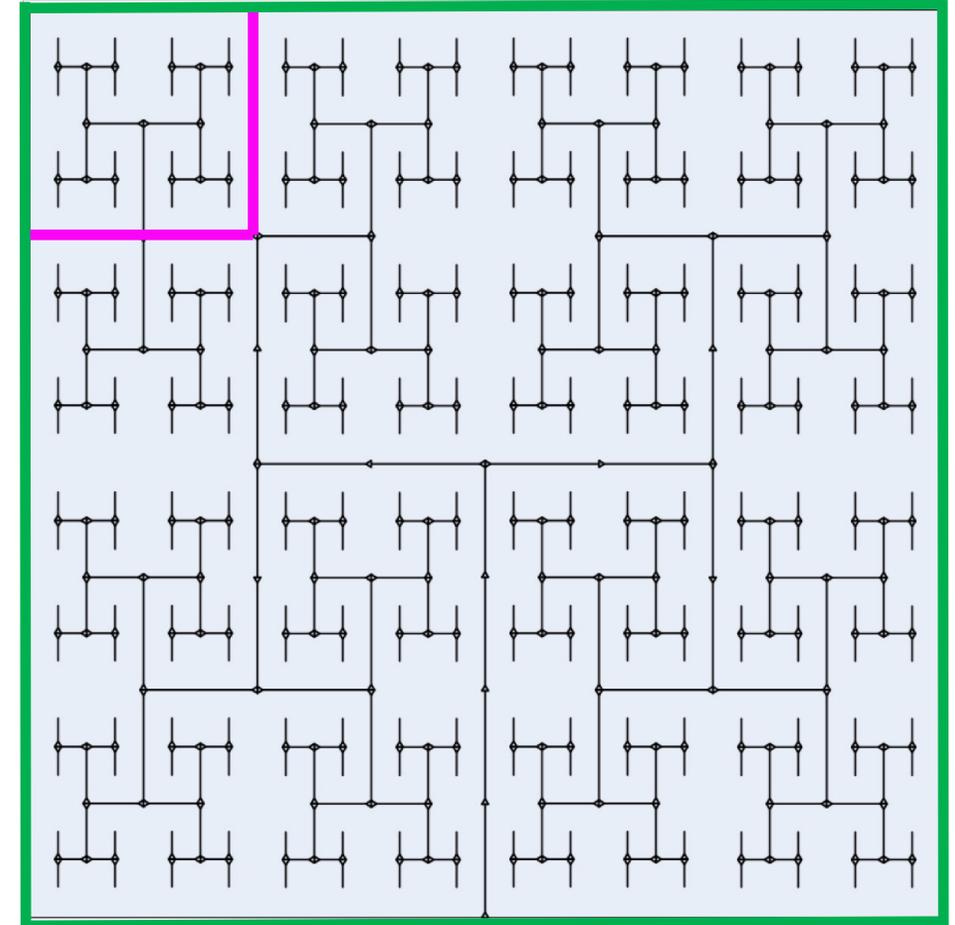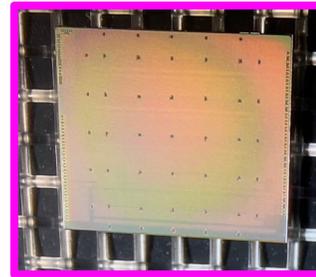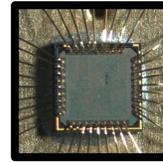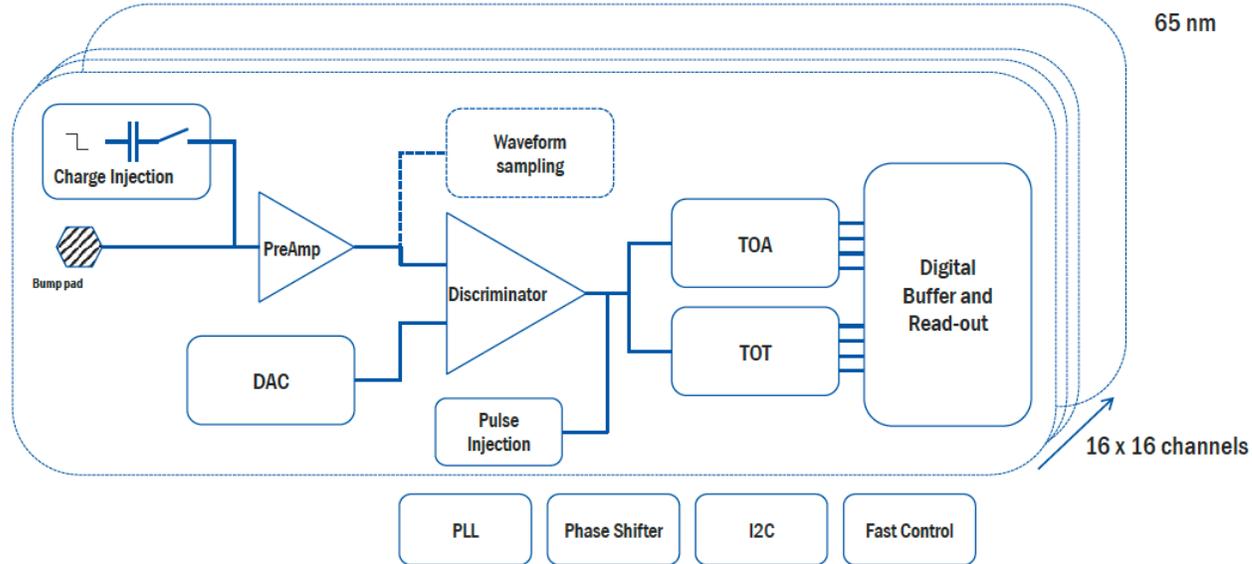
- **Delicate balance act from:**
  - **Low noise & fast rise time**

$$\sigma_{jitter} \sim \frac{e_n C_d}{Q_{in}} \sqrt{t_{rise}} < 40 \ ps$$

  - **Power budget: 1 W/chip, ~4 mW/channel**
- **ETROC innovation:**
  - **Very low power TDC, using simple delay cells with self-calibration**

✓ **ETROC0 : single analog channel**
✓ **ETROC1: with TDC and 4x4 clock tree**
✓ **ETROC2: 16x16 full size full functionality**
❑ **ETROC3: 16x16 preproduction chip**

ETROC

Dec 2018 — **Mar 2020** — *Delayed due to COVID* — ETROC2 submitted **Oct 2022** — ETROC2 received **Apr 2023**

ETROC0 (1x1)

- Analog front-end only
- Wire-bonded with LGAD sensor reached ~33 (30) ps time resolution per hit with preamp. waveform at room temp. (-25 degree C)
- Passed 100 Mrad TID

ETROC1 (4x4)

- Added low-power TDC and 4x4 H-tree for clock distribution
- Bump-bonded with LGAD sensor reached ~42 ps time resolution per hit with TDC data

ETROC2 (16x16)

- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator

LGAD+ETROC0 – Test Beam Results

Strip and **Pixel** Telescope   **Trigger Scintillator**
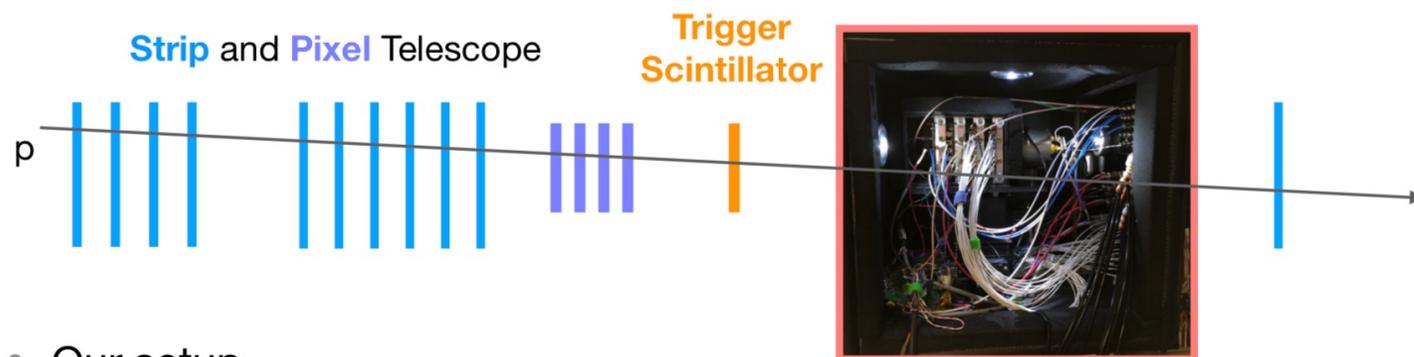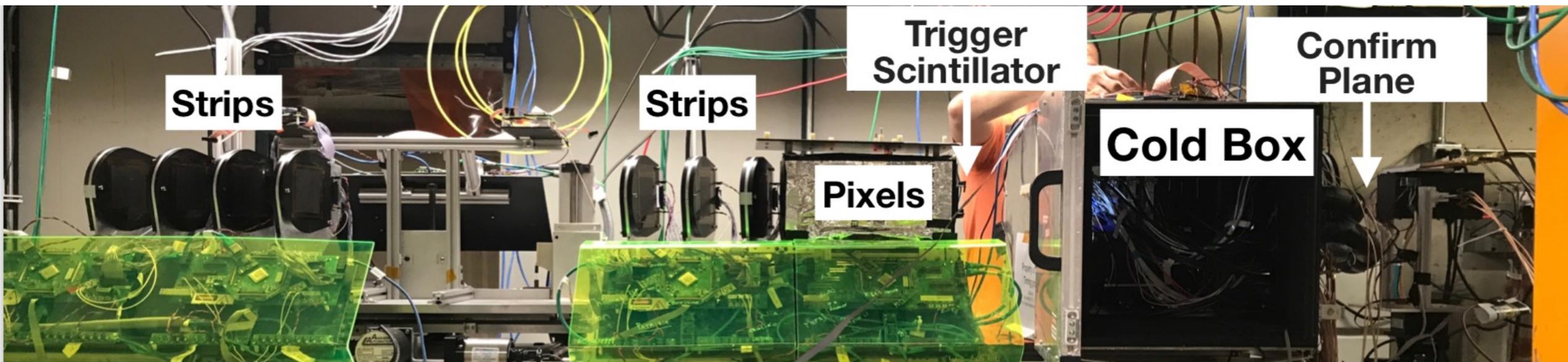
- Our setup
  - Independent scintillator provides trigger
  - Telescope provides proton track
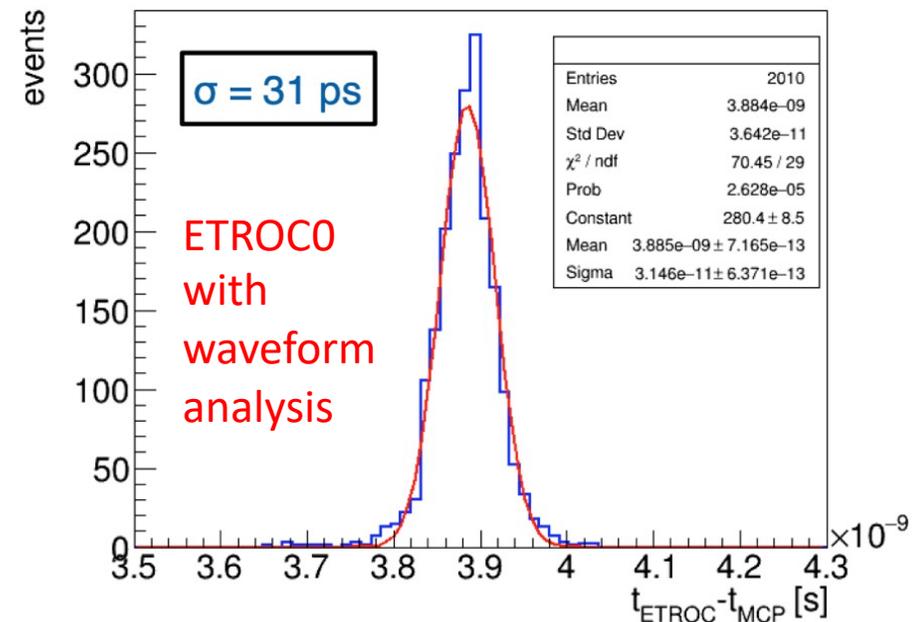 - Oscilloscope saves waveforms
  - Study Δt(LGAD,MCP)

Cold box

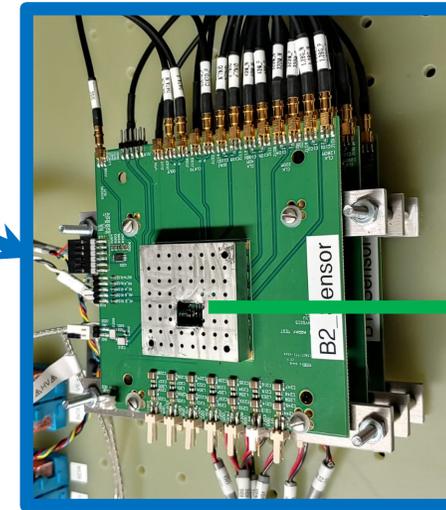LGAD boards on cooling blocks   MCP (Photek) time reference

σ = 31 ps

ETROC0 with waveform analysis

Entries	2010
Mean	3.884e-09
Std Dev	3.642e-11
χ² / ndf	70.45 / 29
Prob	2.628e-05
Constant	280.4 ± 8.5
Mean	3.885e-09 ± 7.165e-13
Sigma	3.146e-11 ± 6.371e-13

$t_{ETROC} - t_{MCP}$ [s]

LGAD+ETROC1 – Test Beam Results

Ch 3 2 1

120 GeV proton Beam

ETROC1 Test Board

ETROC1
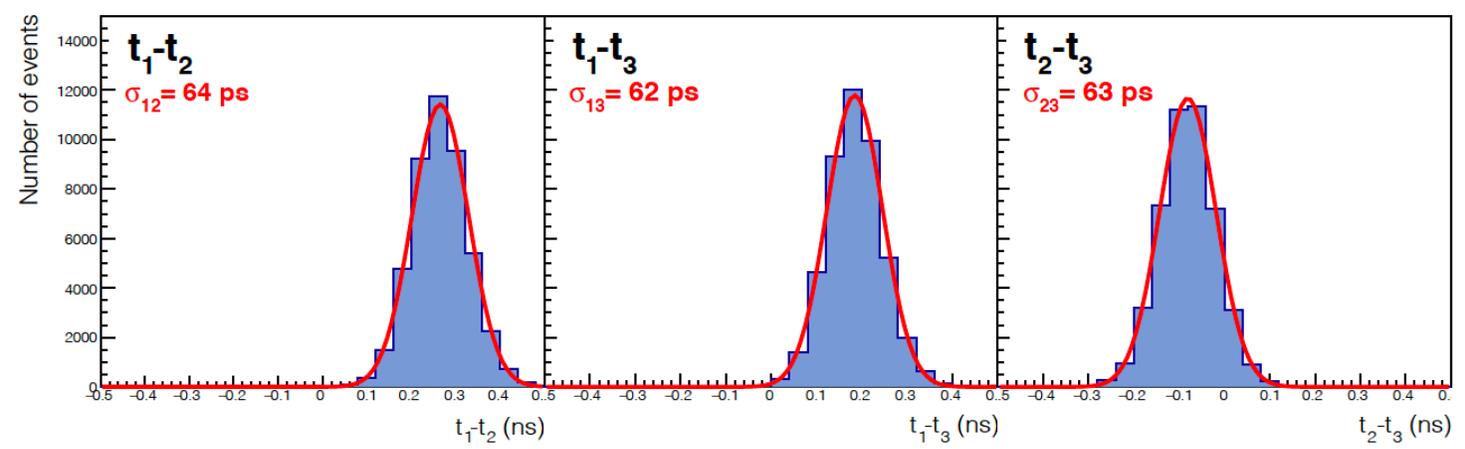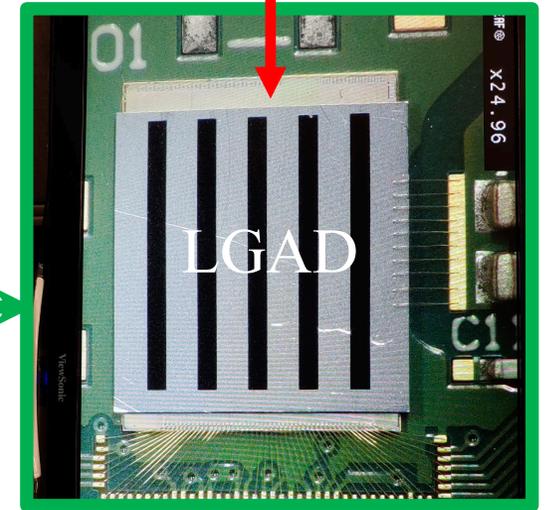
LGAD

LGAD+ETROC1 resolution is 42-46 ps from TDC digital outputs

$$\sigma_i = \sqrt{0.5 \cdot (\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)}$$

t_1-t_2
σ_{12}= 64 ps

t_1-t_3
σ_{13}= 62 ps

t_2-t_3
σ_{23}= 63 ps

ETROC2

✓Initial check on power consumption; detailed study later

✓I2C communication to global circuit and individual pixels

✓Phase-Locked Loop

✓Automatic threshold calibration

✓Digital readout with pattern generator

✓Fast command

✓Initial test with charge injection; detailed check on-going

✓Initial Total Irradiation Dose test; detailed check on-going

✓Initial waveform sampler test; detailed check on-going

✓Initial test of ETROC2+LGAD; detailed check on-going, beam test planned in Sept. (SPS) and Dec. (DESY)

• Wafer probe test started

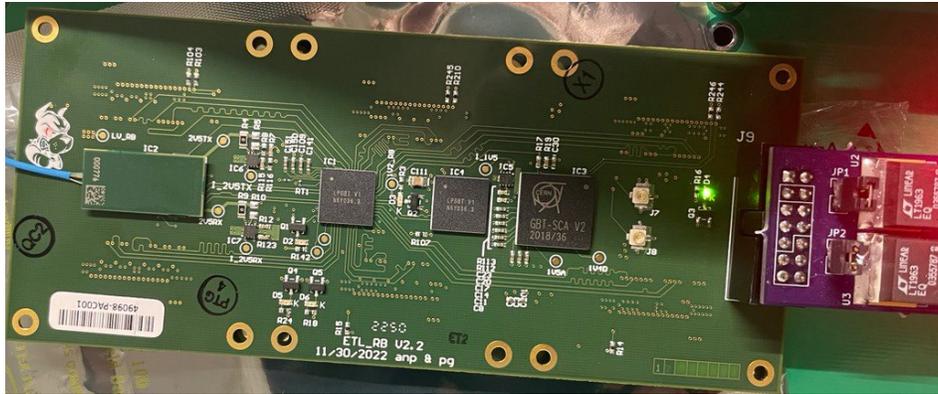• Single Event Upset test being planned
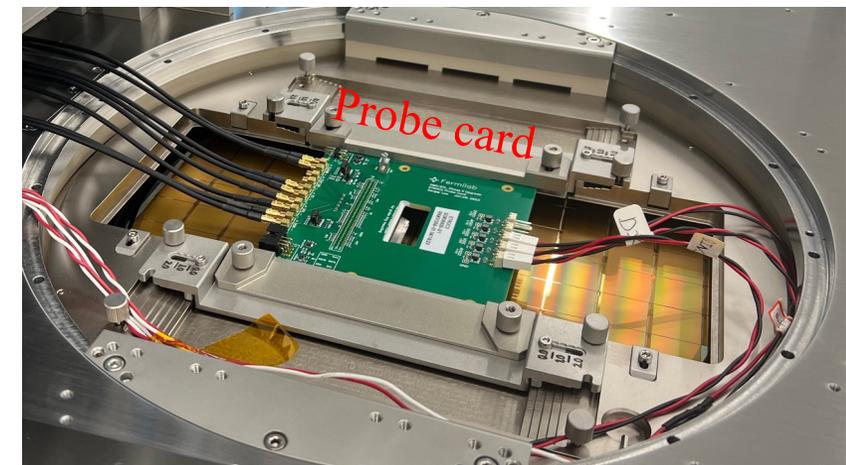
ETL Module Assembly

3 assembly sites established with a gantry or jigs; 1 additional being setup; more under discussion
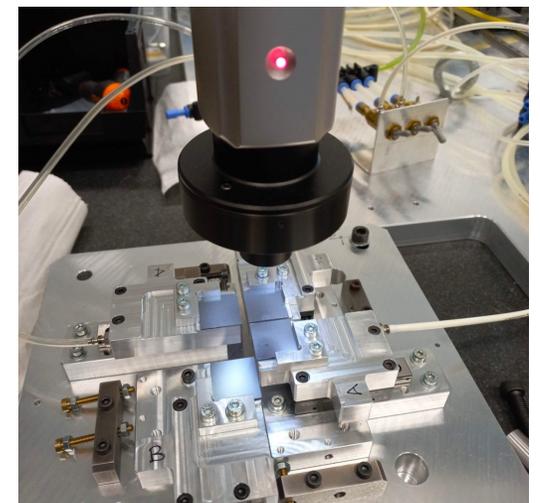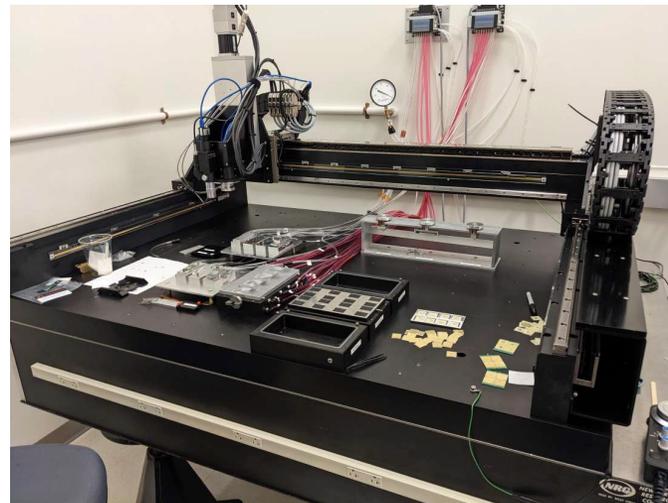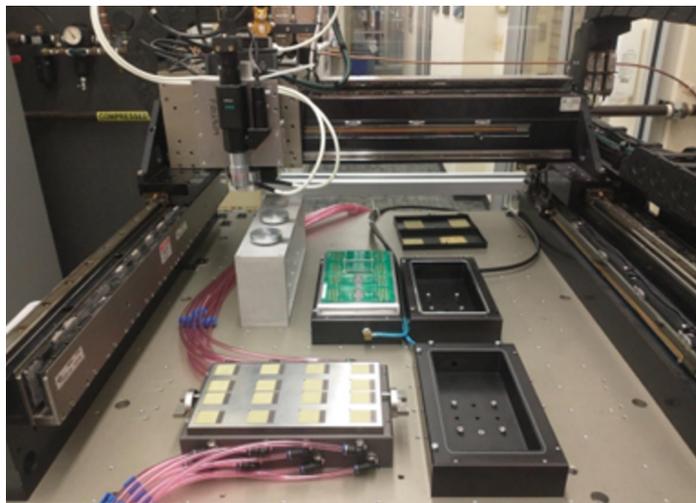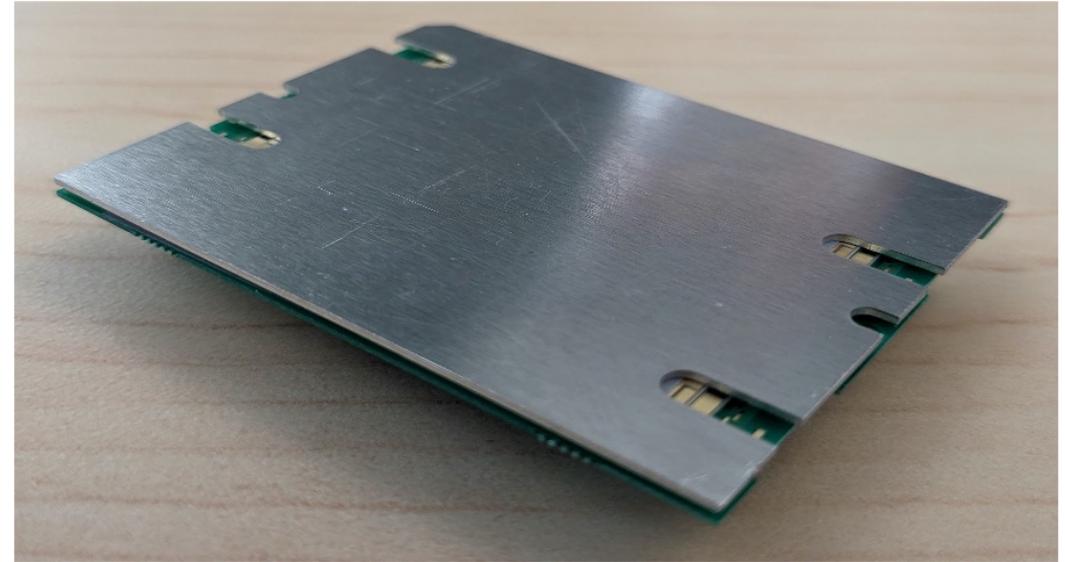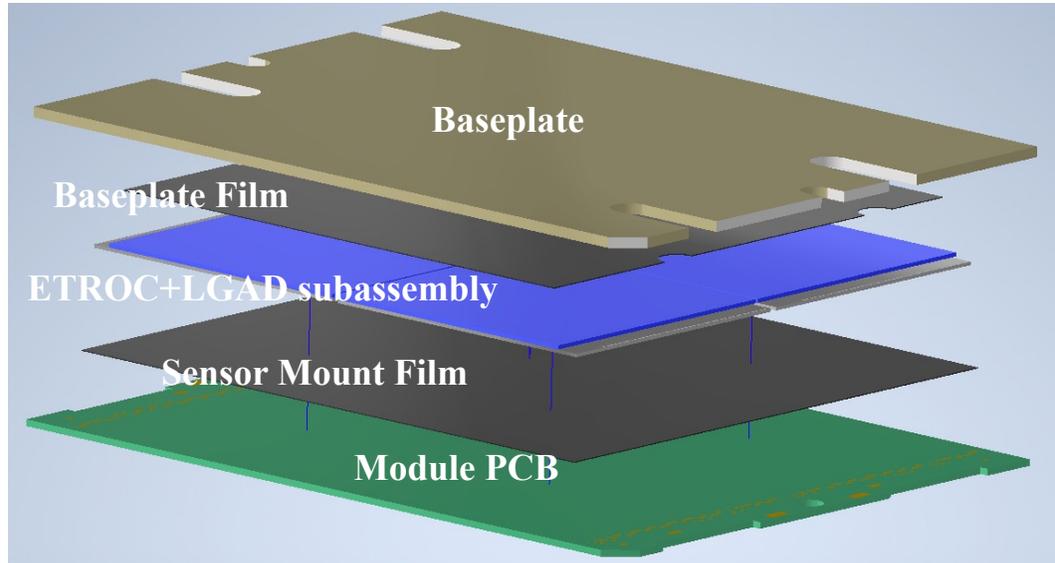
Readout and Power Boards
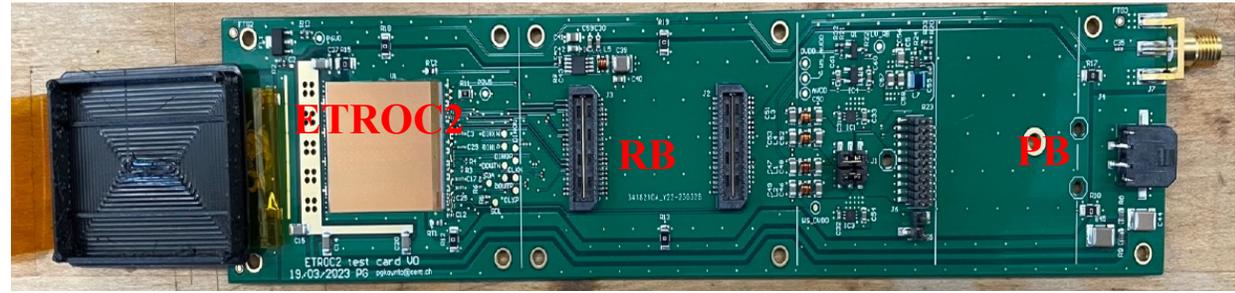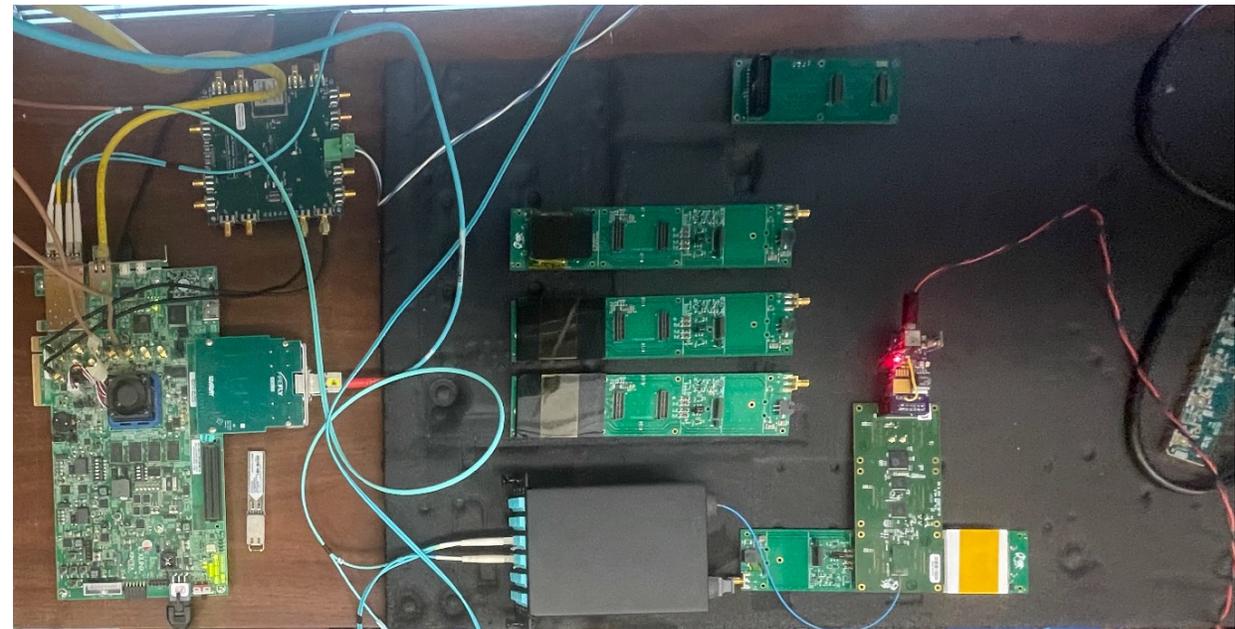
- Prototype V2 readout board
  - LpGBTv1+VTRX

- Prototype V2 power board
  - Efficiencies ~ 65-67%

- First system test with bare ETROC2 on the first functional module PCB successful;
- Full demonstration rely on complete system test

Summary and Outlook

- MTD will be essential for the CMS physics program at HL-LHC
  - Reduce pile-up contributions, improve object reconstruction, enable new physics opportunities

- Mature design for ETL has been established through extensive prototyping and testing
  - LGAD read out by ETROC will provide the needed timing resolution and radiation tolerance at $1.6 < |\eta| < 3$

- ETL is entering a decisive phase of final prototyping
  - Successful MS for LGAD sensors to be concluded soon
  - Initial testing of ETROC2 indicate no major problem but more to learn in coming months
  - Module design and assembly procedure ready to assemble first functional prototypes
  - Successful initial system test with bare ETROC2 using prototype readout and power boards
  - Other detector system components (cooling, mechanic prototypes, and integration optimization) in progress