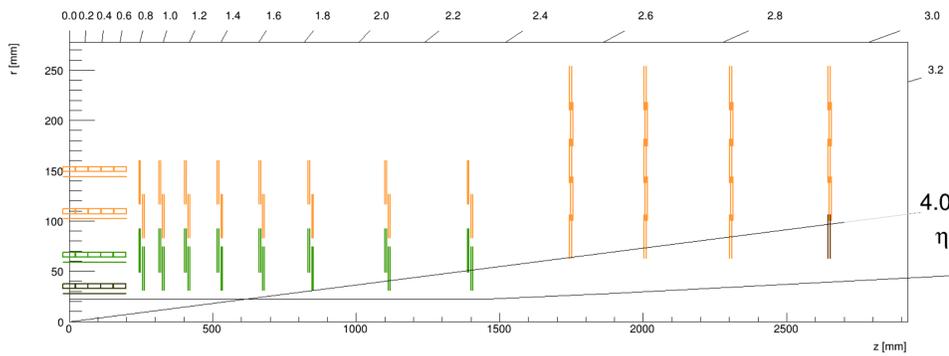


Weijie Jin on behalf of the CMS Collaboration

The CMS Phase-2 Inner Tracker Upgrade



Inner Tracker: 2×1 pixel chip modules, 2×2 pixel chip modules, 3D modules

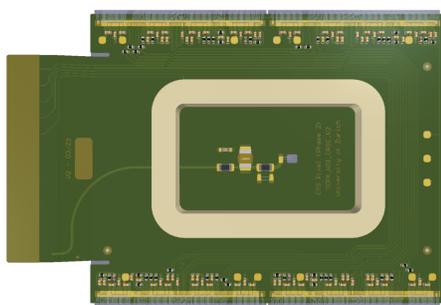
- During the long shutdown 3 (LS3) the LHC will be upgraded to collide protons at a center-of-mass energy of 14 TeV and to reach a peak instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- The upgrade to the HL-LHC brings significant challenges for the CMS inner tracker
 - 3–4 × more pileup (200 proton collisions per bunch crossing)
 - Hit rate up to 3.2 GHz/cm² in layer 1
 - 3 × longer trigger latency (12.8 μs)
 - 10 × more radiation (TID 1.2 Grad, hadron fluence $2.3 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$)
- To deal with these conditions, a complete new Tracker will be built, aiming to maintain and even improve the performance of the current tracker
- To achieve this goal, the Phase-2 Inner Tracker needs
 - Increased granularity: ~2 billion pixels of 25 μm × 100 μm (6 × smaller)
 - Increased coverage: pseudorapidity region up to $|\eta| = 4$
 - Lower material budget: light mechanics, powering

CROC-V1



- Developed for ATLAS and CMS by the RD53 collaboration
- 432 × 336 pixels
- Bump-bonded to the sensor
- Shunt-LDO for powering analog and digital parts independently at 1.2 V
- CML driver for data transmission
- Production chip RD53C-CMS is currently being finalized

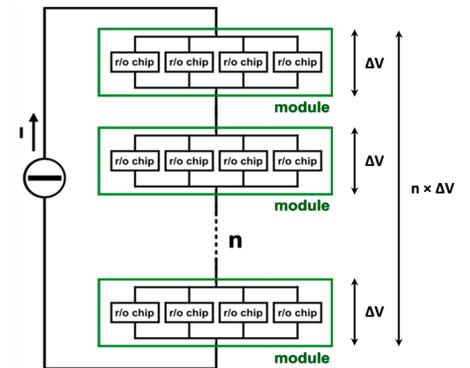
TEPX HDI



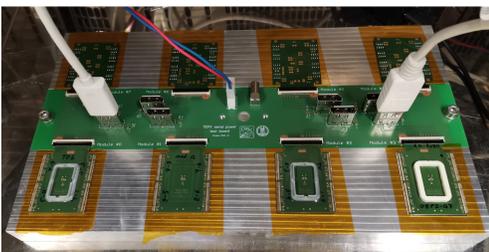
- 4 chips (2×2) powered in parallel
- Data and power from same connector
- Exposed pads that can be used for voltage measurements

Serial Powering of Pixel Modules

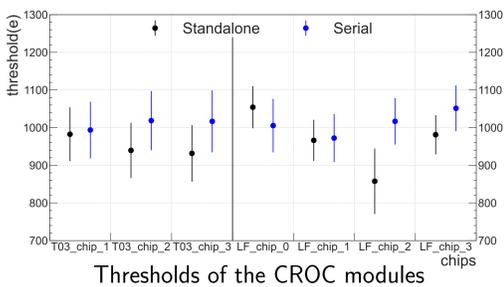
- With increased granularity and pseudorapidity coverage, parallel powering of the pixel modules would require a huge number of cables → increased material budget
- The Phase-2 Inner Tracker will need serial powering (up to 11 modules per chain) → This has never been implemented in HEP for large systems
- Grounds of modules/sensors differ inside the chain
- Enough current injected to satisfy the highest possible load current
- Total current constant – independent of load → comes at the cost of extra power burnt in the Shunt-LDO (known as headroom)



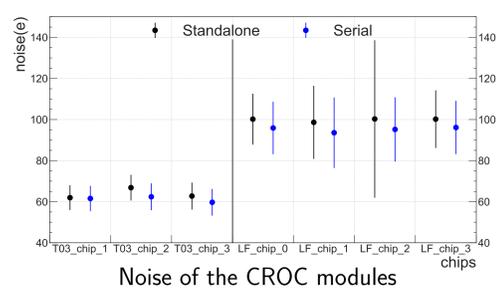
Performance tests of 2×2 pixel chip modules in a serial powering chain



- Climate chamber with -35°C ambient temperature
- Test setup for serial powering of up to 8 quad modules
- Comparing the behaviour of digital and sensor modules either standalone and in a serial powering chain:
 - T03: Digital module with 4 CROC chips
 - LF: Module with LFoundry silicon sensors

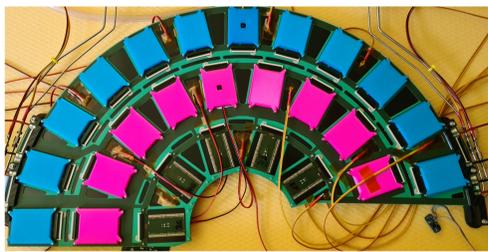


Thresholds of the CROC modules

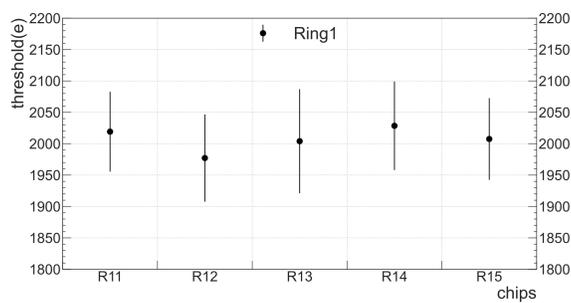


Noise of the CROC modules

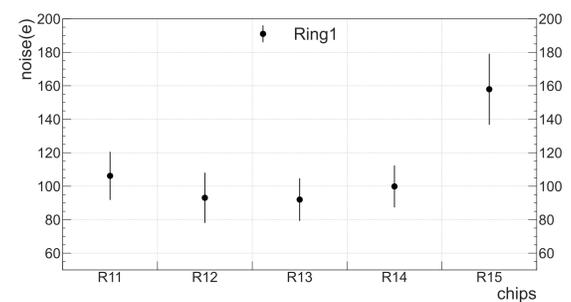
- Thresholds are comparable standalone and in serial power for both digital and sensor modules
- Noise levels are similar standalone and in serial power
- Noise levels of the sensor module are slightly higher than those of the digital module, as expected



Test of the serial power chain on the innermost ring (R1, 5 modules) of a prototype TEPX half-disk, designed for RD53A quads, cooled down by pipes filled with liquid CO₂.



Thresholds of the RD53A modules in ring1



Noise of the RD53A modules in ring1

The noise distribution for one chip per module in the five positions of the serial power chain is shown, and it is compatible with the measurements of the CROC modules.

Conclusions

- Demonstration of digital and sensor modules working in a serial power chain
- Threshold and noise are similar standalone and in serial power.
- RD53A module tests in a disk PCB with CO₂ cooling are performed
- Additional tests with a larger number of modules powered in series will be performed
- CROC module tests will be performed in a prototype disk PCB

References

- CMS Collaboration. The Phase-2 Upgrade of the CMS Tracker, CMS-TDR-014, doi:10.17181/CERN.QZ28.FLHW
- RD53 Collaboration. RD53B users guide, CERN-RD53-PUB-21-001, <https://cds.cern.ch/record/2754251>
- Characterization of irradiated RD53A pixel modules with passive CMOS sensors <https://doi.org/10.1088/1748-0221/17/09/C09004>

