



Contribution ID: 770

Type: Poster

Development of the Belle II Hardware Track Trigger for High Luminosity

In the Belle II experiment, which uses data from the electron-positron collision at the SuperKEKB accelerator, a hardware trigger is used to reduce a readout rate and data size. The track trigger reconstructs three-dimensional tracks using signals from the Central Drift Chamber. The trigger system is composed of FPGAs to meet requirements: latency < 4.5 us, trigger rate < 30 kHz, and trigger efficiency to the B meson physics~100 %.

The trigger rate caused by beam-induced backgrounds is 1 kHz at the current luminosity of $0.4 \times 10^{35} \text{ cm}^{-2} \text{s}^{-1}$, and this would be problematic at the target luminosity of $6 \times 10^{35} \text{ cm}^{-2} \text{s}^{-1}$. The main reason for this high trigger rate is the poor resolution of the vertex position due to noise hits from the beam-induced background and adjacent tracks of the target track. To reject such noise hits, we devised a new algorithm based on a voting method in the parameter space, and we utilized five times more hits which became available thanks to the new FPGA board. This new algorithm can reduce 80% of background tracks while keeping the same tracking efficiency as the previous version.

In this talk, we present expected performance improvement at the next physics data taking in 2023 and the implementation status of the new track trigger.

Collaboration / Activity

Belle II

Primary author: SUDO, Hiroto (The University of Tokyo)

Co-authors: LIN, Jie-Cheng (NTU); SHIU, Jing-Ge (NTU); KOGA, Taichiro (KEK); LAI, Yun-Tsung (KEK); USHI-RODA, Yutaka (The University of Tokyo); LIU, Yuxin (Sokendai)

Presenter: SUDO, Hiroto (The University of Tokyo)

Session Classification: Poster session

Track Classification: Detector R&D and Data Handling