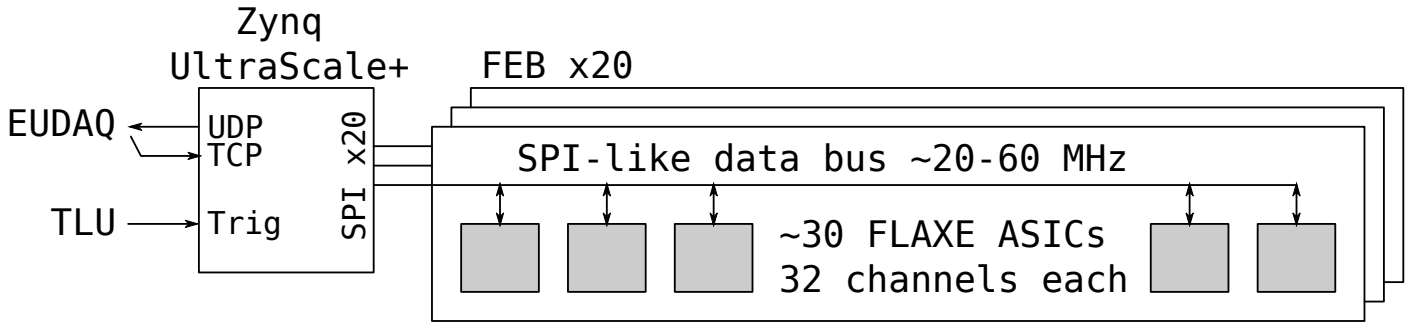
ECAL-P DAQ



- Detector plane read out by the ~30 FLAXE ASICs, each comprising 32 channels with 20 MSps 10-bit ADC in each channel
- Trigger (machine clock?) received from the TLU
- FLAXE ASICs started by FPGA just before BX, based on the trigger related to the previous one
- ~128 ADC samples stored in the internal FLAME memory (~6.4 us long acquisition)
  128 samples * 10 bits * 32 channels / ASIC * 30 ASICs / FEB → 1.23 Mb / BX / FEB
- All ASICs on the FEB connected in parallel to the common data bus (SPI-like). Data from the BX read out sequentially from ASICs between BXs (for 10 BX/s, less than 20 Mbps needed...)
- Single Zynq FPGA reading all 20 FEBs in parallel and processing the data → charge and TOA reconstruction → zero suppression → single UDP 1Gbps link to the EUDAQ (+TCP for slow control)

- Current status: large part of the DAQ working (for slightly different ASIC though) for testbeam purposes
- Needs: training on writing and integrating the EUDAQ producer could be helpful...
- Manpower: One senior (part time) + possibly a PhD student from October
  We are also searching for PostDoc candidate