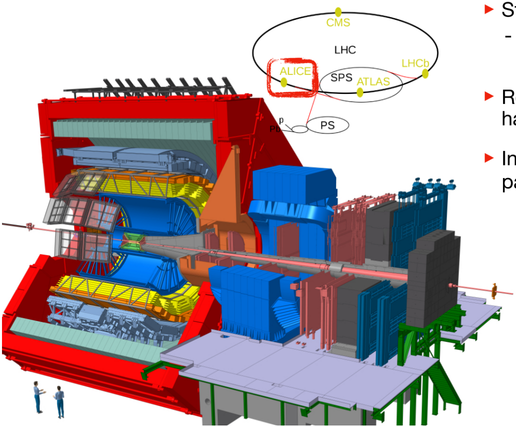
The readout circuitry of Super-ALPIDE and MAPS in embedded in Polyimide

Alperen YÜNCÜ

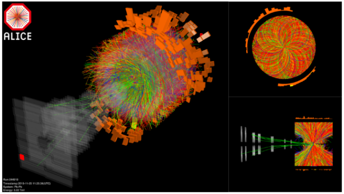
September 2, 2022

ALICE

Detector and main goals



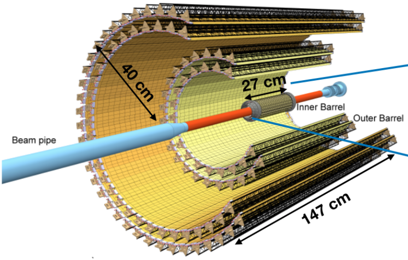
- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction



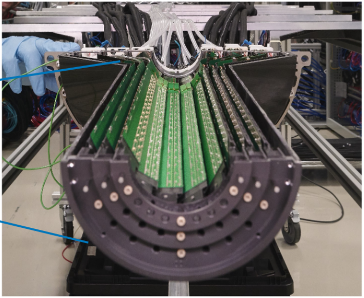
ITS2

It is fabricated in MAPS(Monolithic Active Pixel Sensor) technology. Using TowerJazz 180 nm process. Cover $10\ \mathrm{m}^2$ features 12.5 Gpx.

Layout

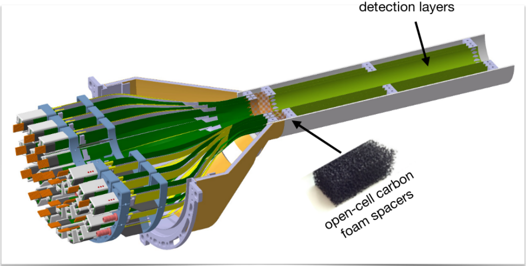


ITS2: assembled three inner-most half-layers



- ITS2 is expected to perform according to specifications or even better
- The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- **Key questions: Can we get closer to the IP? Can we reduce the material further?**

ITS3 Detector Concept

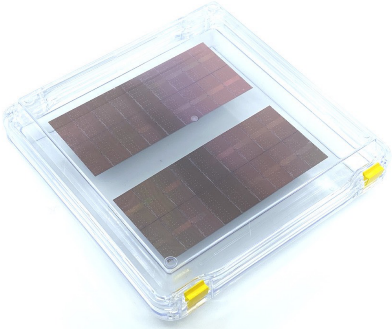


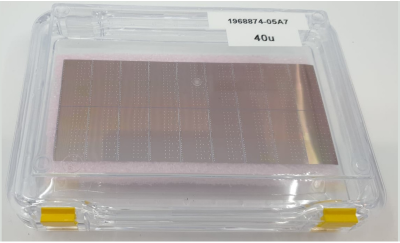
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- Key ingredients:
  - 300 mm wafer-scale chips, fabricated using stitching (65 nm TowerJazz process)
  - thinned down to 20-40 μm (0.02-0.04% X0), making them flexible
  - bent to the target radii
  - mechanically held in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X0(beampipe: 500 μm Be: 0.14% X0)
  - -homogeneous material distribution: negligible systematic error from material distribution

THE WHOLE DETECTOR WILL COMPRISE SIX (!) CHIPS (CURRENT ITS IB: 432) - AND BARELY ANYTHING ELSE

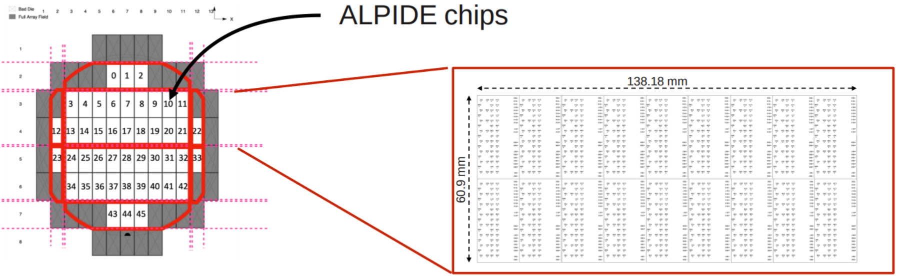
Super ALPIDE Chips



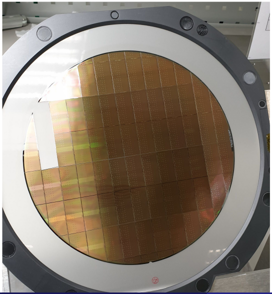


- To study the bending and interconnection of large pieces of processed chips, ”super-ALPIDE” is built
- Comprises of 1 silicon piece cut from an ALPIDE wafer size of $14\,\text{cm} \times 6\,\text{cm}$

Super ALPIDE Chips



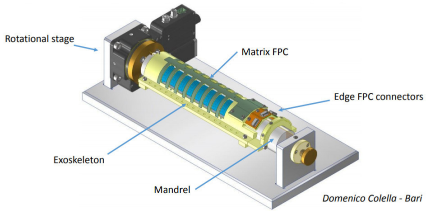
18 ALPIDE chips, covering about a half of an ITS3 half-Layer0

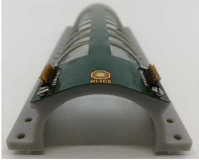


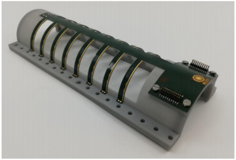
- Super-ALPIDEs are actually an array of ALPIDES.
- They consist 9×2 ALPIDE chips.

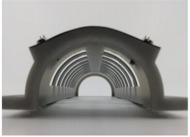
Exoskeleton

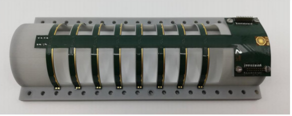
Super-ALPIDE wire-bonding setup





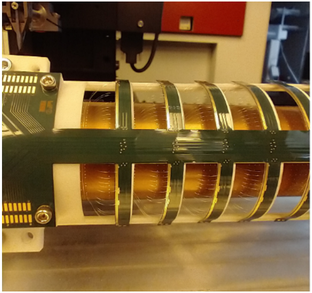


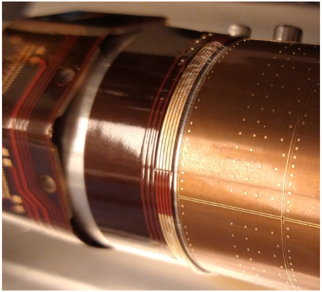




- 3-D printed.
- Designed to support super-ALPIDEs after bending.
- Windows to reach interconnection points at middle of super-ALPIDE
- FPC glued for connections

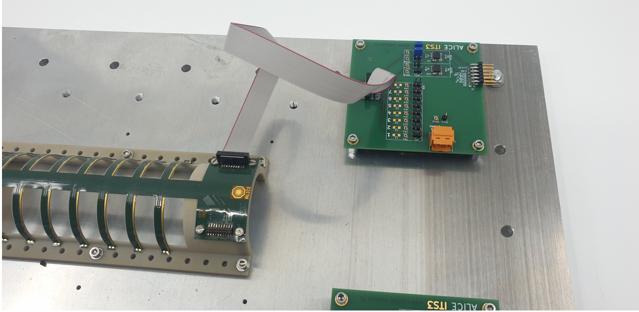
Bonding

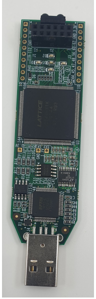




- The first row of ALPIDEs will be wire-bonded to an edge-FPC (just like final ITS3)
- The rest will be bonded to FPC on Exoskeleton via long wires

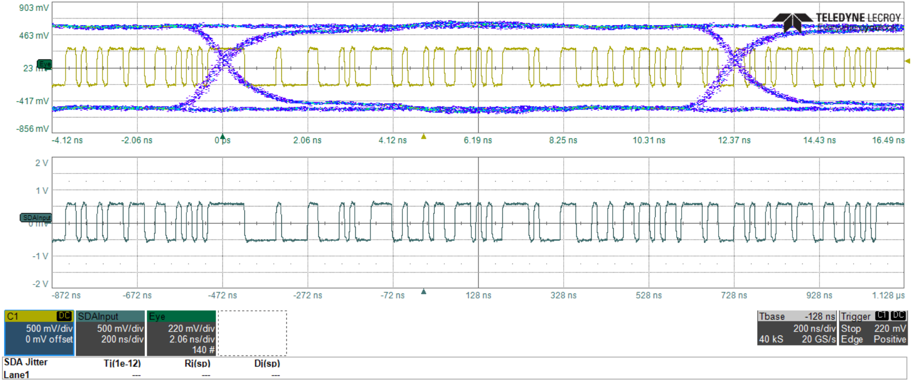
Characterisation of FPC





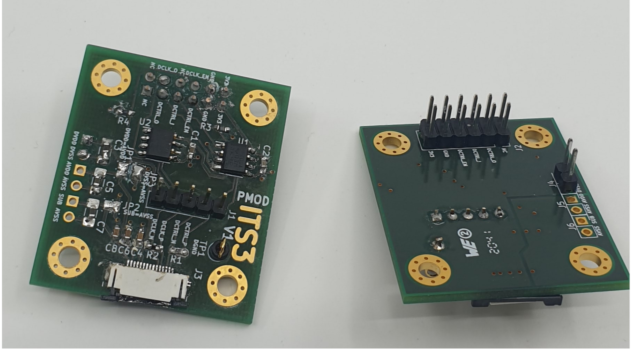
- FPC has been characterised using FPGA via PMOD connection
- Clock signals and PRBS-7 patterns

Characterisation of FPC



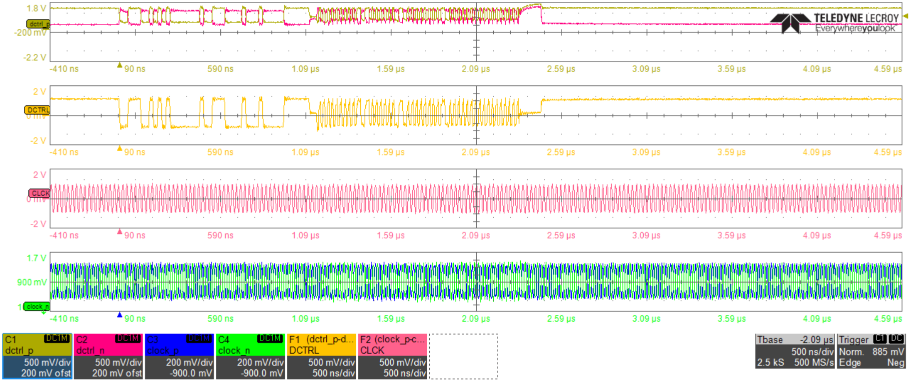
- There is no distortion on signal due to FPC

Readout of a single ALPIDE



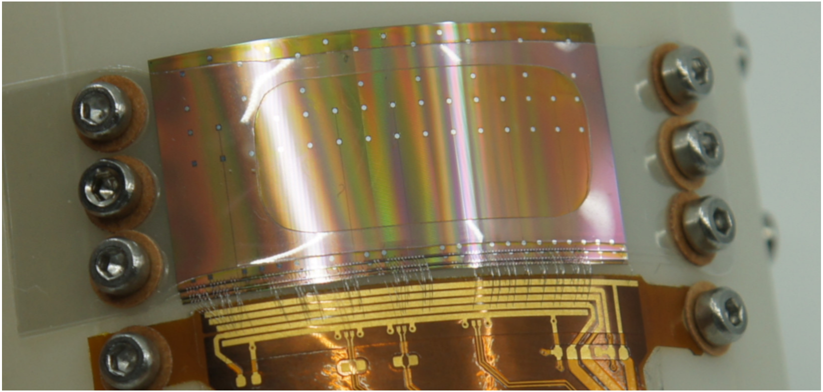
- PMOD adapter boards are built for ALPIDE
- We use single ALPIDE to test readout

Readout of a single ALPIDE



- There is some problems about mismatching chipID's which I am working on right now.

Readout of Triple ALPIDE



- test the readout using triple chips to check readout multiple chip on same readout

MAPS in Polyimide

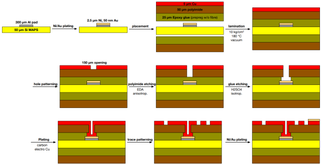


Figure 1: The MAPS foil production process steps.

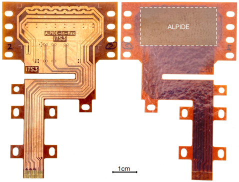
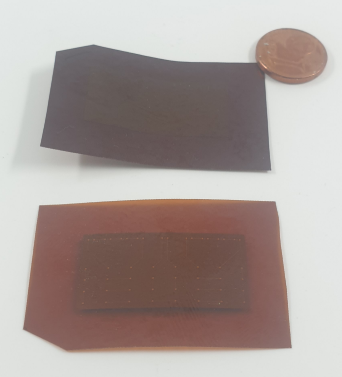
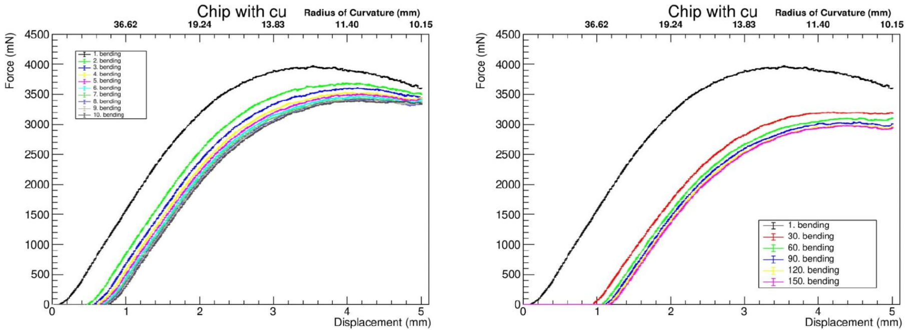


Figure 3: Photographs (front and back) of the assembly. The ALPIDE is embedded at the top part (annotated on the right).

- MAPS (Monolithic Active Pixel Sensors) embeded in Polyimide
- Paper is on arxiv: `https://arxiv.org/pdf/2205.12669.pdf`
- Submitted to Nucl. Instrum. Methods Phys. Res. A



Bending of MAPS



- Because of Polymide, maps has some plastic properties
- Thanks to Polymide layer all chips are protected and hardly can be broken

Summary

- Bonded Super-ALPIDE hasn't arrived, yet. We expect them to arrive by the end of September.
- The electrical characterisation on FPC have been successfully done.
- Readout tests are still ongoing.
- First samples of Maps in Polymide are tested for physical properties. How the physical properties changes by temperature zchanges will be ivestigated.