



Special Release

11th MicroTCA Workshop
6 - 8 December, 2022
DESY, Hamburg

The Artix®-7 based SIS8172 MTCA.4 FMC Carrier



Outline

- Motivation
- Module Design
- Firmware Framework
- Software
- FMC and RTM Application Examples

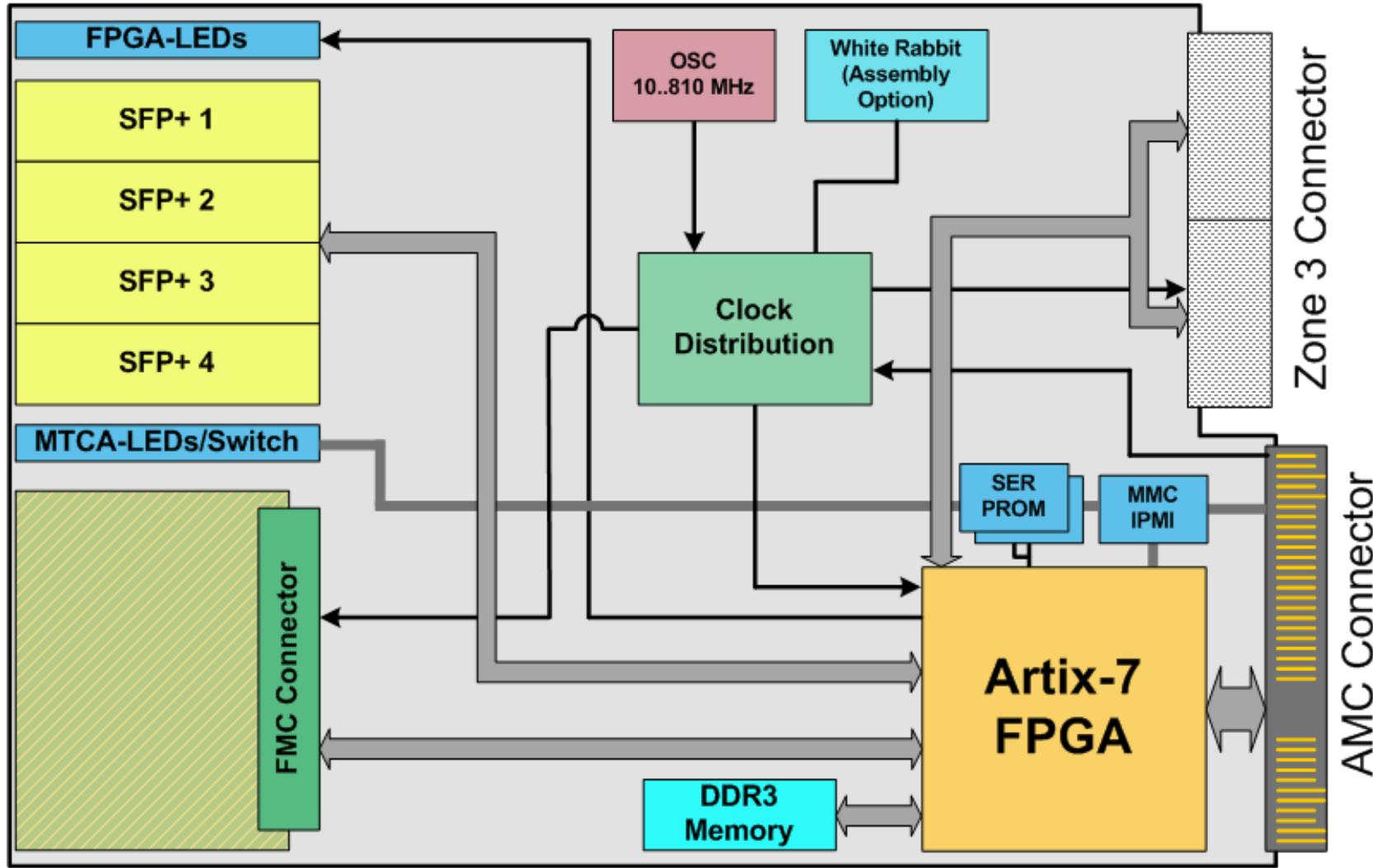
Motivation for SIS8172 Design

- Replacement for Virtex-5 based legacy digital I/O FMC carrier
- Migration to Vivado
- New compact Digital I/O applications

SIS8172 Module Design

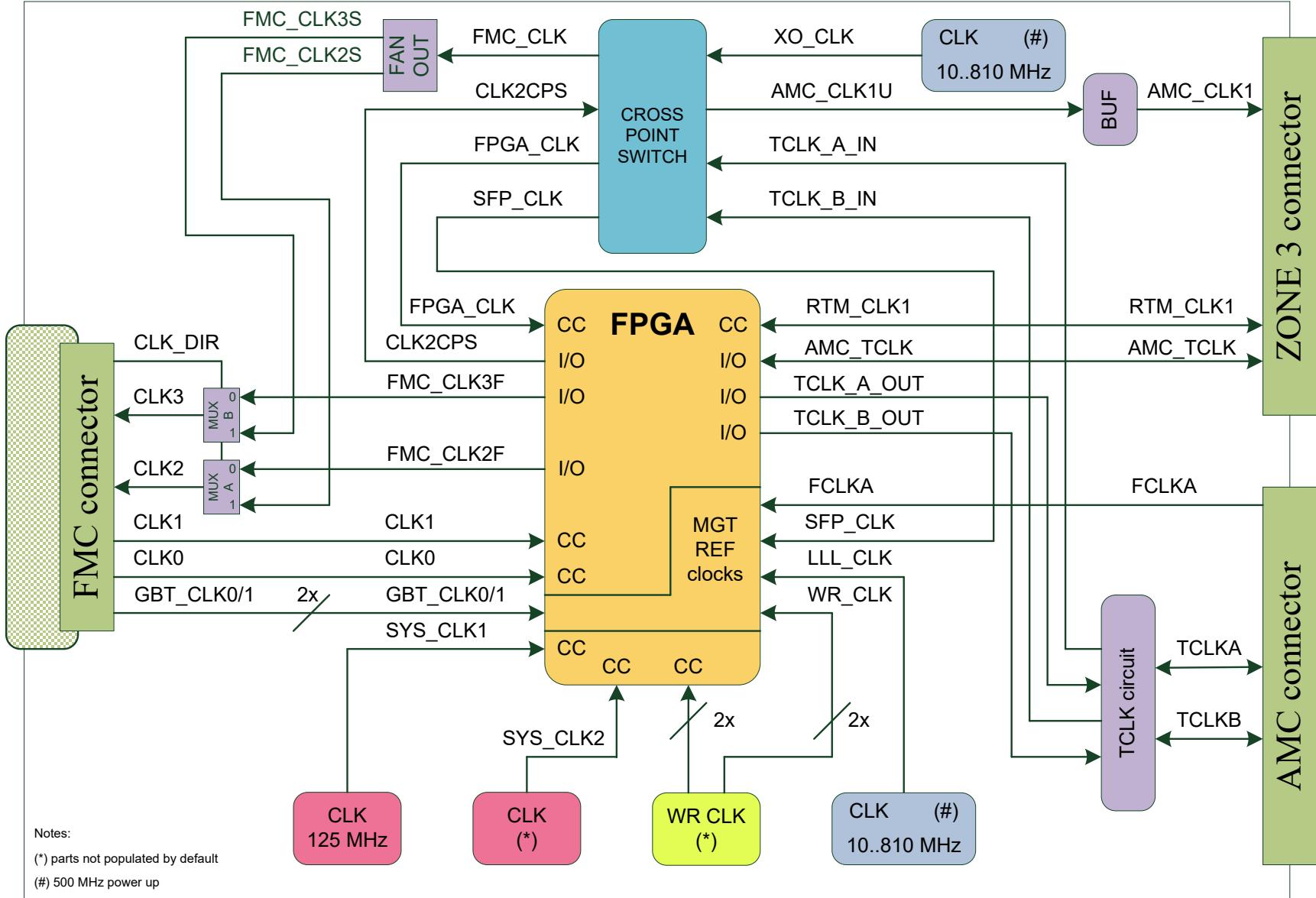
- MTCA.4 AMC
- Zone 3 Class D1.0 Implementation
- XC7A200T-2FGG1156C Artix®-7 FPGA
- Dual FPGA Configuration Flash
- 4 Lane PCIe Gen2
- 256 M x 32 Bit DDR3 Memory
- Quad SFP+ Cage
- HPC FMC Site
- 4 Point to Point Link Backplane Interface
- 4 AMC Ports MLVDS (8 MLVDS lines)
- White Rabbit Timing Option
- DESY MMC1.0 with Atxmega
- Standalone Operation
- In-field firmware Upgrade Support

Block Diagram

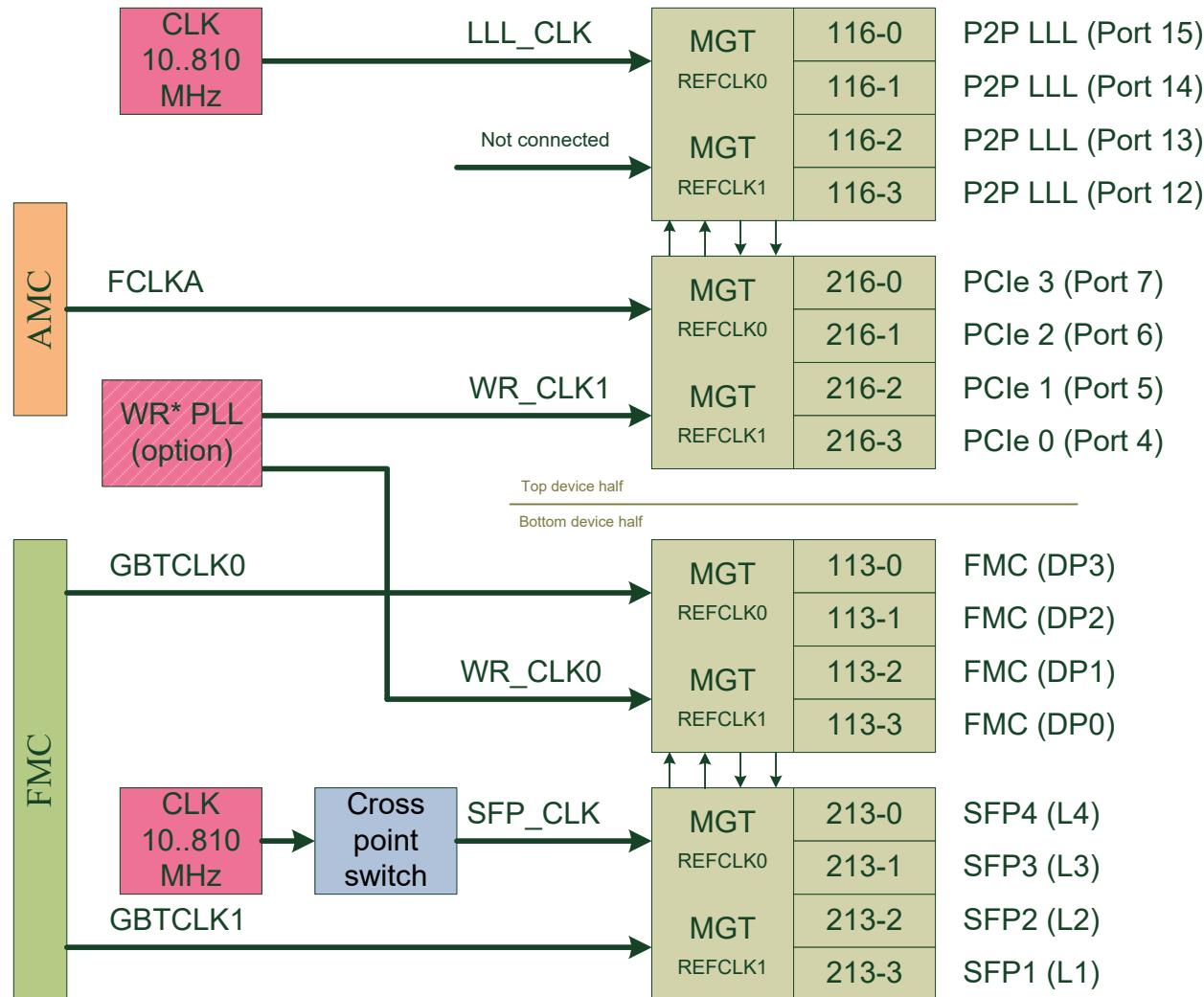


4-lane PCIe, 4 Serial Ports, 8 MLVDS lines ...

Clock Distribution

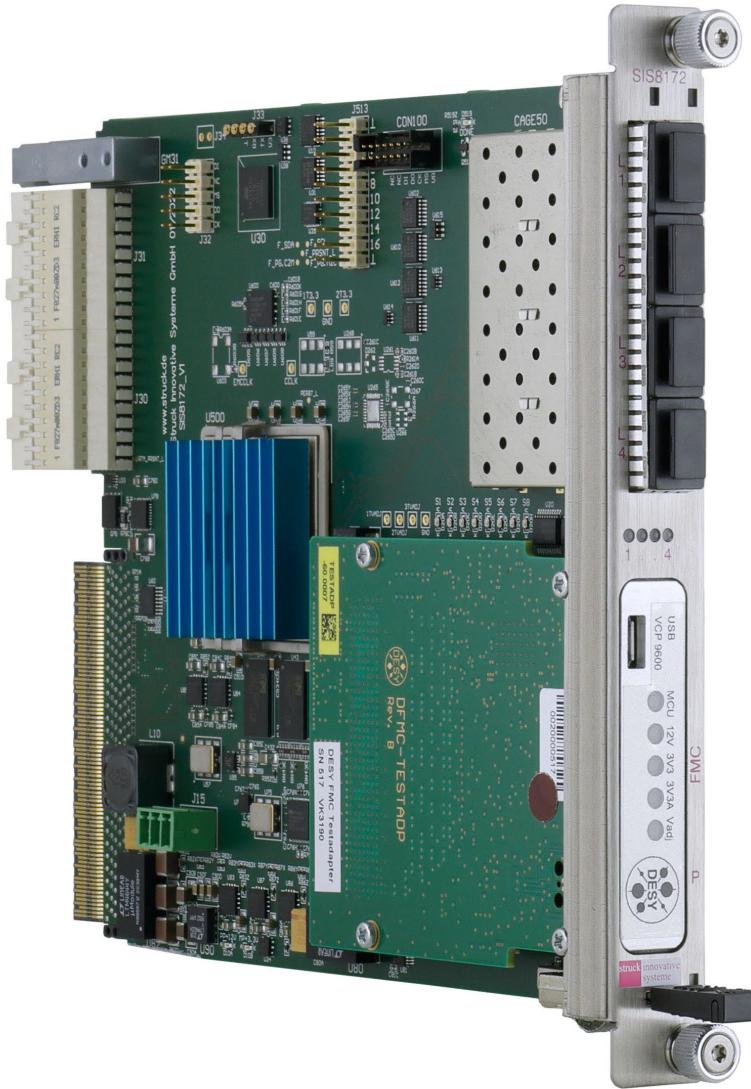


MGT Clock Scheme



* WR – White Rabbit

SIS8172 with DESY TESTADP FMC



Artix®-7 FPGA Limitations

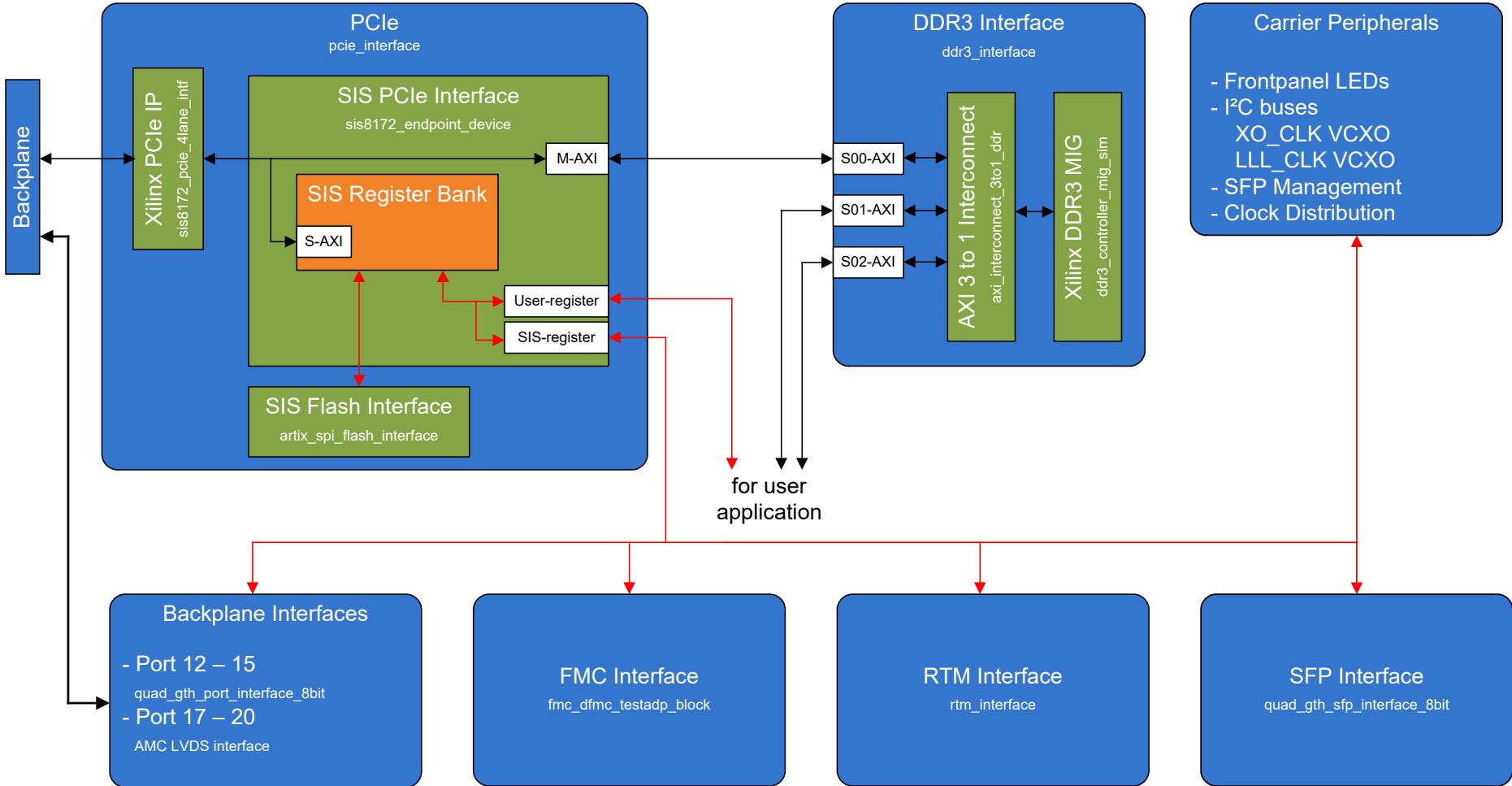
- PCIe Gen2
- DDR3 Memory
- 6.6 Gbit/s MGT Speed

Compared to (Virtex-5)

- PCIe Gen2
- DDR2 Memory
- 3.75 Gbit/s MGT Speed (LX, SX)

but: @ decent cost

SIS8172 Vivado Base Project



SIS8172 Test Suite

```
>>>>> SIS8172 Main Tests <<<<<

Used Device: /dev/sis8172-0
Used Cate: 212.60.16.101
Used Slot: 1 (Addr.: 0x72)

[q] Device Information Overview
[w] LED Test
[e] Memory Test
[r] MLVDS Link Test
[t] Clock Source I (CCP) Test (Frq. 123.45 MHz)
[z] TCLK A Loop Test (Source TCLK A out (Frq. 25 MHz))
[u] TCLK B Loop Test (Source TCLK B out (Frq. 50 MHz))
[i] 'CLK 2 RTM' Test (Frq. 250 MHz)

[a] Port Link Test (press ^C to stop)
[s] SFP Link Test (press ^C to stop)
[d] FMC Test
[f] RTM Test

[y] Discover devices
[x] Select device
[v] Get FMC compatibility check policy
[b] Enable relaxed policy
[n] Enable strict policy

[space] Quit
```

SIS8172 Example Software

- Available in source code

```
clock_dist_control
device_discover
device_information
dfmc_testadp_test
flash_update
memorytest
mlvds_test
port_link_test
rtm_io_test
sfp_link_test
user_irq
Makefile
SIS8172.sh
```

SIS8172 FMC Applications I

Open Hardware (OHWR)

FMC DIO 32 CH TTL A

In-/Output programmable in 8 channel
groups

- General purpose I/O
- SIS8800 Multi Purpose Scaler- like FW implemtation e.g. in combination with DESY motion controller
(Michael Fenner talk)



Picture courtesy Creotech

Available through Creotech

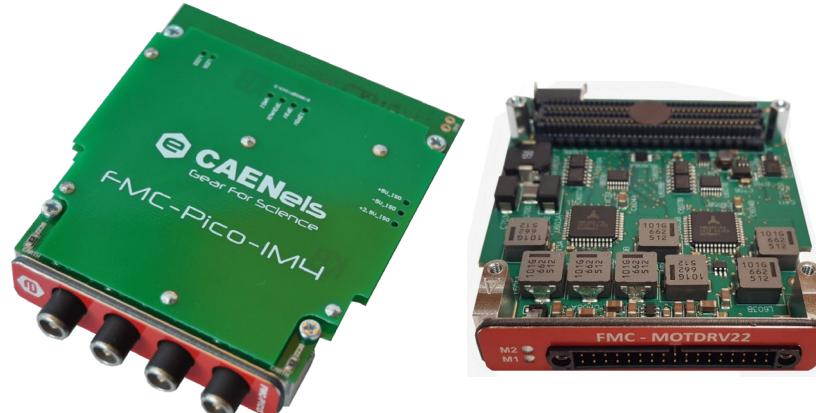
SIS8172 FMC Applications II

PICO-1M4 (CAENELS)
Picoammeter e.g. for Beamlines

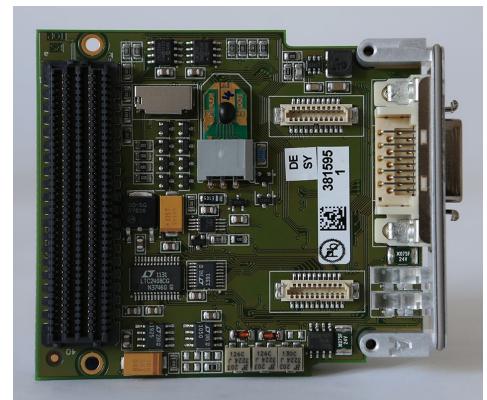
DOSIMON
Radiation Safety

MOTDRV22 (CAENELS)
Motordriver

Digitizer for Spectroscopy
(Talk by Sarmad Adeel)



Pictures courtesy CAENELS



Picture courtesy DESY

SIS8172 RTM Applications I

- Beam Loss Monitor (BLM)
- Machine Protection System (MPS)
- PETRA 4 HF Movement Monitor
- PZT4 Piezo Controller (Low Level Radiofrequency)
- ...
- Any existing Zone Class D1.0 RTM
- Yet to be developed...

SIS8172 RTM Applications II

Example:

Beam Loss Monitor (BLM) RTM
In use at FLASH and XFEL

Readout of 8 PMTs over RJ45

Compatible redesign
envisaged for Petra IV



Picture courtesy DESY

Summary

- Hard- and Firmware development of flexible semi-custom digital MTCA.4 AMC
- Prototype production run of 10 boards
- **Bummer:** EOL ITB AMC connector
- **Otherwise:** Initial revision marketable

First SIS8172 modules shipped in Oct. '22
→ firmware evaluation/integration underway

SIS8172 with OHWR I/O FMC Demo @ booth

Acknowledgements

We would like to thank

- Kay Rehlich
- Timmy Lensch and
- Tim Wilksen

for their valuable input during the project definition phase.

www.struck.de



Questions/Discussion



Quick stopover
option after
WS Dinner Cruise:



Santa Pauli X-Mas Market

Wednesdays open till 11pm

U3 Baumwall 2 stops to St. Pauli