

**PETRA IV.**  
NEW DIMENSIONS

Fast Orbit Feedback Control

# MicroTCA based FOFB System for PETRA IV

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2022-12-07

11<sup>th</sup> MicroTCA Workshop for Industry and Research

**HELMHOLTZ** RESEARCH FOR  
GRAND CHALLENGES

**MSK.**  
Maschine Strahlkontrollen



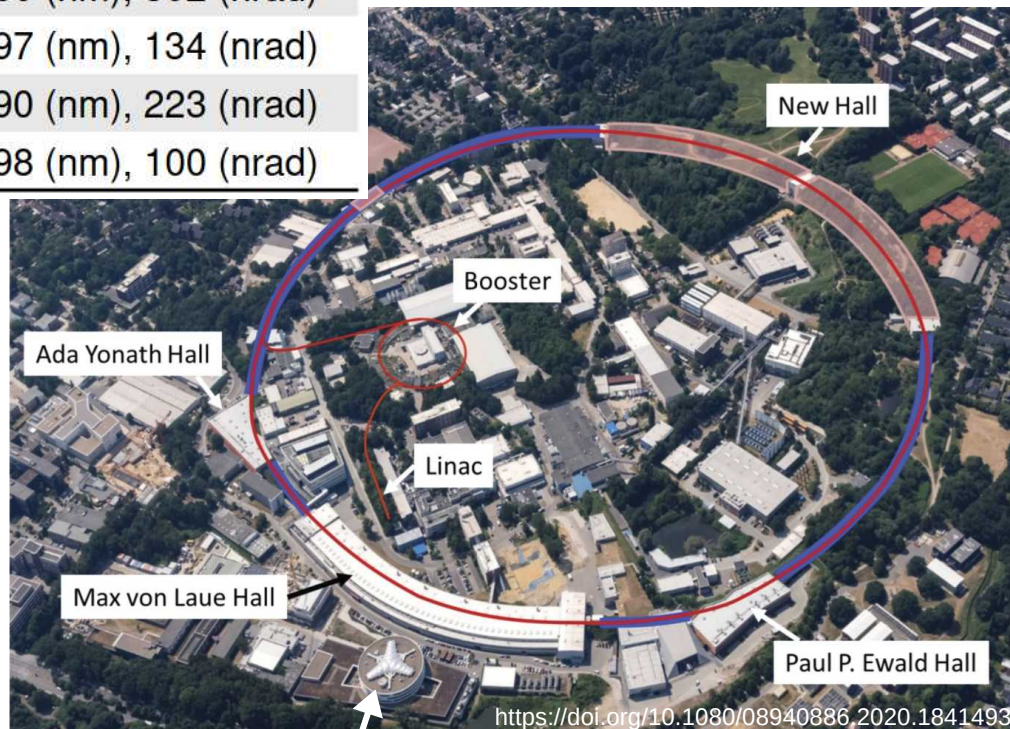
# PETRA IV

## It is not an update but a new machine in PETRA III tunnel

Electron beam stability requirements based upon 10% criteria

| Plane                           | RMSD max.            |
|---------------------------------|----------------------|
| Horizontal at standard cell IDs | 660 (nm), 302 (nrad) |
| Vertical at standard cell IDs   | 297 (nm), 134 (nrad) |
| Horizontal at flagship IDs      | 890 (nm), 223 (nrad) |
| Vertical at flagship IDs        | 398 (nm), 100 (nrad) |

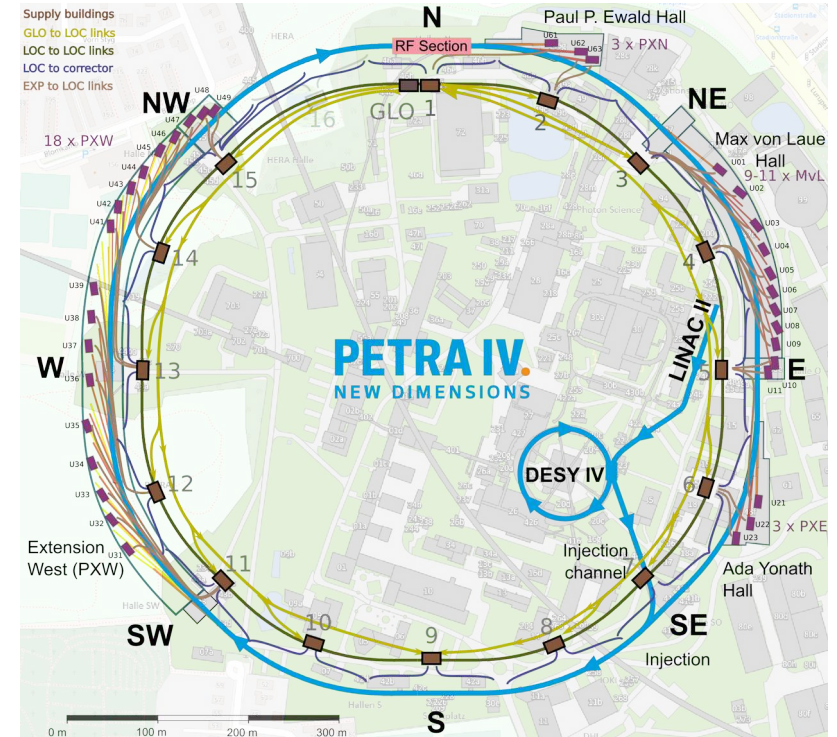
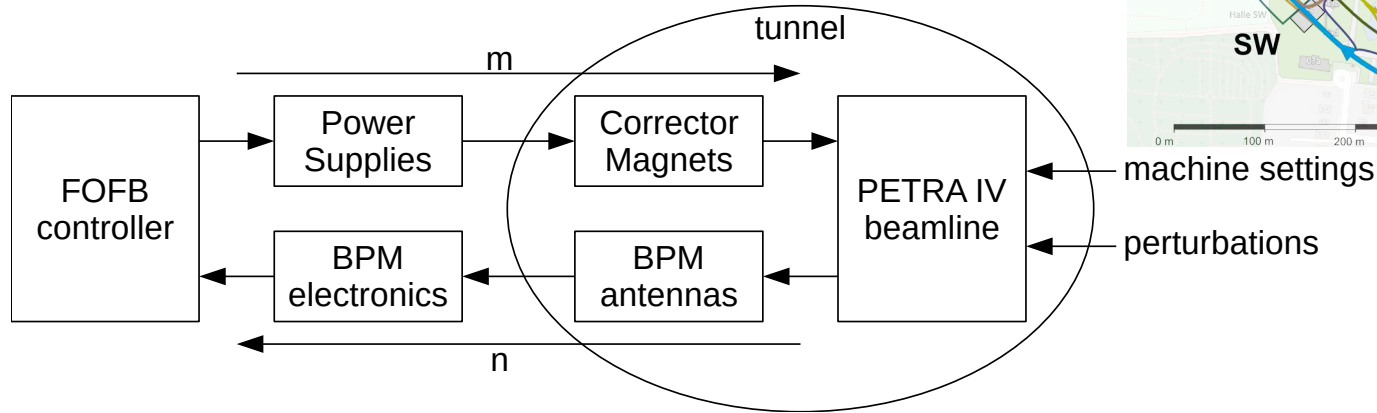
- Aiming for 1 kHz disturbance rejection bandwidth
- RMS deviation on position and pointing angle to be 5-10% of beam size and divergence



# PETRA IV Fast Orbit Feedback

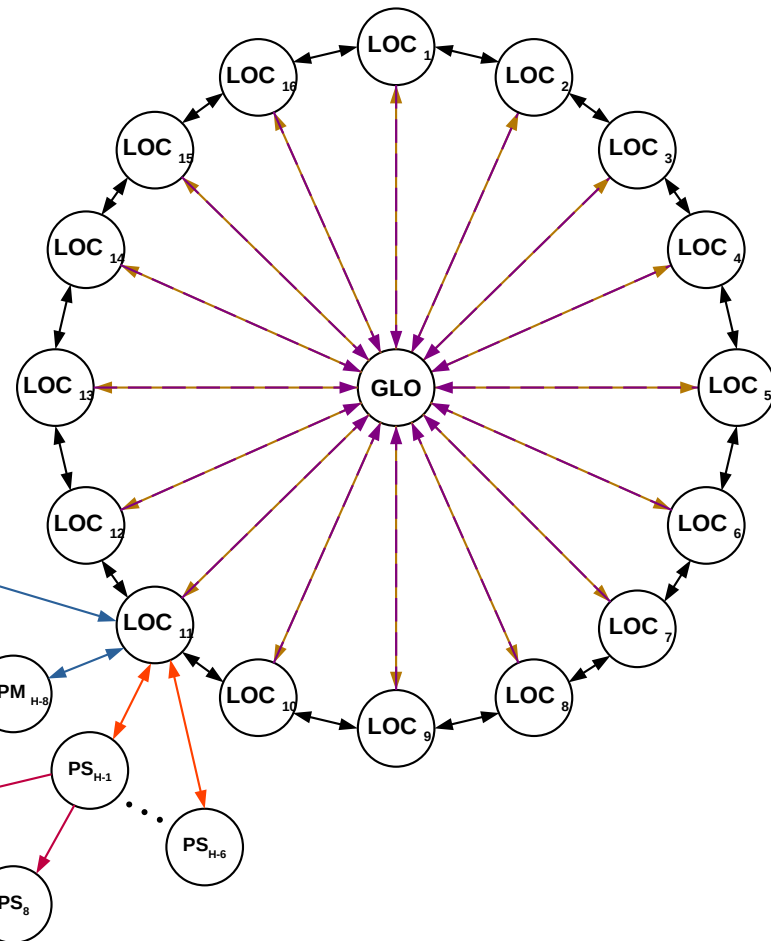
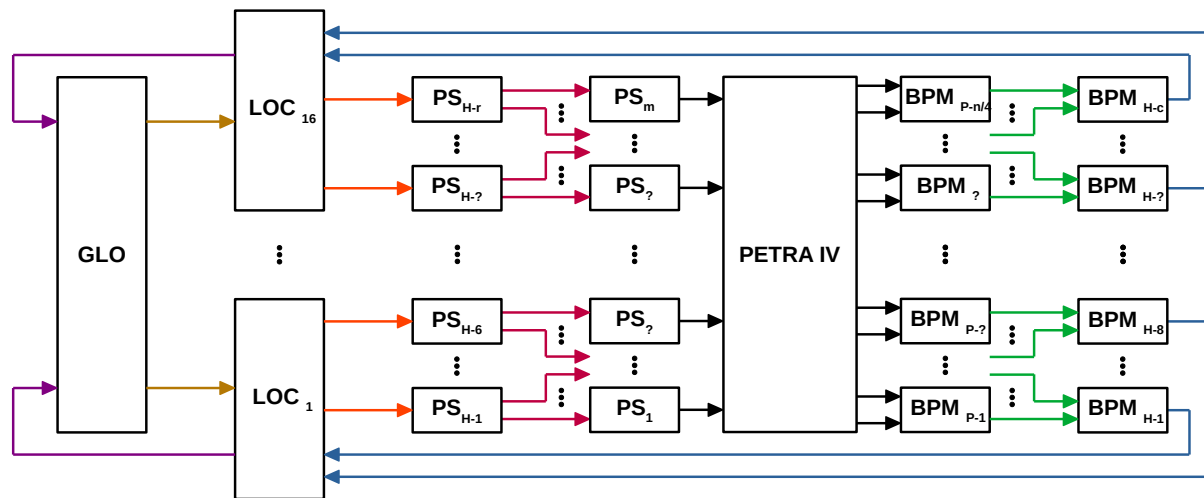
## A Large ( $n \times m$ ) MIMO System

- 789 BPM =  $n/2$
- 522 Fast Corrector Magnets =  $m$
- 15 access paths to the tunnel
- 16 LOCal nodes and a GLObal node
- GLO, LOC-16 and LOC-1 together at North



# PETRA IV Fast Orbit Feedback

## Extended Star Topology

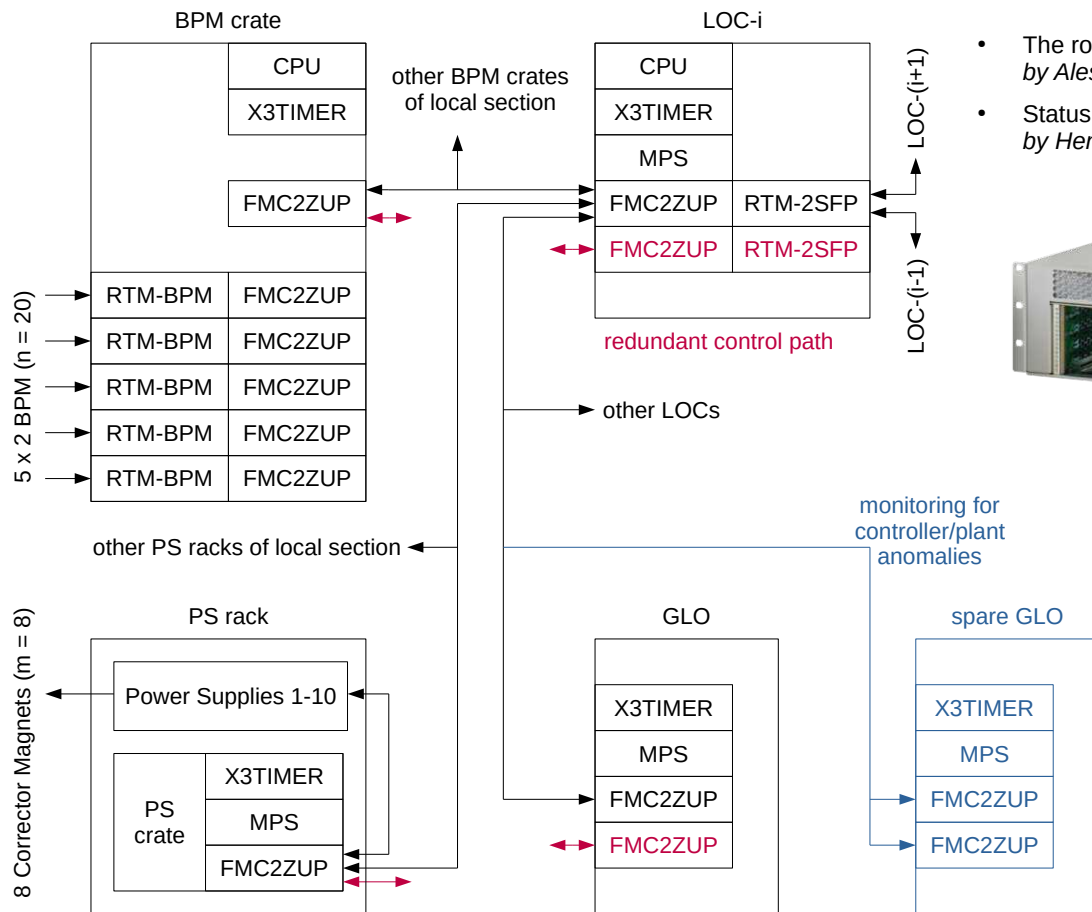


- 8 BPM crates per LOC
  - 5 BPM processors per crate
    - 2 BPM per processor
- 6 PS racks per LOC
  - 8 (+2) PS per rack
    - 1 Corrector Magnet per PS



# PETRA IV Fast Orbit Feedback

## MicroTCA for FOFB controllers, BPM system, Power Supply datahub, timing and safety

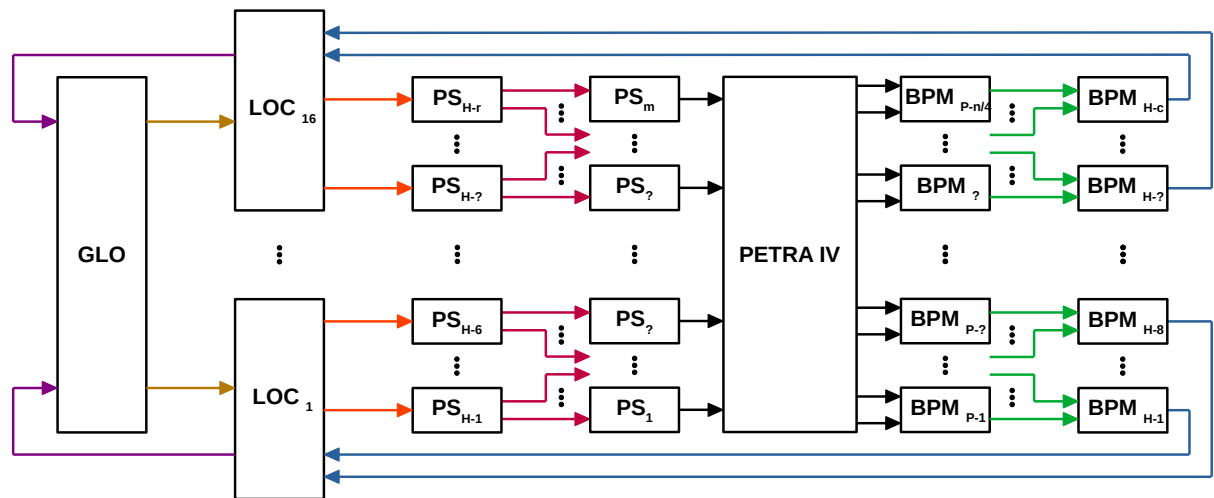


- The role of Libera Brilliance+ in developing the new MicroTCA.4 BPM System for PETRA IV by Ales Bardorfer, Wednesday, Session-5
- Status report on the PETRA IV timing system development by Hendrik Lippek, Thursday, Session-7



# PETRA IV Fast Orbit Feedback

## Point to Point Links



 **Aurora 8B/10B**  
 6.25 Gbps single lane  
 4 bytes lane width  
 framing interface with CRC  
 user\_clk @ 156.25 MHz  
 41 clock cycles latency

 **Aurora 64B/66B**  
 10 Gbps single lane  
 8 bytes lane width  
 framing interface with CRC  
 user\_clk @ 156.25 MHz  
 55 clock cycles latency

|              | # | n/4           | c           | 16          | 1          | 16         | r           | m            |
|--------------|---|---------------|-------------|-------------|------------|------------|-------------|--------------|
| node         |   | BPM processor | BPM datahub | LOC FOFB    | GLO FOFB   | LOC FOFB   | PS datahub  | Power Supply |
| transmission |   | backplane     | optical     | optical     | optical    | optical    | optical     | optical      |
| payload      |   | 23040 Bytes   | 17408 Bytes | 15616 Bytes | 6400 Bytes | 7680 Bytes | 15360 Bytes |              |
| throughput   |   | 3200 Gbps     | 1240 Gbps   | 155 Gbps    | 155 Gbps   | 931 Gbps   | 3860 Gbps   |              |
| latency      |   | 262 ns        | 352 ns + Δ  | 6 us        | 6 us       | 352 ns + Δ | 262 ns      |              |

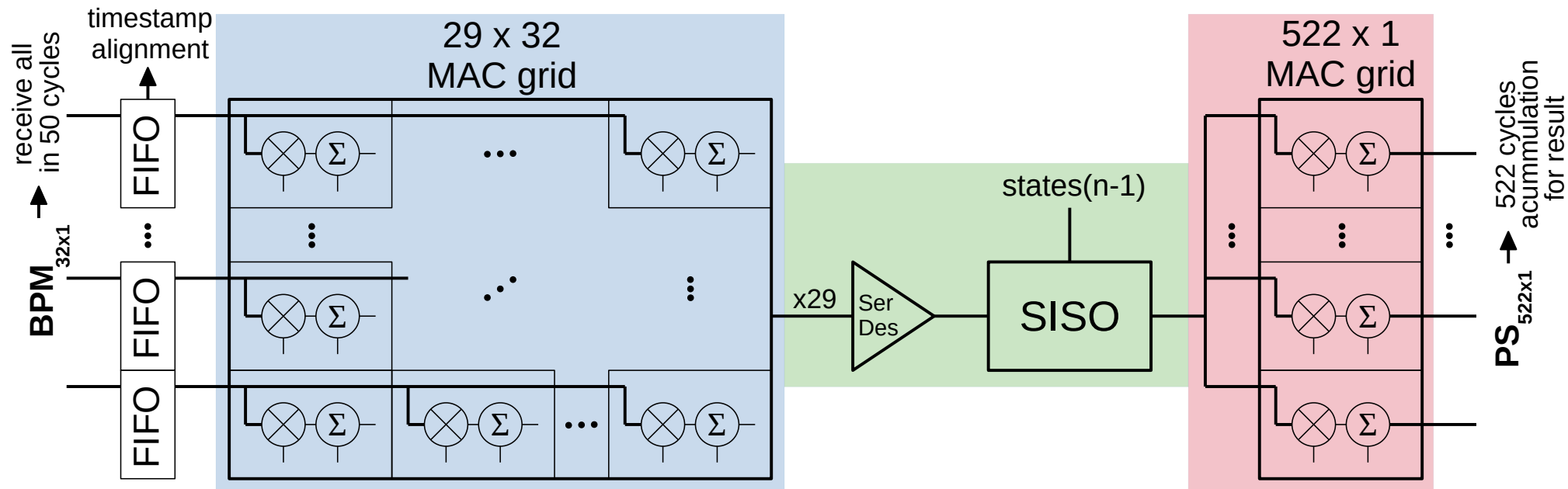
# PETRA IV Fast Orbit Feedback

## Controller Latency

$$\left[ \Sigma^{-1} U^T \right]_{522 \times 1578} * BPM_{1578 \times 1} = \lambda_{522 \times 1}$$

$$\left[ V^T \right]_{522 \times 522} * OUT_{522 \times 1} = PS_{522 \times 1}$$

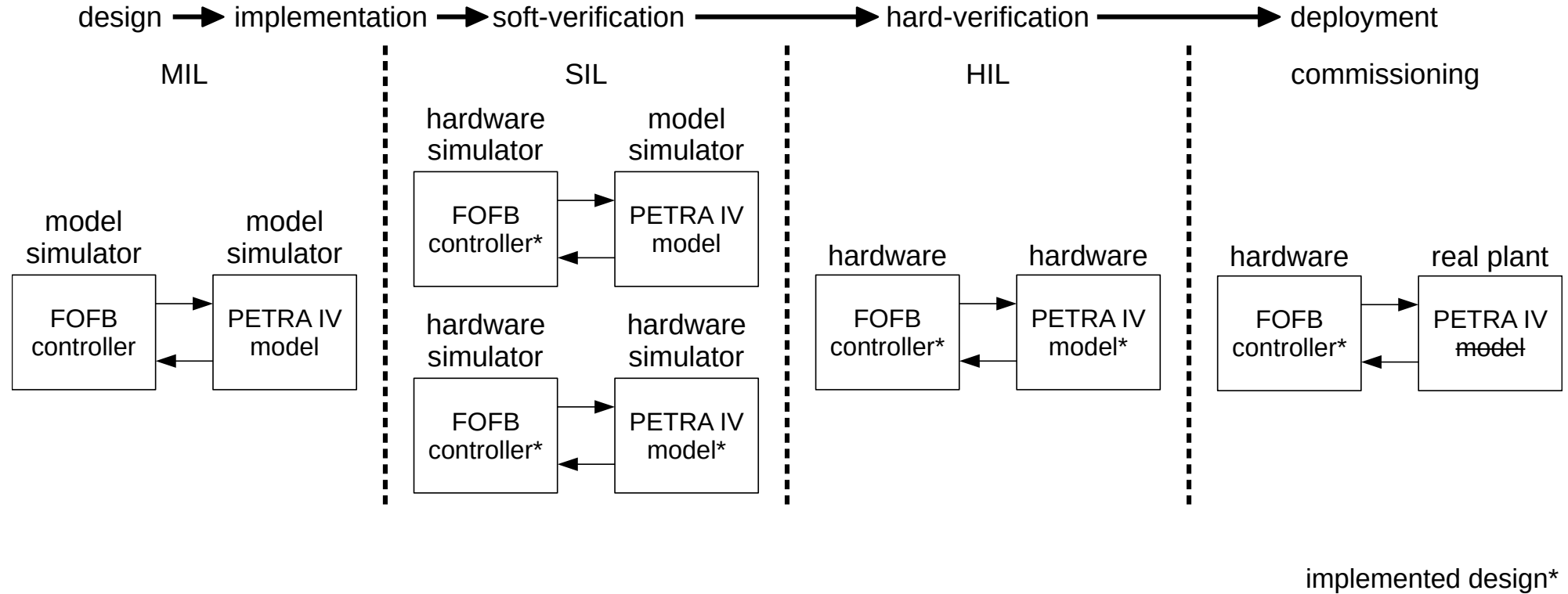
$$\lambda_{522 \times 1} - REF_{522 \times 1} \Rightarrow SISO_{522 \times 1} \Rightarrow OUT_{522 \times 1}$$



29 parallel row operation with resource sharing

# PETRA IV Fast Orbit Feedback

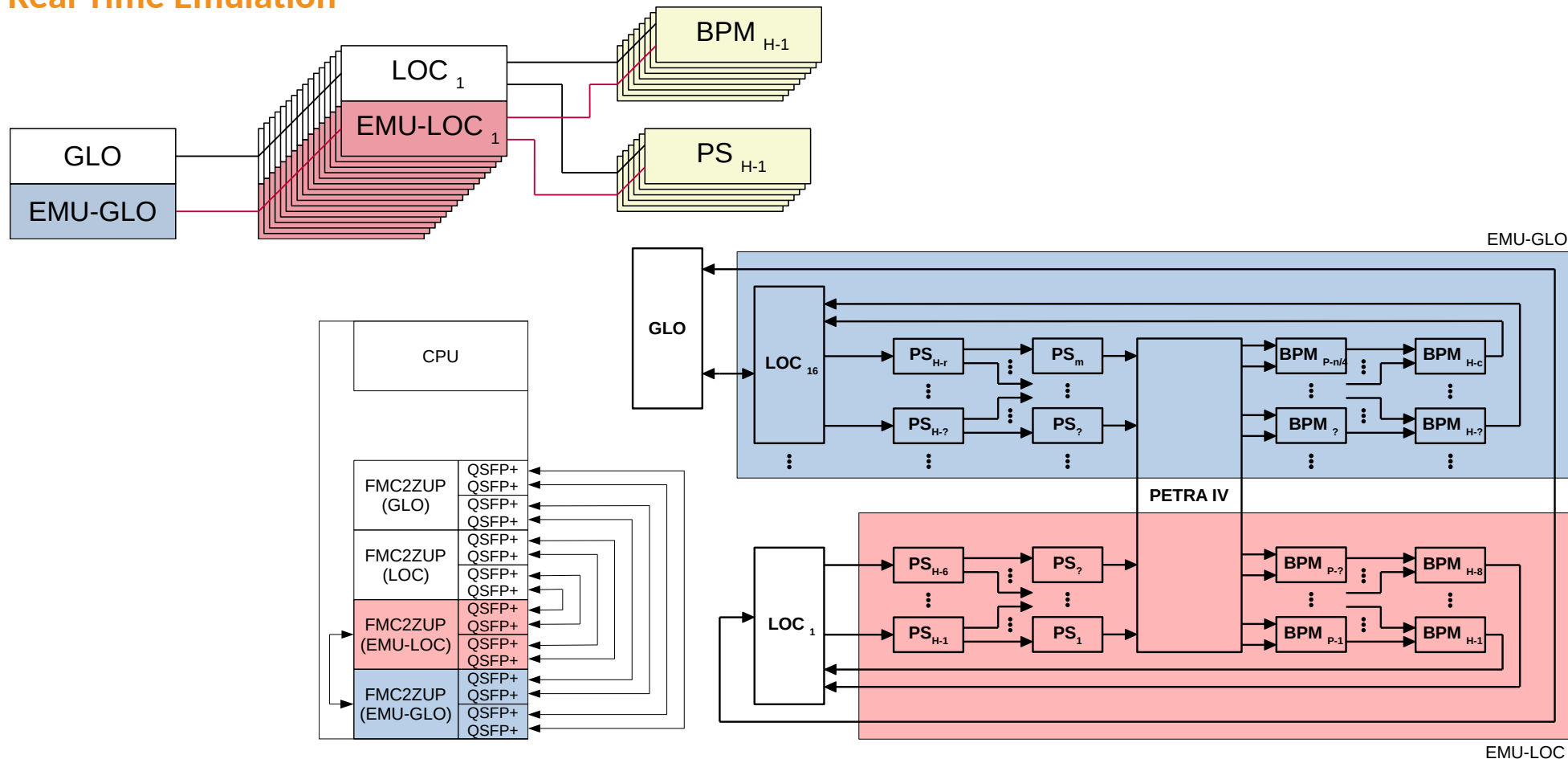
## Model Based Design

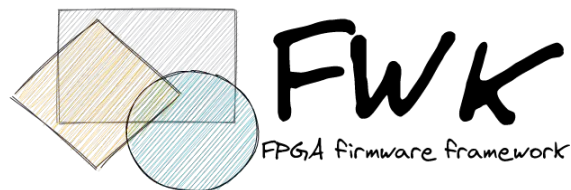




# PETRA IV Fast Orbit Feedback

## Real-Time Emulation





[gitlab.desy.de/fpga/fw/fw](https://gitlab.desy.de/fpga/fw/fw)

- Open Source FPGA Framework at MSK-DESY  
*by Cagil Gumus, Thursday, Session-7*



[github.com/ChimeraTK](https://github.com/ChimeraTK)

- ChimeraTK: Teil 1 & 2  
*by Martin Killenberg, Tuesday, Tutorial Sessions*
- Extension of the Python Bindings for the ChimeraTK DeviceAccess Library  
*by Christian Willner, Thursday, Session-8*

# Thank you.

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**DESY.**

Deutsches  
Elektronen-Synchrotron

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