Status of FOFB upgrade at SOLEIL

MTCA workshop 2022

Romain BROUCQUART

December 7th 2022

SOLEIL Synchrotron

3rd generation light source

France, 20km south of Paris.

In operation since 2006.

29 beamlines in operation.

Energy	2,75 GeV
Circumference	355 m
Revolution period	1,18 µs
Number of Cells	16
Beamlines	29

Upgrade to SOLEIL-II

TDR ongoing.

Shutdown scheduled for 2027.

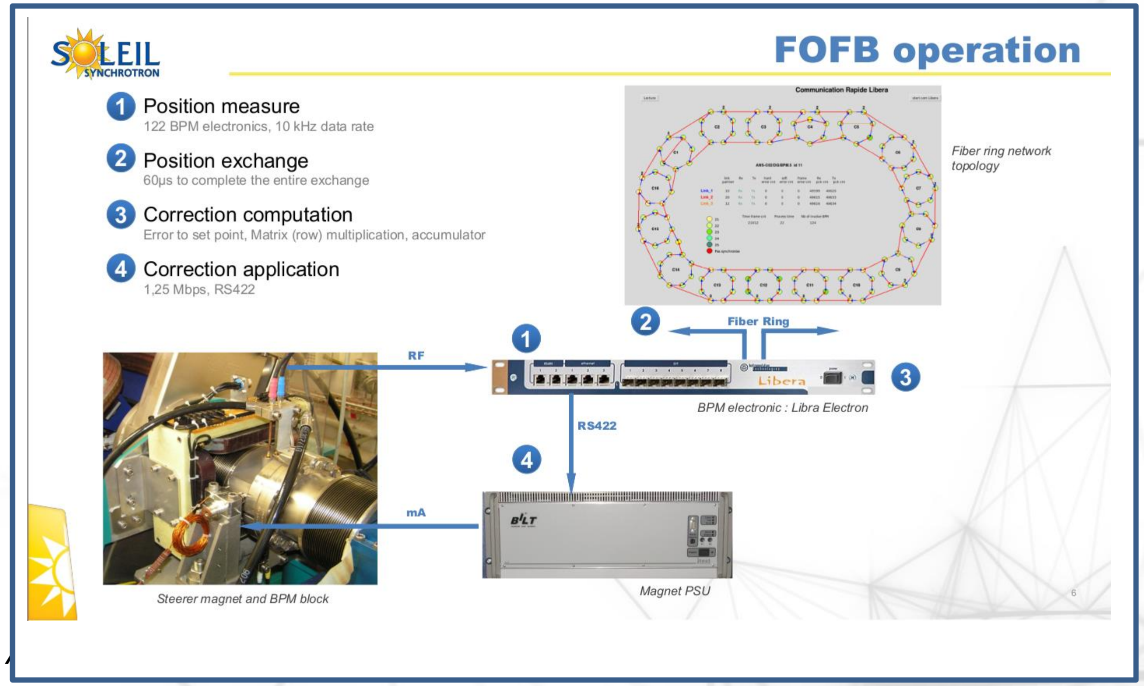
Fast Orbit FeedBack upgrade ahead of the long technical shutdown.

Fast Orbit Feedback System

Compensate quick but small perturbations on the storage ring orbit.

Connected to many devices and services: 122 BPM, 100 PSC, Timing...

Dedicated fast network.



Glossary

BPM: Beam Position Monitor

PSC: Power Supply for Correctors

FOFB Upgrade

Fast Orbit Feedback Upgrade Challenges

Follow boundary systems (BPM, timing, PSC) and machine upgrade.

Host future correction algorithms and fast lattice identification features.

Performances improved (correction bandwidth).

A new platform to support these goals

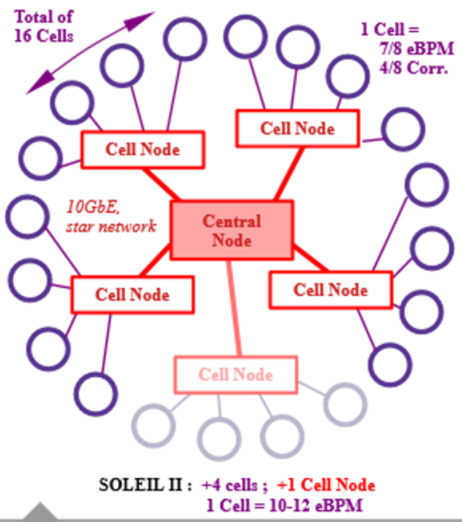


Figure 1 - Proposed two level star topology. As SOLEIL II increases the number of systems, the network will expand by adding a Cell Node.

New Platform for FOFB

Hardware

- **MTCA system**
- **Custom RTM board**
- **Star dedicated network, two levels**

FPGA Firmware

- **In house development**
- **Rely on DESY FWK**

Embedded software

- **OPCUA server**
- **Python prototype**
- **ChimeraTK for production**

Control software

- **Tango OPCUA client**
- **Tango devices for interfaces**

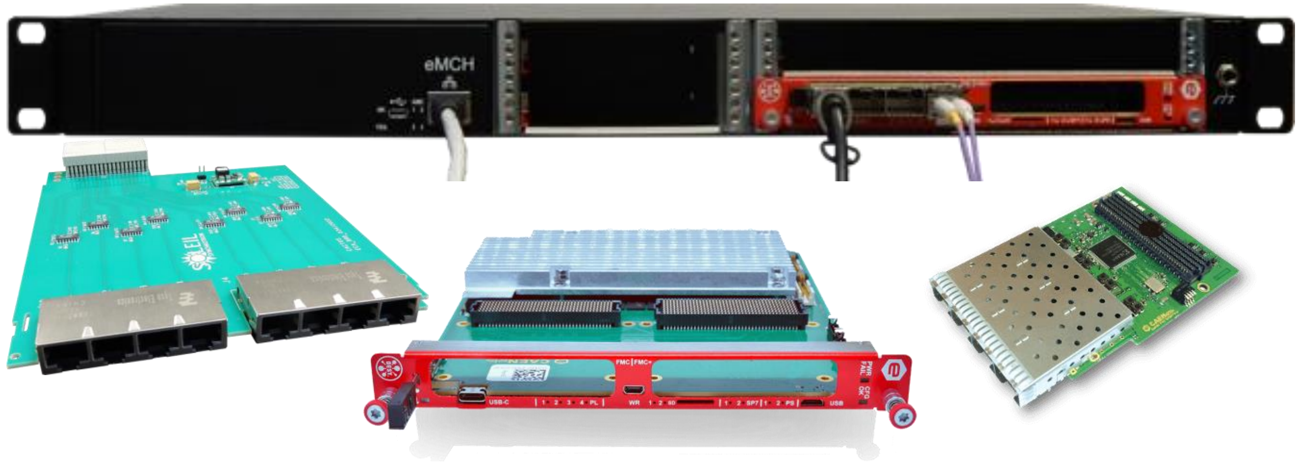
	Actual FOFB	Future FOFB
# BPM	122	180
# Corr. PSU	50 H & V	?
Data rate	10 kHz	100 kHz
Correction Bandwidth	150 Hz	1 kHz
Latency (communication + computation)	100 µs	10 µs
Stability	10% of beam size 20 µm H ; 0,8 µm V	2-5% of beam size 50 nm H & V
Algorithm	PI, 122x50 matrix from SVD + Tikhonov	?

Hardware: MTCA platform

Same platform for Cell Nodes and Central Node

- nVent NATIVE-R1
  - 1U simple crate
  - no PCIe switch, point ot point backplane
  - eMCH
- DESY/CAENels DAMC-FMC2ZUP
  - FPGA Zynq UltraScale +
  - 4 GB DDR4, 2 slots FMC
  - Timing interface
- CAENels 4SFP+ FMC
- Custom RTM

Electronics installed in the lab, with Libera Electron

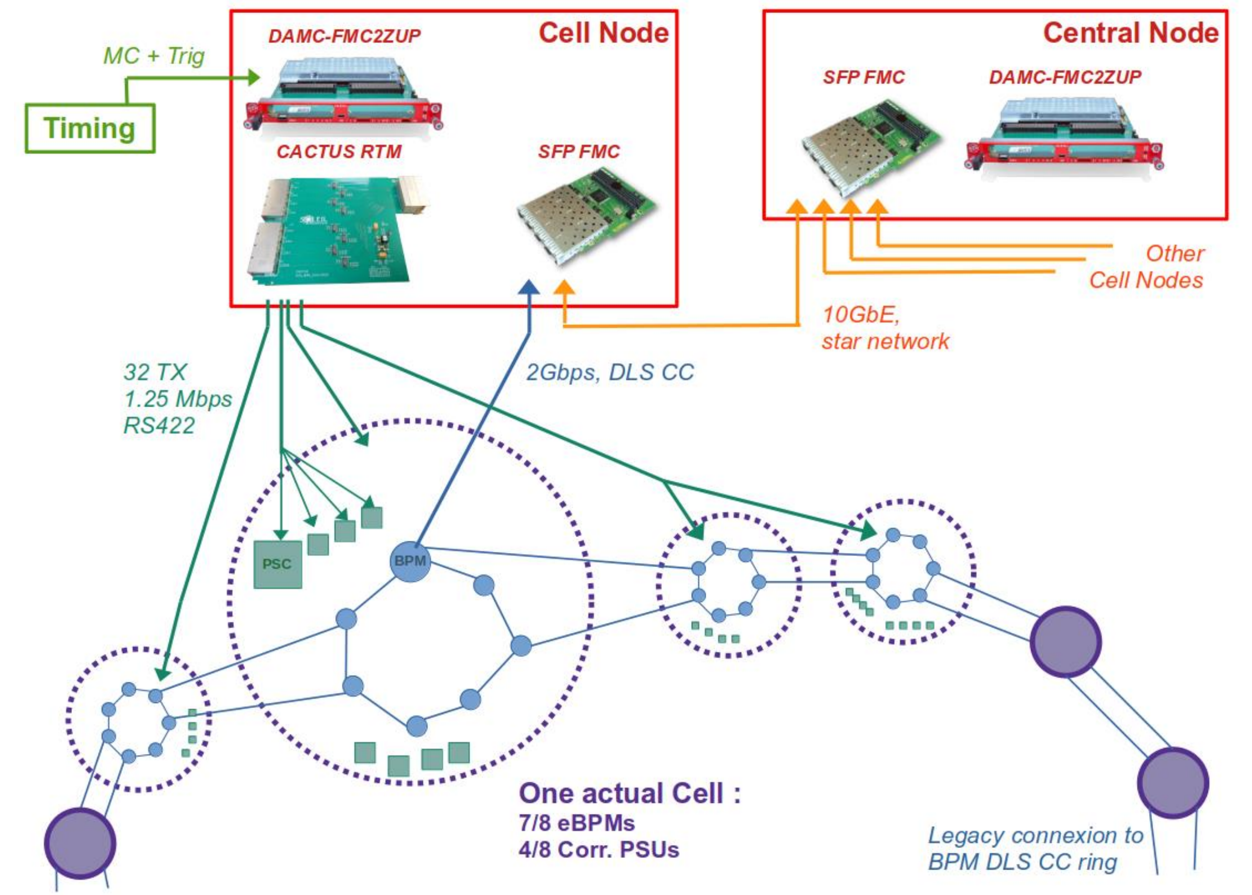


MTCA platform for CellNodes and Central Nodes.

Hardware: Dedicated network

Connexion to boundary systems

- Data flow
  - Read BPM custom protocol (Diamond CC).
  - Converge position to Central Node, Dispatch correction command back to Cell Nodes.
  - 10GbE, custom position/correction packet carried by Ethernet Frame
  - Send UART RS422 command to PSC.
- Date with Machine Clock and Trigger.
- Fast stream capture
  - Still working on solutions
- Future Cell
  - 10-12 BPM. Unknown protocol, interface.
  - Unknown number of corrector, protocol, interface.
  - 4 more Cells: add a Cell Node.

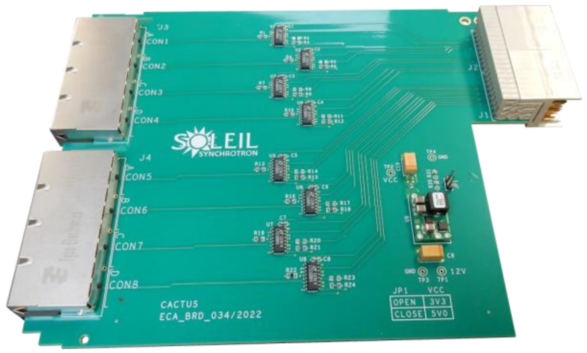


System integration. One Cell node is connected to 4 cells.

Hardware: Custom RTM board

CACTUS RTM

- Very simple RTM board
  - 32 TX Differential Drivers (RS422)
  - Output on RJ45 sockets (4 pairs by socket)
  - Will be used until PSC upgrade (2027)
- A first prototype... not ambitious enough !
  - MTCA management dropped
  - Handshake and power bring-up impossible.
  - Validated with external power
- Boards with corrected design expected for January

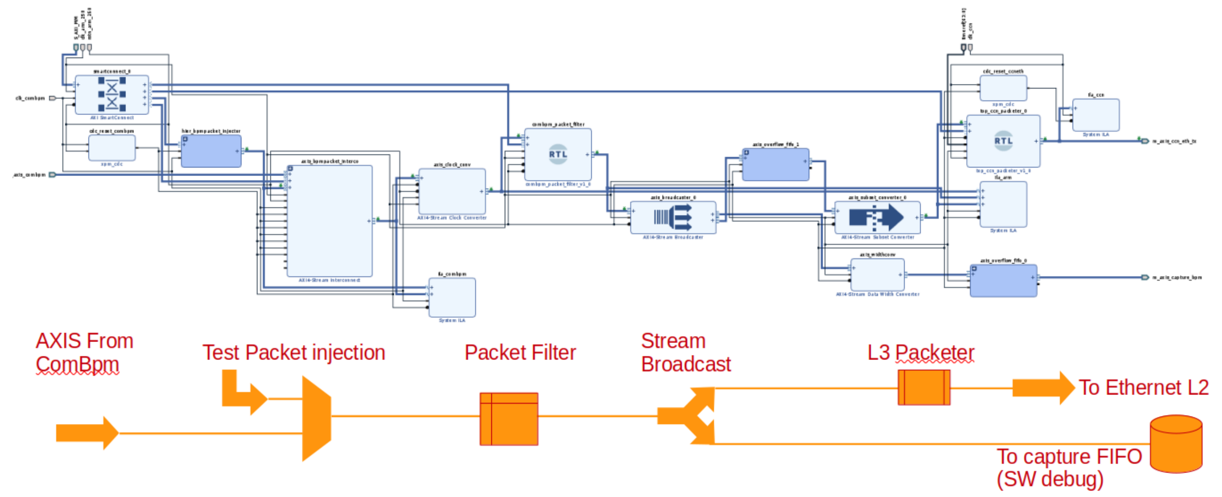


CACTUS: Custom RTM board for corrector PSU communication

FPGA Firmware

Using DESY's FWK

- Project automation
  - Coherence, split system in modules
  - Deployment and version control
  - Memory map, access eased (DESYRDL, ChimeraTK)
- Still using BlockDesign
  - Data flow chain easy to view
  - Debug point easy to insert
  - AXI-MM and AXIS easy wiring
  - Xilinx AXI-MM interconnection still used
- Two project created: CellNode and CentralNode
  - 7 modules redacted (ComBpm, ComPSC, Ethernet packeter...)
  - Common module in both project
  - Will soon Use DESY BSP for our project (DAMC-FMC2ZUP)



Cell Node upstream Block design, and AXIS synopsys.

See "Open Source FPGA Framework at MSK-DESY" by Cagil Guemues, Thursday, Session 7

Embedded software

Embedded Linux build with YOCTO

Ease development

SSH connexion, on board python, access to memory bus...

Planning to go with ChimeraTK

Easy access to FPGA register

Access to FPGA registers via AXI-MM

Access AXI-MM via UIO Device Access

Very simple application core

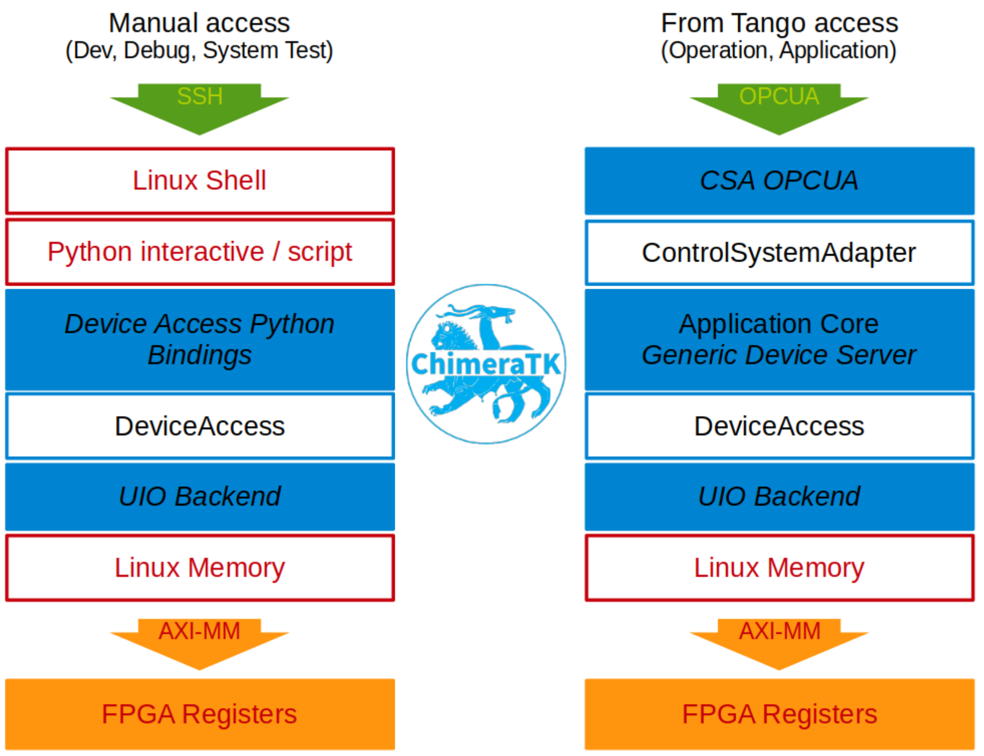
Almost only direct connect to CSA

Generic Device Server

OPCUA server Control System Access: quickly connect to TANGO.

This will help prototyping future features.

Python OPCUA server implementation until CSA OPCUA for ARM platform available.



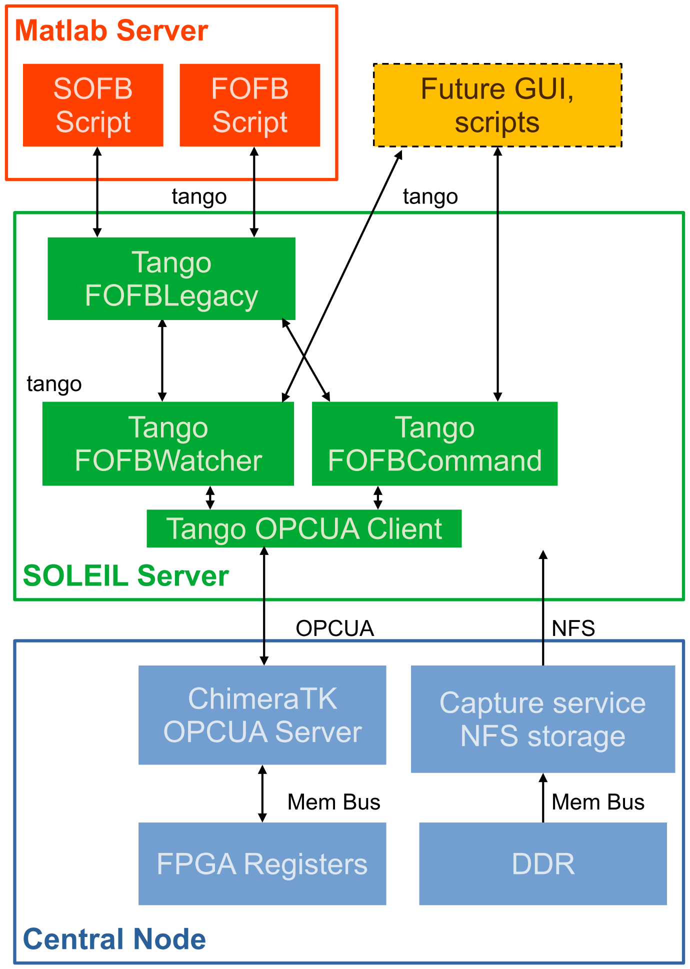
Envision Embeded softwares using ChimeraTK. Gives access to FPGA register to user via SSH or via tango)

See
"Yocto Embedded Linux for SoC based AMCs – Latest developments for demanding applications" *by Patrick Huesmann,*
" Extension of the Python Bindings for the ChimeraTK DeviceAccess Library" *by Christian Willner,*
Thursday, Session 8

Control software

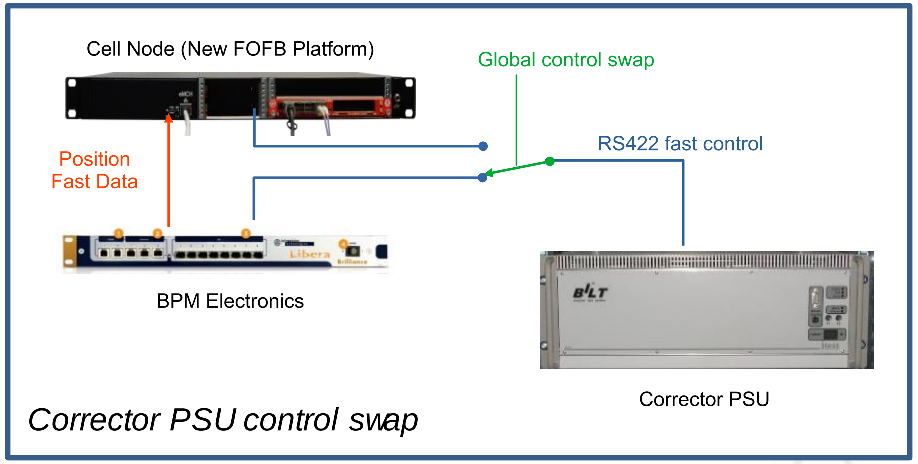
Integrate in SOLEIL TANGO control system

- Generic, dynamic TANGO OPCUA client
- Device TANGO Watcher/Command.
  - They can operate on other system accessible via Tango.
- Simple Translation Device to legacy Matlab
  - Operation GUI, lattice physics
- For data capture (snapshot, not streaming)
  - Control the capture via Tango
  - Output the data outside Tango
  - Use file storage ?



Envisioned Control software stack

Project Timeline



Corrector PSU control swap

Original FOFB Running → **New platform FOFB Running**

- **August 2022** – Reception of electronics
- **May 2022** – CellNode spying BPM network
- **December 2022** – One CellNode and CentralNode connected
- **March 2023** – 4 CellNodes and CentralNode connected. Corrector PSU control swapable new/original FOFB
- **April 2023** – Dedicated machine sessions for closed loop tests
- **July 2023** – End of FOFB commisionning
- **2025** – New BPM electronics
- **2026** – New features available (lattice parameters fast measurment)

Many thanks to...

SOLEIL staff involved in the project

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Thank you !