PETRA IV.
NEW DIMENSIONS

Conceptual Design of the Multi-Bunch Feedback for the Synchrotron Radiation Source PETRA IV based on the Xilinx Zynq UltraScale+ RFSoC

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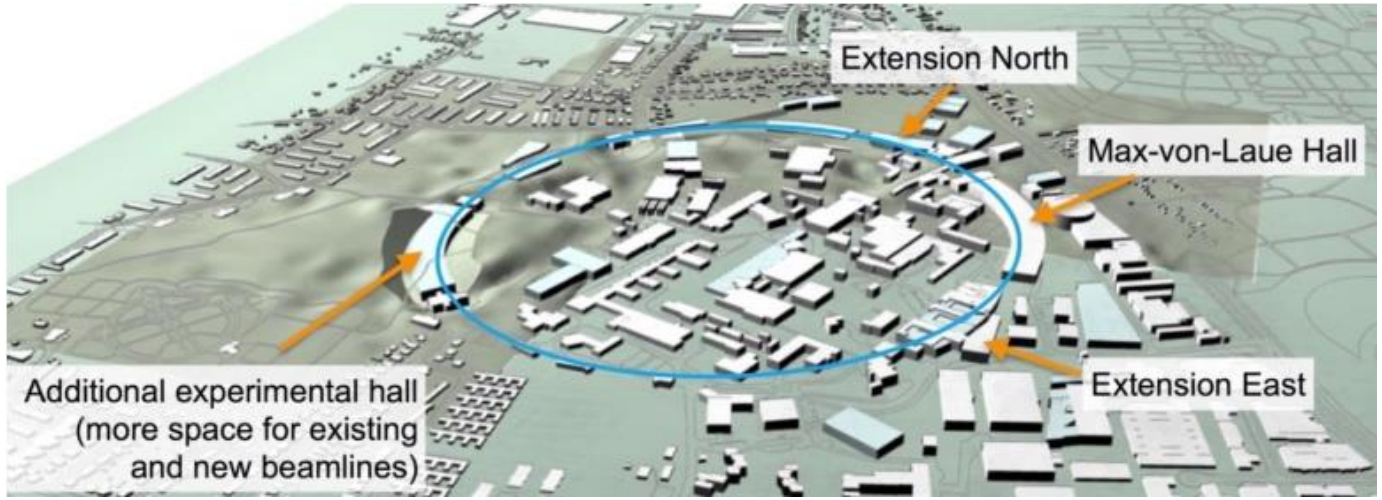
Agenda

- Short introduction to the Multi-Bunch Feedback (MBFB) of PETRA IV
- MicroTCA.4 based electronics for the MBFB (concept)



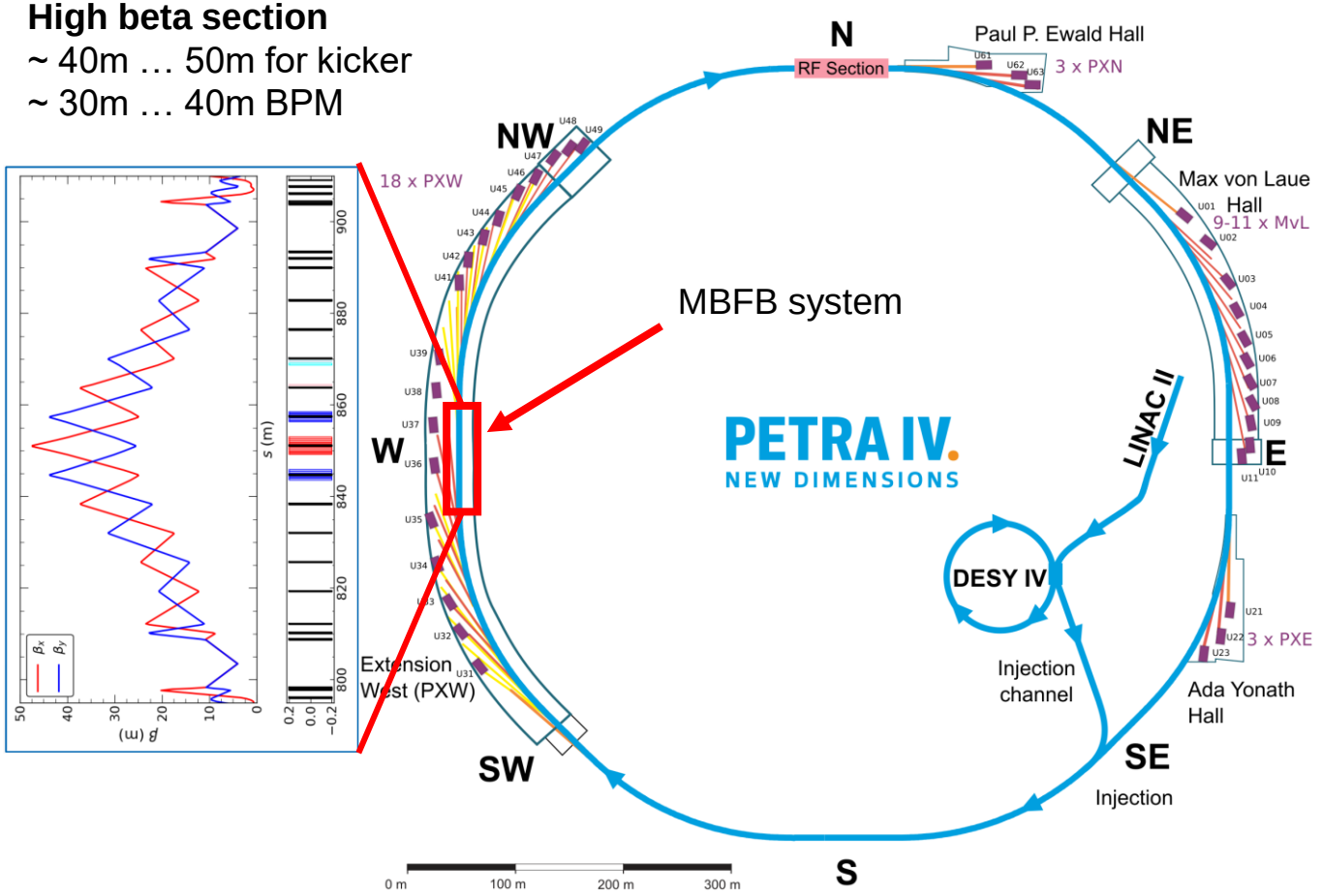
MBFB parameters

Requirements and infrastructure

PETRA IV design parameters in the brightness (B) and timing (T) mode and the requirements for the T-MBFB

Design Parameter	Value
Energy E	6 GeV
Revolution frequency f_{rev}	130.12 kHz
Emittance (ϵ_x / ϵ_y)	< 20 / 4 pm rad (**B**) / < 50 / 10 pm rad (**T**)
Total current I	200 mA (**B**), 80 mA (**T**)
Number of bunches M	max. 3840 (**B**), 80 (**T**)
Bunch current I_b	<70 μA (**B**), 1 mA (**T**)
Bunch spacing T_{rep}	2 ns (**B**), 96 ns (**T**)
Bunch length σ_t	45.7 ps (**B**), 64.3 ps (**T**)
Betatron freq. (f_x / f_y)	23.4 kHz / 35.2 kHz
T-MBFB det. bandwidth	> 500 MHz
T-MBFB det. resolution	<1 µm at ±1 mm det. range
T-MBFB damping time τ	< 40 turns (A_p < 200 µm)

High beta section
~ 40m … 50m for kicker
~ 30m … 40m BPM

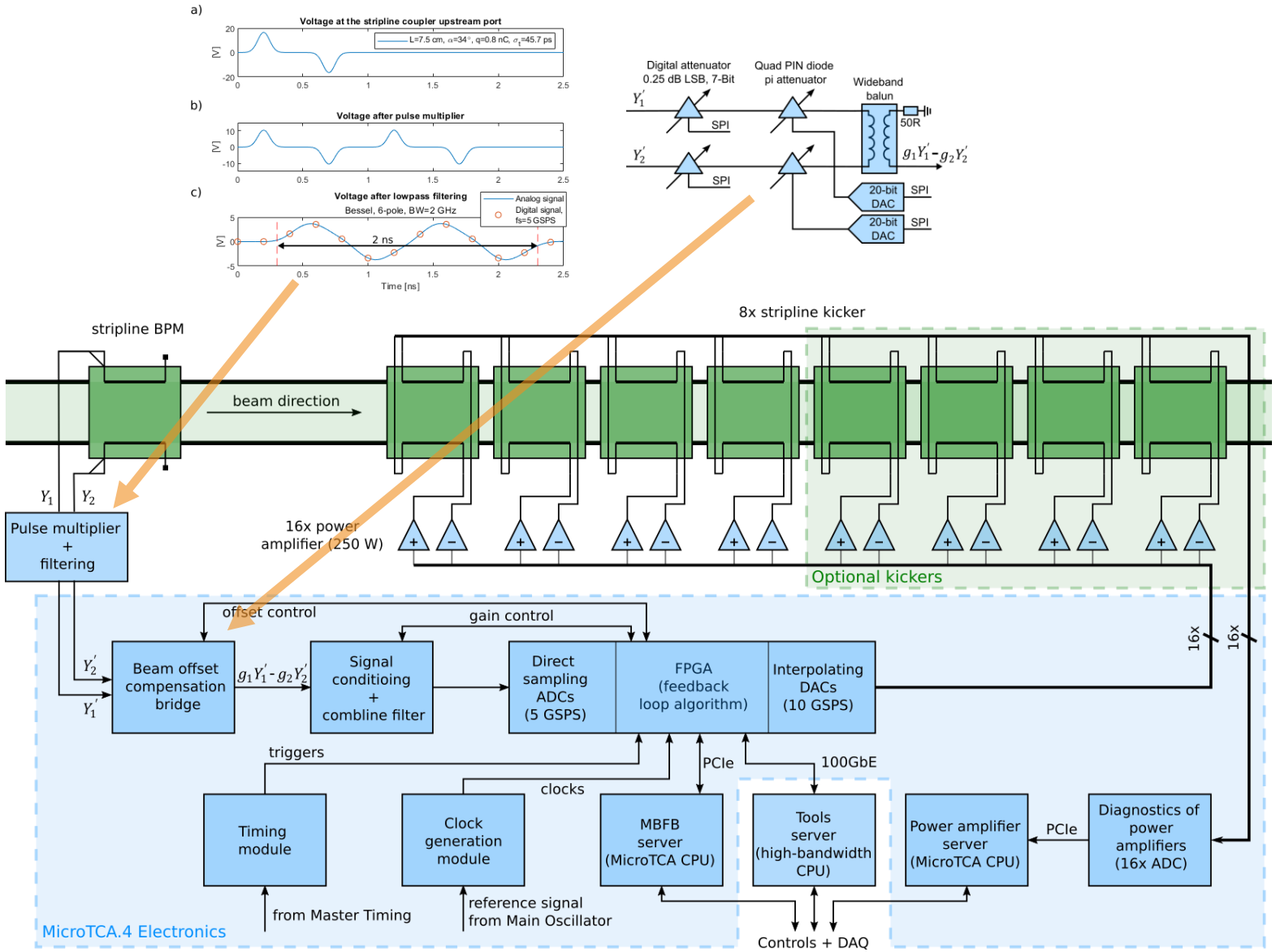


MBFB architecture

Feedback signal flow and diagnostics

- Feedback signal flow
  - Stripline BPM (1 GHz)
  - Pulse multiplier and filtering (increase SNR)
  - Beam offset compensation (increase of dynamic range and resolution)
  - Signal conditioning and combline filter
  - 5 GSPS ADCs
  - Processing
  - 10 GSPS DACs

  } DAMC-DS5014DR
  - High power amplifiers (HPAs)
  - Stripline kickers (DC-250 MHz)
- Diagnostics and tools for machine studies
  - Diagnostics of kick voltage of HPAs
  - Diagnostics of bunch phase, charge, position, profile
  - Tune measurement, growth-damp analysis, emittance control



S. Jablonski, H.T. Duhme, B. Dursun, J. Klute, S. H. Mirza, S. Pfeiffer, H. Schlarb, Conceptual Design of the Transverse Multi-Bunch Feedback for the Synchrotron Radiation Source PETRA IV, Proc. of IBIC2022, Kraków, Poland, Sep. 2022.

MBFB electronics

MicroTCA.4 modules

Modules for the feedback:

- DRTM-MBFB-CSI – beam offset compensation
- DRTM-MBFB-FE – front-end
- DAMC-DS5014DR – ADC / DAC / processing board
- DAMC-FMC2ZUP

Modules for the HPA diagnostics:

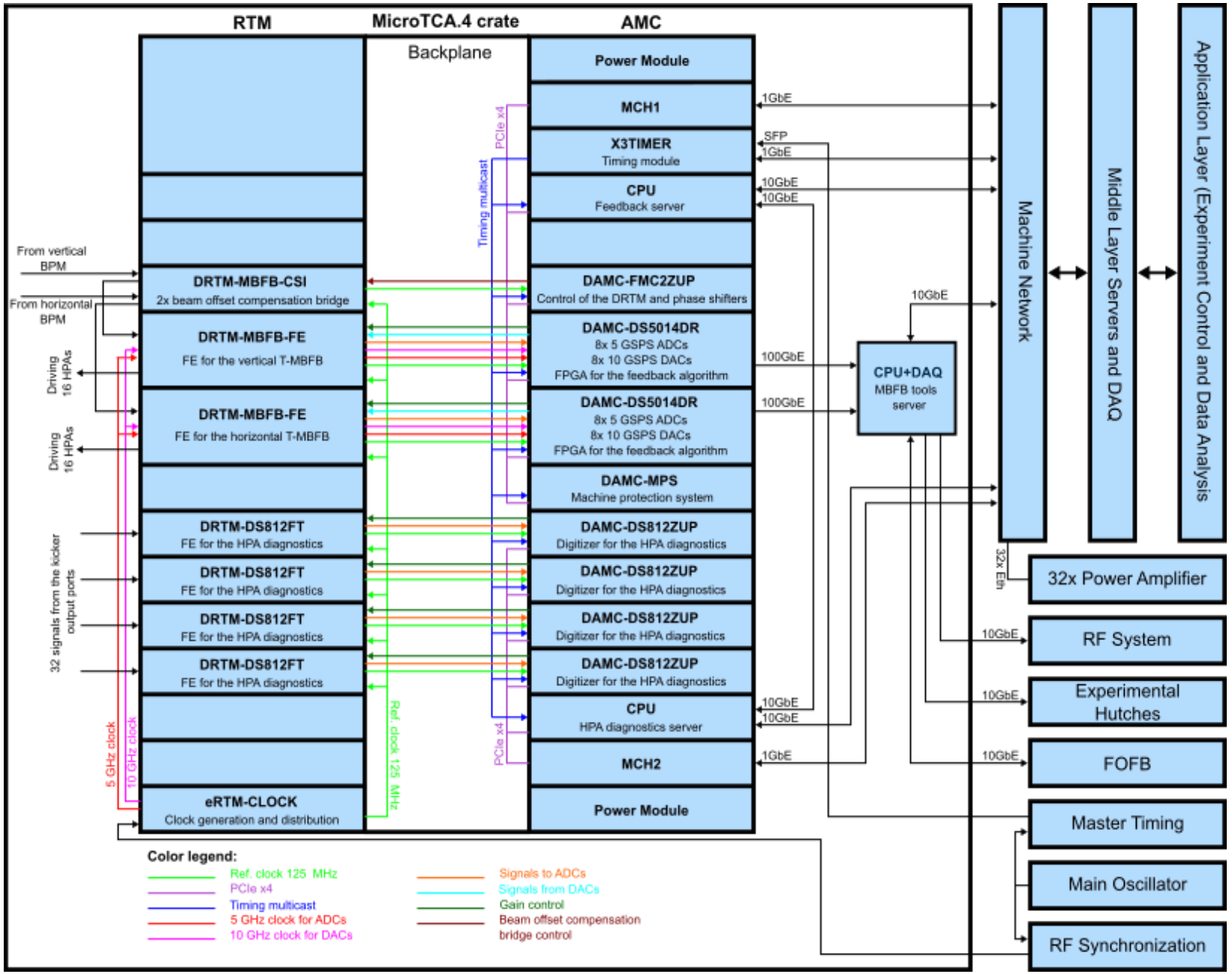
- DAMC-DS812ZUP – ADC board
- DRTM-DS812FT – front-end

Modules for the timing and clocks:

- eRTM-CLOCK
- X3Timer (H. Lippek)

Support modules:

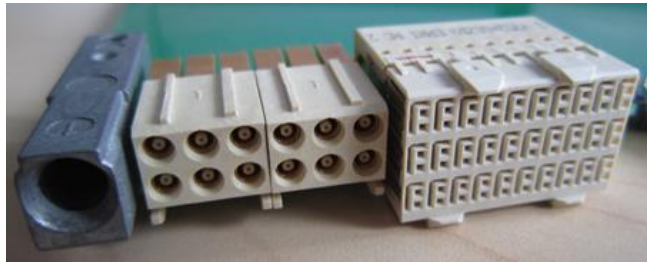
- MCH, CPU, Power module
- MPS

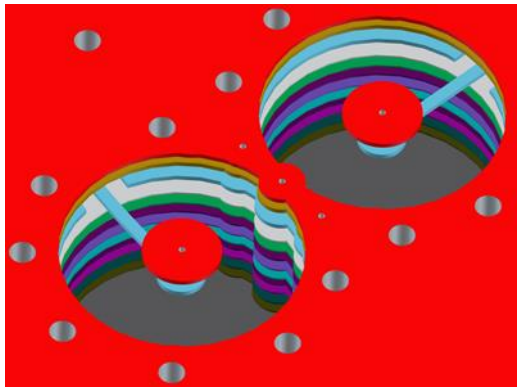


New Zone3 Class RF1.1 recommendation

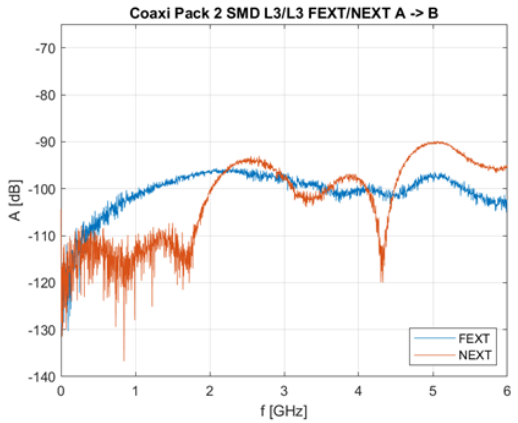
Differential pins for DACs

- Differential output DACs in the Class RF1.1 instead of Gbit-Links in the Class RF1.0
- Single-ended signals up 6 GHz, high isolation between channels





Courtesy of J. Zink



Courtesy of J. Zink

Class RF1.0

		Digital Clock IO	Digital fixed IO	Digital Clock Input	Digital user IO		Standard Gbit-Links			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D7-	RF-CLK3-	D5-	D2-	GBT7-TX-	GBT4-TX-	GBT1-TX-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D7+	RF-CLK3+	D5+	D2+	GBT7-TX+	GBT4-TX+	GBT1-TX+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D6-	RF-CLK1-	D4-	D1-	GBT6-TX-	GBT3-TX-	GBT0-TX-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D6+	RF-CLK1+	D4+	D1+	GBT6-TX+	GBT3-TX+	GBT0-TX+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	D3-	D0-CC-	GBT5-TX-	GBT2-TX-	GBT0-RX-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	D3+	D0-CC+	GBT5-TX+	GBT2-TX+	GBT0-RX+	PWRA2	PWRA1
		Single Ended Analog Signals									
J31		3	2	1							
	B	ADC-IN7	DAC-OUT1	DAC-OUT3							
	A	ADC-IN6	DAC-OUT0	DAC-OUT2							
J32		3	2	1							
	B	ADC-IN1	ADC-IN3	ADC-IN5							
	A	ADC-IN0	ADC-IN2	ADC-IN4							

Table 1: Zone 3 - Class RF1.0 pin assignment J30, J31 and J32 connector, AMC side view

Class RF1.1

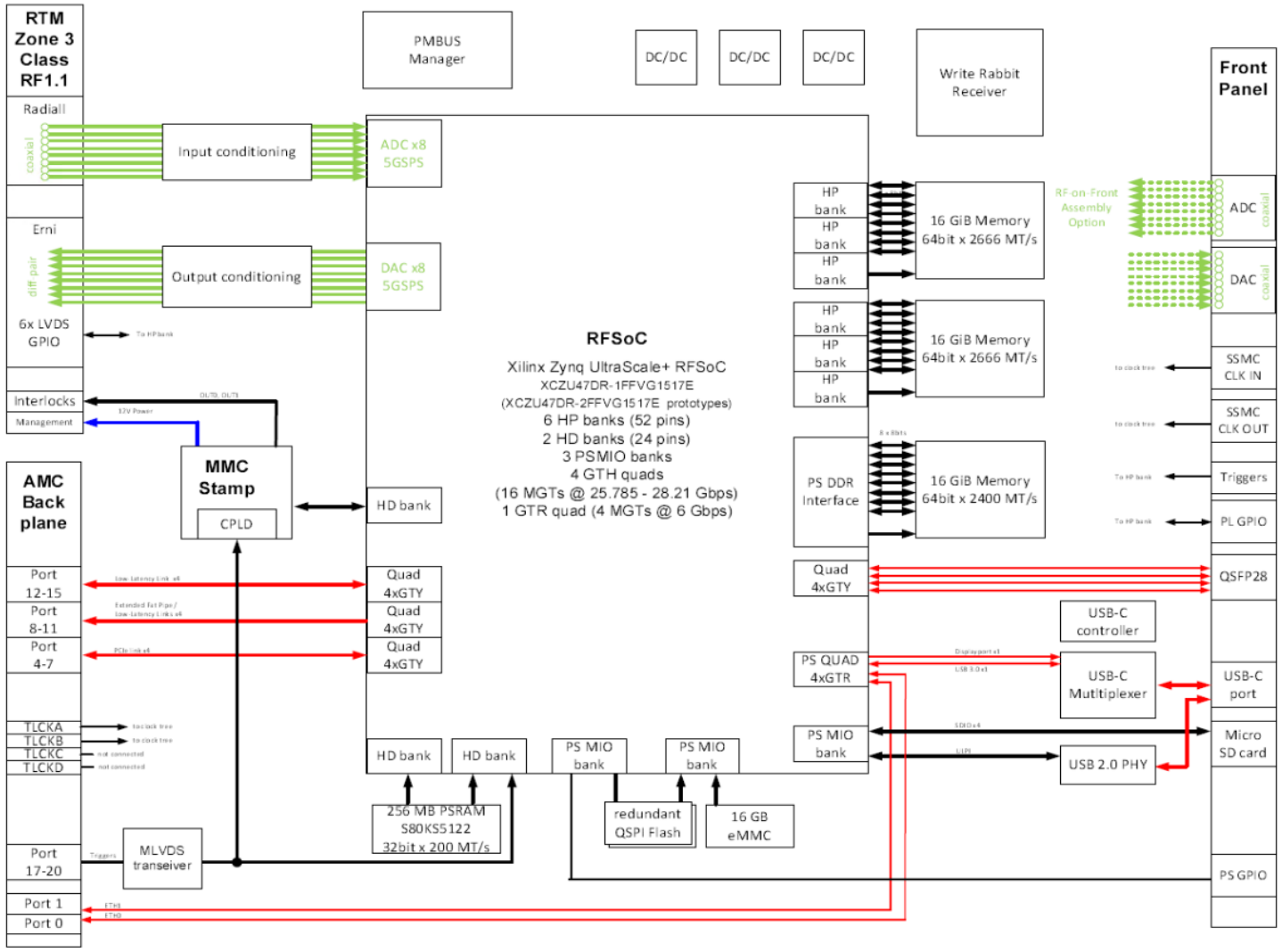
		Digital Clock IO	Digital fixed IO	Digital Clock Input	Digital user IO		Differential DACs			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D7-	RF-CLK3-	D5-	D2-	DAC7-	DAC4-	DAC1-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D7+	RF-CLK3+	D5+	D2+	DAC7+	DAC4+	DAC1+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D6-	RF-CLK1-	D4-	D1-	DAC6-	DAC3-	DAC0-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D6+	RF-CLK1+	D4+	D1+	DAC6+	DAC3+	DAC0+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	D3-	D0-CC-	DAC5-	DAC2-	GBT0-RX-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	D3+	D0-CC+	DAC5+	DAC2+	GBT0-RX+	PWRA2	PWRA1
		Single Ended Analog Signals									
J31		3	2	1							
	B	ADC-IN7	DAC-OUT1	DAC-OUT3							
	A	ADC-IN6	DAC-OUT0	DAC-OUT2							
J32		3	2	1							
	B	ADC-IN1	ADC-IN3	ADC-IN5							
	A	ADC-IN0	ADC-IN2	ADC-IN4							

Table 1: Zone 3 - Class RF1.1 pin assignment J30, J31 and J32 connector, AMC side view

DAMC-DS5014DR based on Xilinx Zynq UltraScale+ RFSoC Gen. 3

Basic parameters

- 8x ADC (grouped in 4 dual-channel tiles)
  - 14-bit resolution, sampling rate of 5 GSPS
  - AC-coupling (30 MHz – 6 GHz) to front panel or to Zone 3 connector (Class RF1.1) – single-ended
- 8x DAC (grouped in 2 four-channel tiles)
  - 14-bit resolution, sampling rate of 10 GSPS
  - AC-coupling (30 MHz – 6 GHz), single-ended to front panel or DC-coupling (DC – 2.5 GHz), differential to Zone 3 connector (Class RF1.1)
  - Variable output power (-22 dBm to 3 dBm)
- Memory
  - PS: 16GB 64-bit DDR4, PL: 2x 16GB 64-bit DDR4
  - eMMC-NAND FLASH, QSPI FLASH, Micro SD Card, PSRAM
- Interfaces
  - 100 GbE zQSFP+, USB type-C on the front panel
  - 12x GTY to AMC ports 4-15

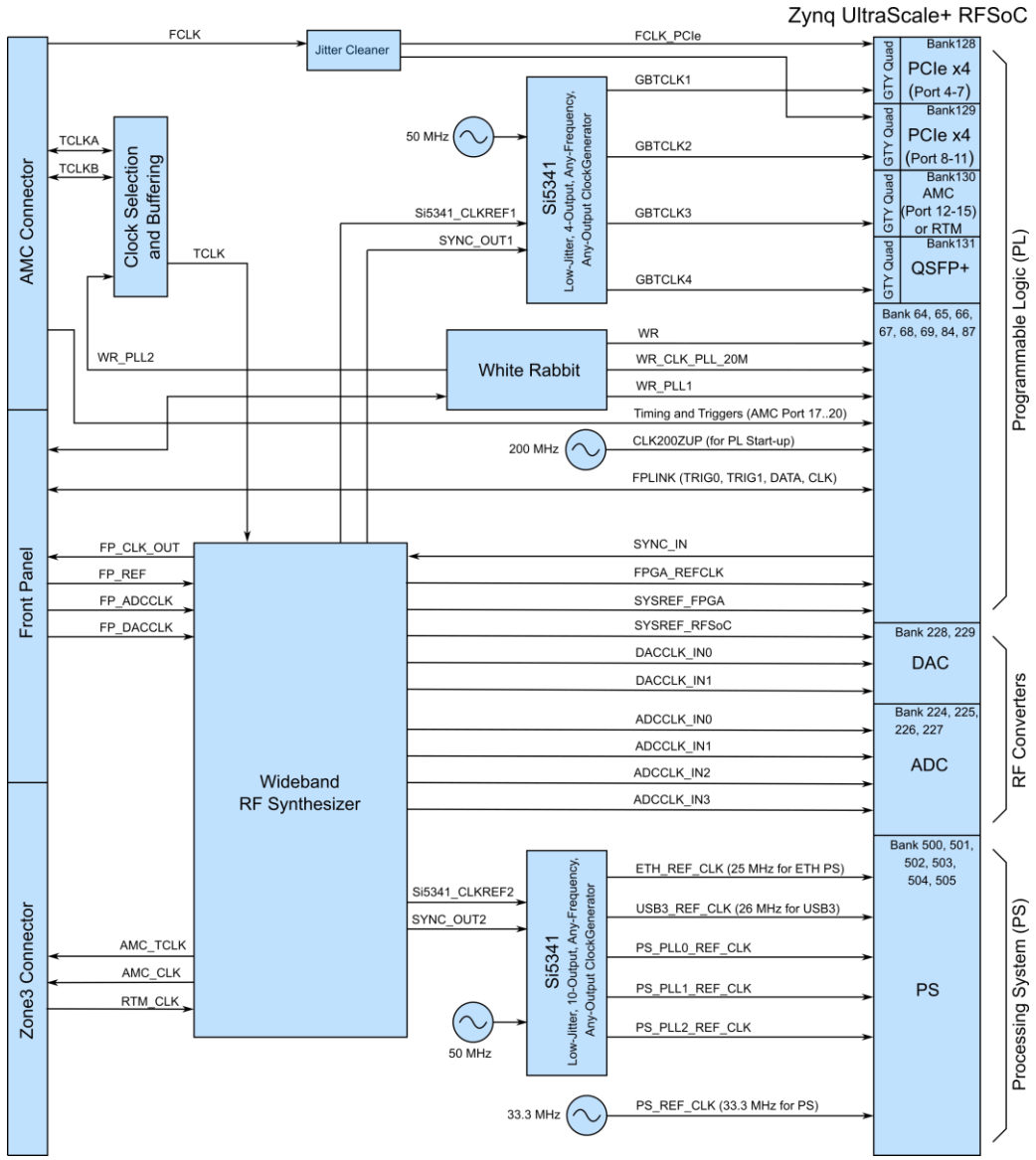


Courtesy of M. Fenner

DAMC-DS5014DR based on Xilinx Zynq UltraScale+ RFSoC Gen. 3

Clock tree + specification

- Clocking
  - External reference clock from front panel, RTM (RTM_CLK), TCLKA/B or WR
  - Sampling clock for the RF converters
    - Wideband RF synthesizer
    - External sampling clock from front panel
    - Clock generated by the internal RFSoC PLL
  - White Rabbit endpoint
  - Clock tree configurable from MMC Stamp or Processing System
- Specification (in preparation)
  - Detailed information on the DAMC-DS5014DR module parameters, interfaces and electrical properties

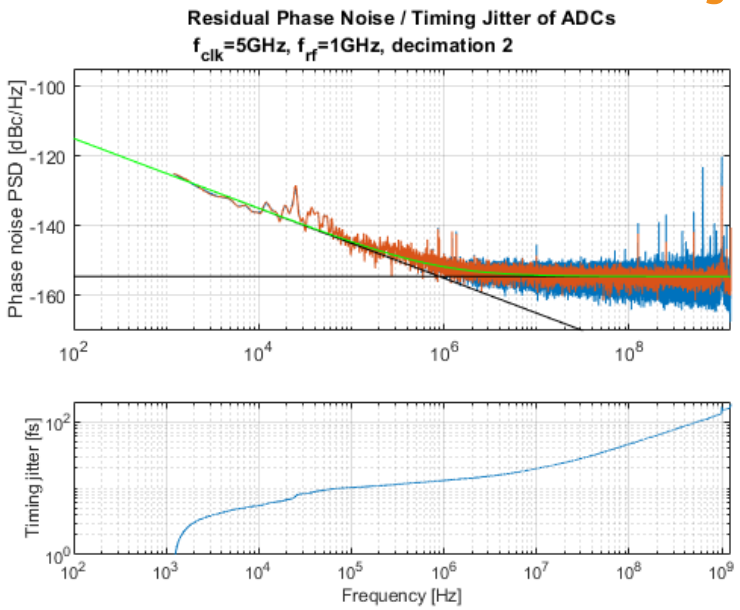


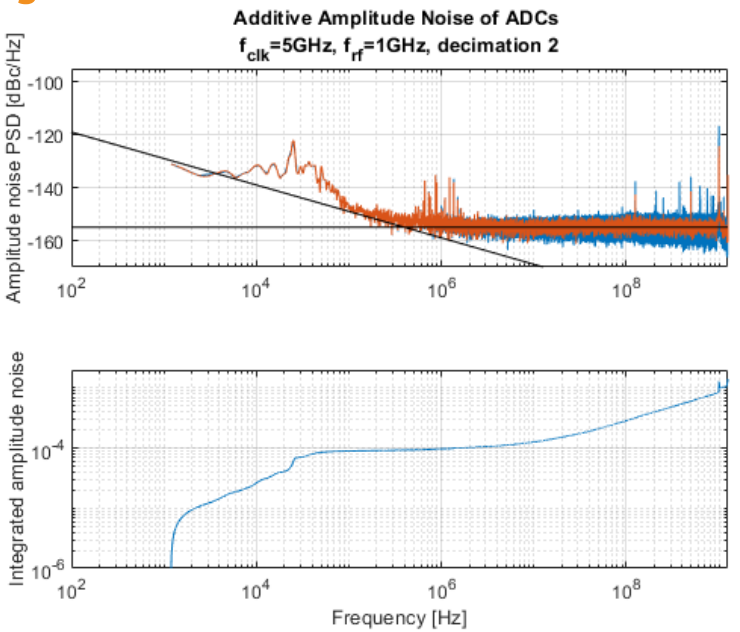
Xilinx Zynq UltraScale+ RFSoC Gen. 3

Performance of ADCs and DACs measured with the ZCU208 Eval Kit

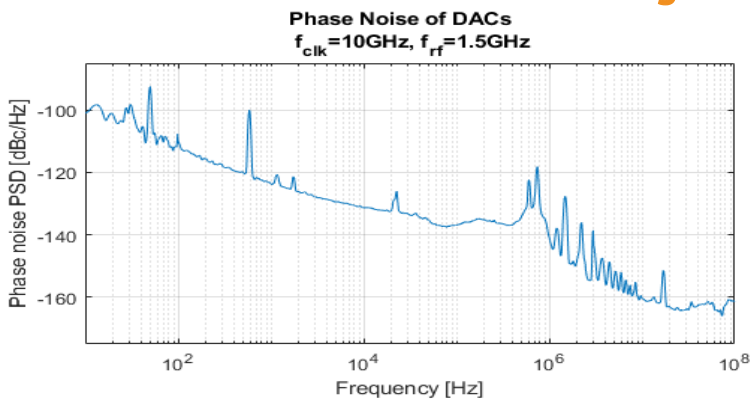
- ADCs (f_{clk}=5 GHz, f_{rf}=1 GHz)
  - Residual white phase noise: -154.5 dBc/Hz
  - Timing jitter: 70 fs rms (1kHz – 250MHz)
  - Addtive white amplitude noise: -155 dBc/Hz
  - Integrated Amplitude Noise: 0.044% (1kHz – 250MHz)
- DACs (f_{clk}=10 GHz, f_{rf}=1.5 GHz)
  - White phase noise: <-162 dBc/Hz
  - Timing jitter: 36.5 fs rms (10 Hz – 100 MHz)
  - White amplitude noise: <-165 dBc/Hz
  - Integrated Amplitude Noise: 0.020% (10 Hz – 10 MHz)

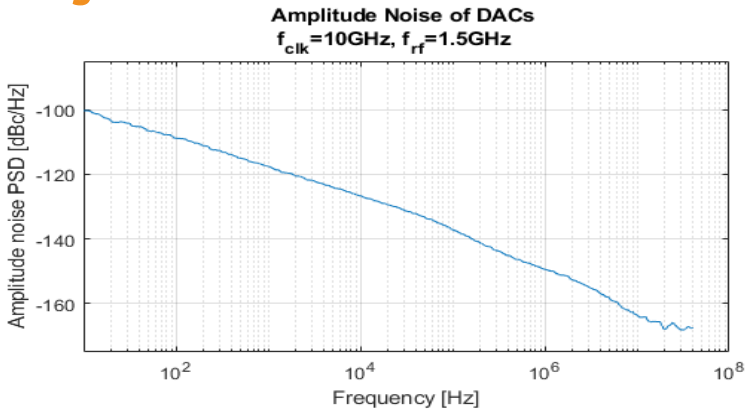
Noise of analog-to-digital converters





Noise of digital-to-analog converters

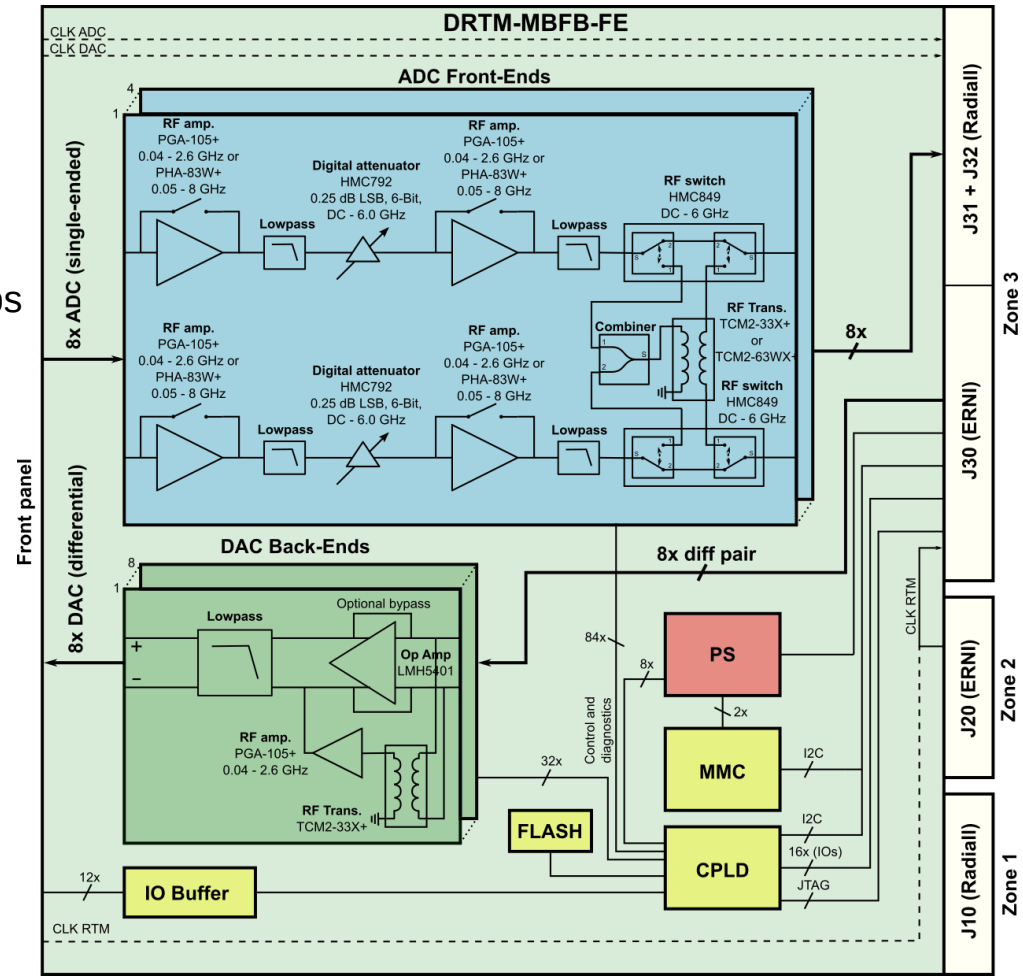


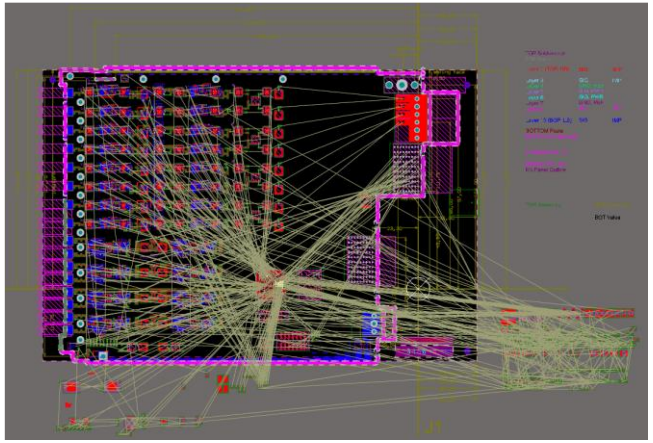


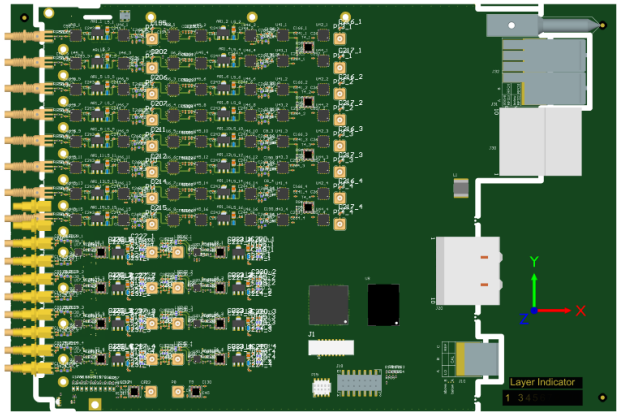
DRTM-MBFB-FE: front-end/back-end module for the DAMC-DS5014DR

Basic parameters

- 8x front-end for ADCs
  - Single-ended, AC-coupled
  - Possible various assembly versions
  - Bandwidth: 40 MHz – 6 GHz
  - Gain: -25 dB to +20 dB, 0.25 dB steps
  - Max. input RF power: +30 dBm
  - 2x up to 6-pole LC filters
- 8x back-end for DACs
  - Single-ended (AC-coupled) or differential (DC-coupled) output
  - Bandwidth: DC – 2.5 GHz
  - Output power: -15 dBm to +13 dBm
  - 2x up to 4-pole LC filters
- Class RF1.1
- CPLD for diagnostics and control



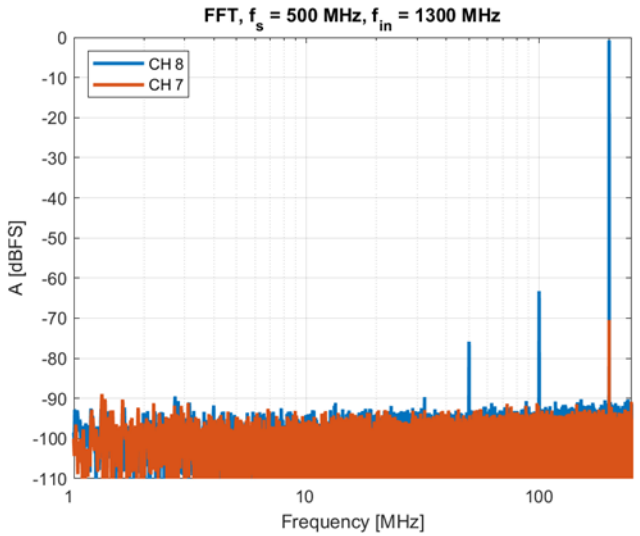


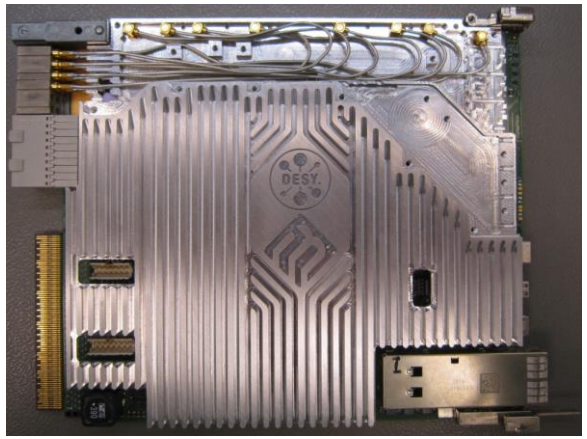


Diagnostics of high power amplifiers

DRTM-DS812FT + DAMC-DS812ZUP

- Low-latency, 8-channel, 12-bit digitizer
- AC/DC inputs on the AMC front panel or over Zone3 Class RF1.0
- 2.7-GHz bandwidth
- Non-harmonic SFDR of about -90 dBc
- Sampling rate of 500/800 MSPS each channel
- Zynq UltraScale+™ MPSoC
- 4 GBytes data memory
- Low-noise PLL with on-board VCSO and TXCO
- Trigger inputs and White Rabbit support
- PCIe Gen.3 x 8 and zQSFP+ support
- Support for JESD DACs via Zone 3





Pictures by courtesy of J. Zink

Summary

- MicroTCA.4 form factor with the „analog” RTMs fits well to implement wideband, reliable and high performance electronics for the Multi-Bunch Feedback of Petra IV
- RFSoC has been selected due to its compactness (lower PCB design effort), processing power, high-speed interfaces and low-noise RF-ADCs/RF-DACs
- The project involves the development of a few RTM/AMC modules, the system prototype is expected in 2024

Thank you

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